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Foundations of Analog and Digital Electronic Circuits

ANANT AGARWAL AND JEFFREY H. LANG

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In Praise of Foundations of Analog and Digital Electronic Circuits

"This book, crafted and tested with MIT sophomores in electrical engineering and computer science over a period of more than six years, provides a comprehensive treatment of both circuit analysis and basic electronic circuits. Examples such as digital and analog circuit applications, field-effect transistors, and operational amplifiers provide the platform for modeling of active devices, including large-signal, small-signal (incremental), nonlinear and piecewise-linear models. The treatment of circuits with energy-storage elements in transient and sinusoidal-steady-state circumstances is thorough and accessible. Having taught from drafts of this book five times, I believe that it is an improvement over the traditional approach to circuits and electronics, in which the focus is on analog circuits alone."

-PAUL E. GRAY, Massachusetts Institute of Technology

"My overall reaction to this book is overwhelmingly favorable. Well-written and pedagogically sound, the book provides a good balance between theory and practical application. I think that combining circuits and electronics is a very good idea. Most introductory circuit theory texts focus primarily on the analysis of lumped element networks without putting these networks into a practical electronics context. However, it is becoming more critical for our electrical and computer engineering students to understand and appreciate the common ground from which both fields originate."

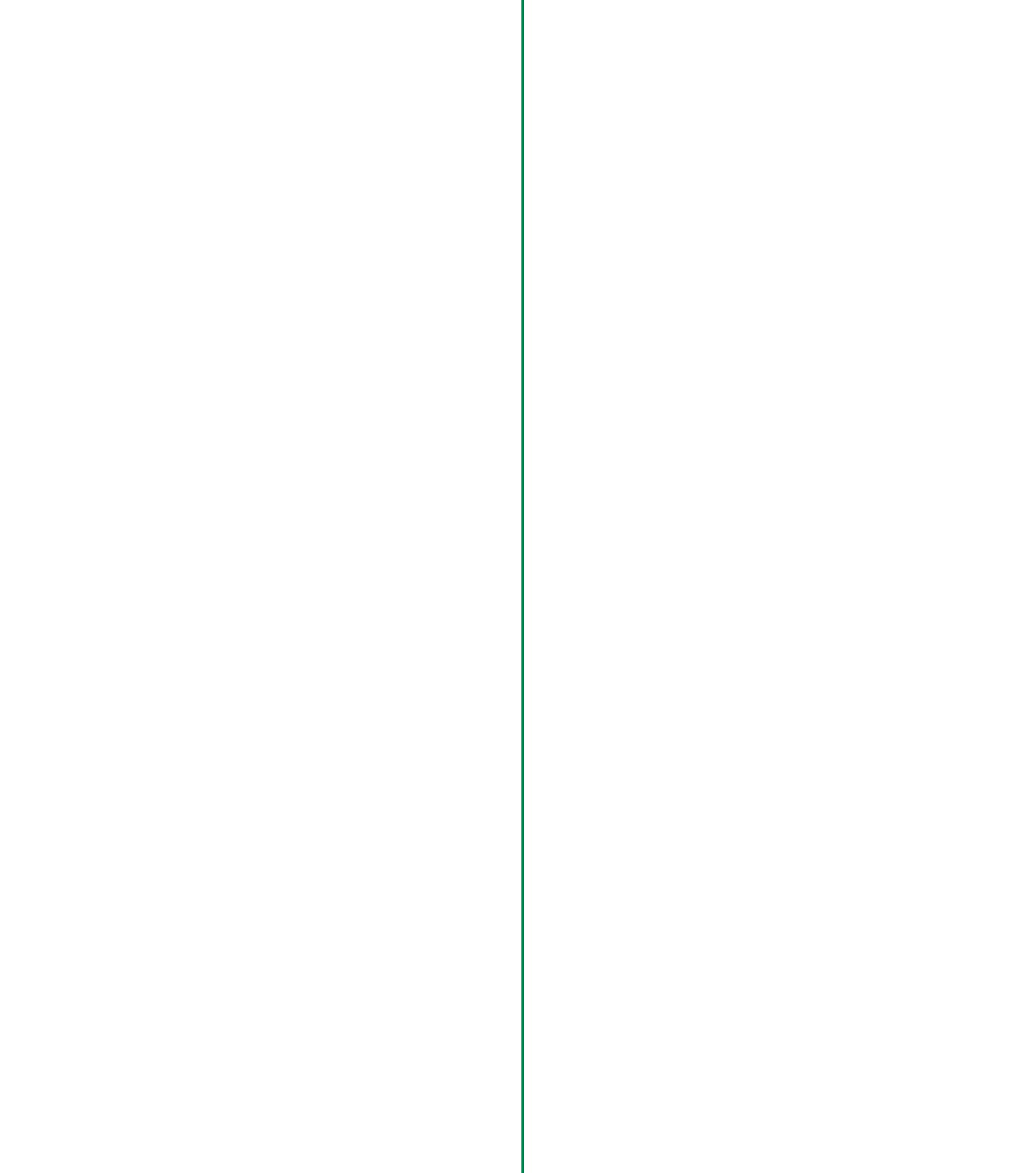
-GARY MAY, Georgia Institute of Technology

"Without a doubt, students in engineering today want to quickly relate what they learn from courses to what they experience in the electronics-filled world they live in. Understanding today's digital world requires a strong background in analog circuit principles as well as a keen intuition about their impact on electronics. In Foundations... Agarwal and Lang present a unique and powerful approach for an exciting first course introducing engineers to the world of analog and digital systems."

-RAVI SUBRAMANIAN, Berkeley Design Automation

"Finally, an introductory circuit analysis book has been written that truly unifies the treatment of traditional circuit analysis and electronics. Agarwal and Lang skillfully combine the fundamentals of circuit analysis with the fundamentals of modern analog and digital integrated circuits. I applaud their decision to eliminate from their book the usual mandatory chapter on Laplace transforms, a tool no longer in use by modern circuit designers. I expect this book to establish a new trend in the way introductory circuit analysis is taught to electrical and computer engineers."

-TIM TRICK, University of Illinois at Urbana-Champaign



Foundations of Analog and Digital Electronic Circuits

about the authors

Anant Agarwal is Professor of Electrical Engineering and Computer Science at the Massachusetts Institute of Technology. He joined the faculty in 1988, teaching courses in circuits and electronics, VLSI, digital logic and computer architecture. Between 1999 and 2003, he served as an associate director of the Laboratory for Computer Science. He holds a Ph.D. and an M.S. in Electrical Engineering from Stanford University, and a bachelor's degree in Electrical Engineering from IIT Madras. Agarwala led a group that developed Sparcle (1992), a multithreaded microprocessor, and the MIT Alewife (1994), a scalable shared-memory multiprocessor. He also led the Virtual Wires project at MIT and was a founder of Virtual Machine Works, Inc., which took the Virtual Wires logic emulation technology to market in 1993. Currently Agarwal leads the Raw project at MIT, which developed a new kind of reconfigurable computing chip. He and his team were awarded a Guinness world record in 2004 for LOUD, the largest microphone array in the world, which can pinpoint, track and amplify individual voices in a crowd. Co-founder of Engim, Inc., which develops multi-channel wireless mixed-signal chipsets, Agarwal also won the Maurice Wilkes prize for computer architecture in 2001, and the Presidential Young Investigator award in 1991.

Jeffrey H. Lang is Professor of Electrical Engineering and Computer Science at the Massachusetts Institute of Technology. He joined the faculty in 1980 after receiving his SB (1975), SM (1977) and Ph.D. (1980) degrees from the Department of Electrical Engineering and Computer Science. He served as the Associate Director of the MIT Laboratory for Electromagnetic and Electronic Systems between 1991 and 2003, and as an Associate Editor of "Sensors and Actuators" between 1991 and 1994. Professor Lang's research and teaching interests focus on the analysis, design and control of electromechanical systems with an emphasis on rotating machinery, micro-scale sensors and actuators, and flexible structures. He has also taught courses in circuits and electronics at MIT. He has written over 170 papers and holds 10 patents in the areas of electromechanics, power electronics and applied control, and has been awarded four best-paper prizes from IEEE societies. Professor Lang is a Fellow of the IEEE, and a former Hertz Foundation Fellow.

Agarwal and Lang have been working together for the past eighty years on a fresh approach to teaching circuits. For several decades, MIT had offered a traditional course in circuits designed as the first core undergraduate course in EE. But by the mid-'90s, vast advances in semiconductor technology, coupled with dramatic changes in students' background evolving from amateur radio to computer culture, had rendered this traditional course poorly motivated, and many parts of it were virtually obsolete. Agarwal and Lang decided to revamp and broaden this first course for EE, ECE or EECS by establishing a strong connection between the contemporary worlds of digital and analog systems, and by unifying the treatment of circuits and basic MOS electronics. As they developed the course, they solicited comments and received guidance from a large number of colleagues from MIT and other universities, students, and alumni, as well as industry leaders.

Unable to find a suitable text for their new introductory course, Agarwal and Lang wrote this book to follow the lectures schedule used in their course. "Circuits and Electronics" is taught in both the spring and fall semesters at MIT, and serves as a prerequisite for courses in signals and systems, digital/computer design, and advanced electronics. The course material is available worldwide on MIT's OpenCourseWare website, <http://ocw.mit.edu/OcwWeb/index.htm>.

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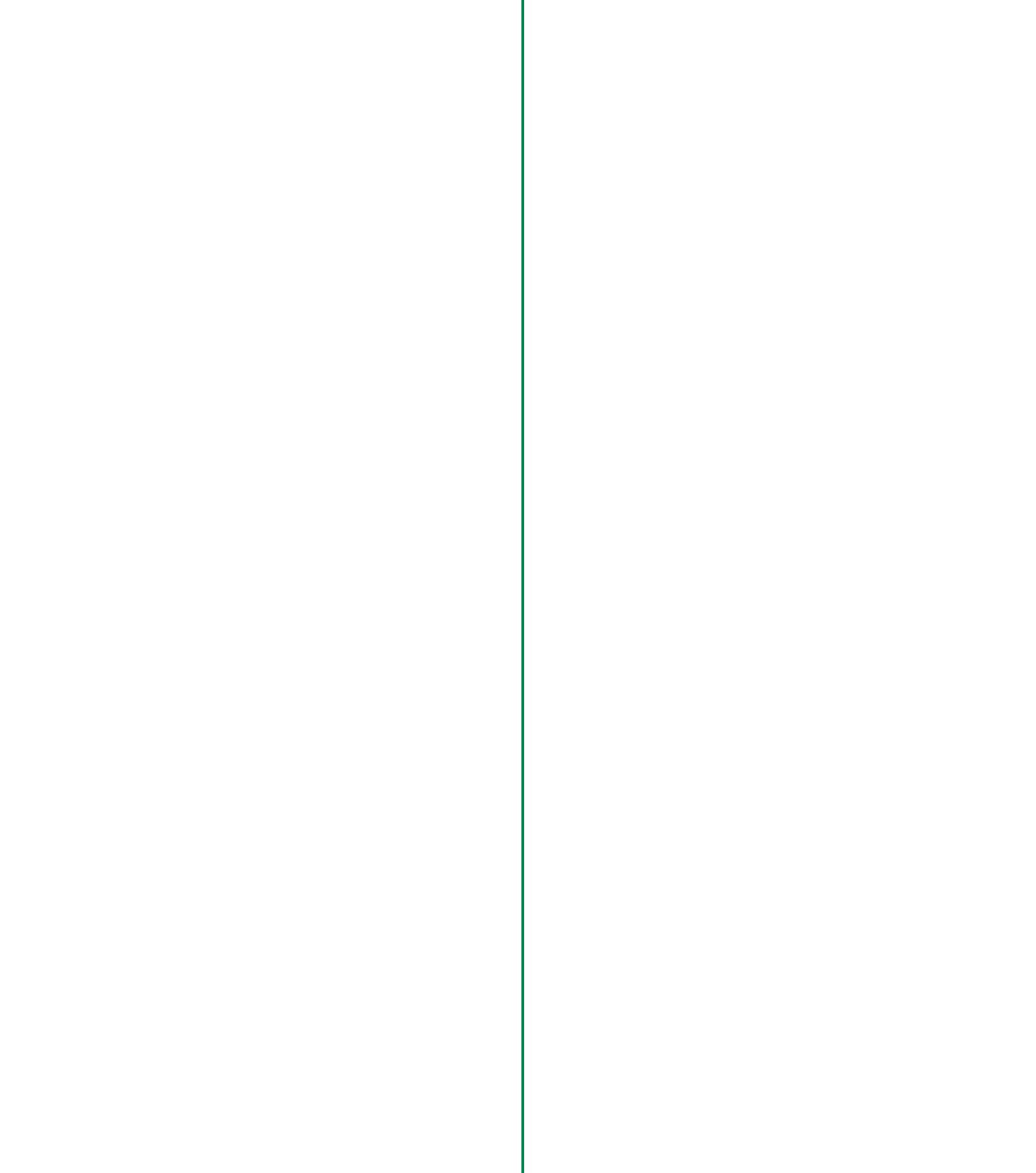
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ToAnu,Akash, and Anisha
—AnantAgarwal

ToMarija,Chris,John,Matt
—JeffreyLang



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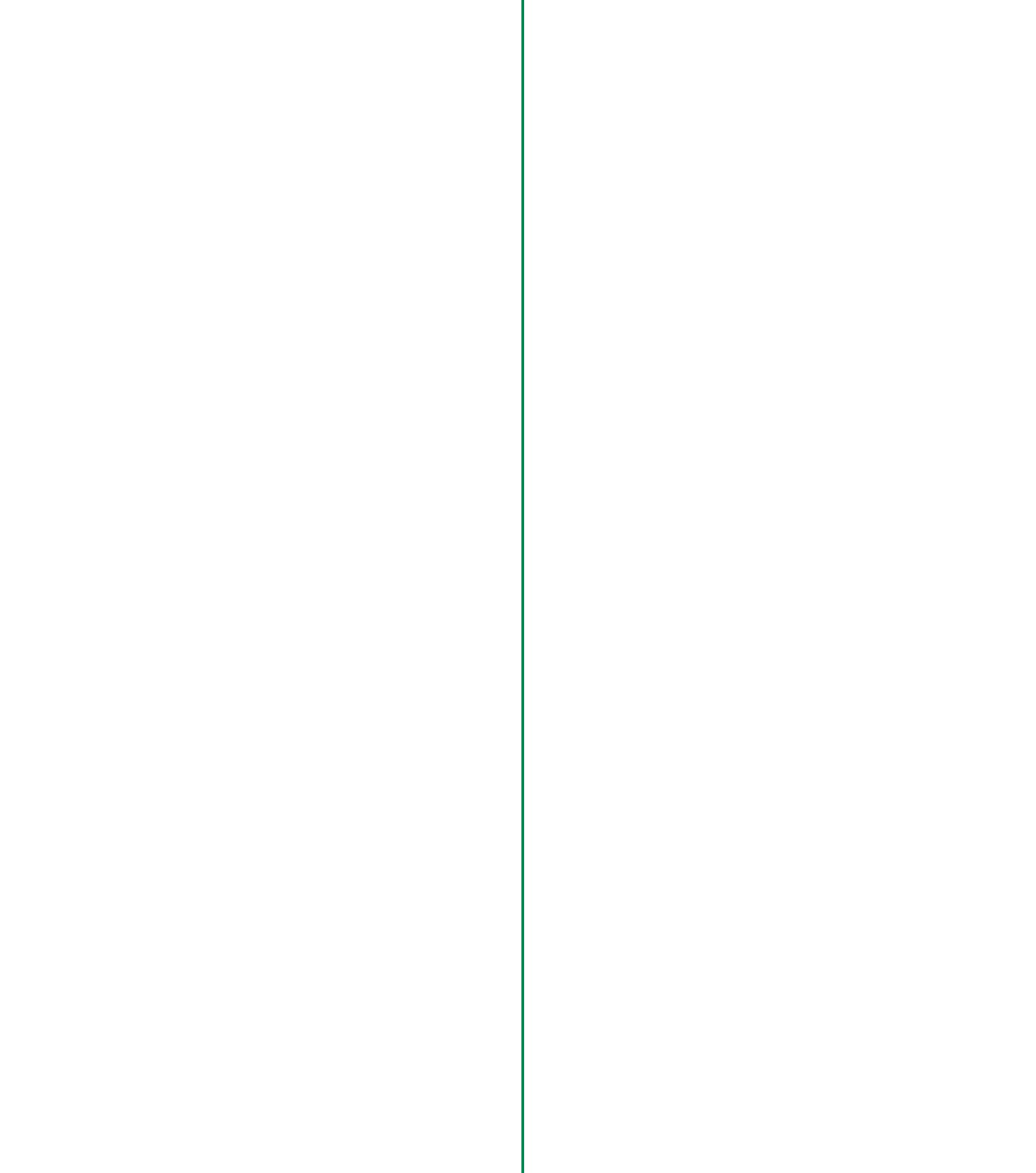
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preface

APPROACH

This book is designed to serve as a first course in an electrical engineering or an electrical engineering and computer science curriculum, providing students at the sophomore level a transition from the world of physics to the world of electronics and computation. The book attempts to satisfy two goals: Combine circuits and electronics into a single, unified treatment, and establish a strong connection with the contemporary worlds of both digital and analog systems.

These goals arise from the observation that the approach to introducing electrical engineering through a course in traditional circuit analysis is fast becoming obsolete. Our world has gone digital. A large fraction of the student population in electrical engineering is destined for industry or graduate study in digital electronics or computer systems. Even those students who remain in core electrical engineering are heavily influenced by the digital domain.

Because of this elevated focus on the digital domain, basic electrical engineering education must change in two ways: First, the traditional approach to teaching circuits and electronics without regard to the digital domain must be replaced by one that stresses the circuits foundations common to both the digital and analog domains. Because most of the fundamental concepts in circuits and electronics are equally applicable to both the digital and the analog domains, this means that, primarily, we must change the way in which we motivate circuits and electronics to emphasize their broader impact on digital systems. For example, although the traditional way of discussing the dynamic behavior of first-order RC circuits appears unmotivated to the student headed into digital systems, the same pedagogy is exciting when motivated by the switching behavior of a switch and resistor inverter driving a non-ideal capacitive wire. Similarly, we motivate the study of the step response of a second-order RLC circuit by observing the behavior of a MOS inverter when pin parasitics are included.

Second, given the additional demands of computer engineering, many departments can ill-afford the luxury of separate courses on circuits and on electronics. Rather, they might be combined into one course.¹ Circuits courses

¹In his paper, "Teaching Circuits and Electronicsto First-Year Students," in *Int. Symp. Circuits and Systems (ISCAS)*, 1998, Yannis Tsividis makes an excellent case for teaching an integrated course in circuits and electronics.

treat networks of passive elements such as resistors, sources, capacitors, and inductors. Electronics courses treat networks of both passive elements and active elements such as MOS transistors. Although this book offers a unified treatment for circuits and electronics, we have taken some pains to allow the crafting of a two-semester sequence— one focused on circuits and another on electronics — from the same basic content in the book.

Using the concept of “abstraction,” the book attempts to form a bridge between the world of physics and the world of large computer systems. In particular, it attempts to unify electrical engineering and computer science as the art of creating and exploiting successive abstractions to manage the complexity of building useful electrical systems. Computer systems are simply one type of electrical system.

In crafting a single text for both circuits and electronics, the book takes the approach of covering a few important topics in depth, choosing more contemporary devices when possible. For example, it uses the MOSFET as the basic active device, and delegates discussions of other devices such as bipolar transistors to the exercises and examples. Furthermore, to allow students to understand basic circuit concepts without trapping of specific devices, it introduces several abstract devices as examples and exercises. We believe this approach will allow students to tackle designs with many other extant devices and those that are yet to be invented.

Finally, the following are some additional differences from other books in this field:

The book draws a clear connection between electrical engineering and physics by showing clearly how the lumped circuit abstraction directly derives from Maxwell’s Equations and a set of simplifying assumptions.

The concept of abstraction is used throughout the book to unify the set of engineering simplifications made in both analog and digital design.

The book elevates the focus of the digital domain to that of analog. However, our treatment of digital systems emphasizes their analog aspects. We start with switches, sources, resistors, and MOSFETs, and apply KVL, KCL, and so on. The book shows that digital versus analog behavior is obtained by focusing on particular regions of device behavior.

The MOSFET device is introduced using a progression of models of increased refinement—the S model, the SR model, the SCS model, and the SU model.

The book shows how significant amounts of insight into the static and dynamic operation of digital circuits can be obtained with very simple models of MOSFETs.

Various properties of devices, for example, the memory property of capacitors, or the gain property of amplifiers, are related to both their use in analog circuits and digital circuits.

The state variable viewpoint of transient problems is emphasized for its intuitive appeal and since it motivates computer solutions of both linear or nonlinear network problems.

Issues of energy and power are discussed in the context of both analog and digital circuits.

A large number of examples are picked from the digital domain emphasizing VLSI concepts to emphasize the power and generality of traditional circuit analysis concepts.

With these features, we believe this book offers the needed foundation for students headed towards either the core electrical engineering majors including digital and RF circuits, communication, controls, signal processing, devices, and fabrication—or the computer engineering majors—including digital design, architecture, operating systems, compilers, and languages.

MIT has a unified electrical engineering and computer science department. This book is being used in MIT's introductory course on circuits and electronics. This course is offered each semester and is taken by about 500 students a year.

OVERVIEW

Chapter 1 discusses the concept of abstraction and introduces the lumped circuit abstraction. It discusses how the lumped circuit abstraction derives from Maxwell's Equations and provides the basic method by which electrical engineering simplifies the analysis of complicated systems. It then introduces several ideal, lumped elements including resistors, voltage sources, and current sources.

This chapter also discusses two major motivations of studying electronic circuits—modeling physical systems and information processing. It introduces the concept of a model and discusses how physical elements can be modeled using ideal resistors and sources. It also discusses information processing and signal representation.

Chapter 2 introduces KVL and KCL and discusses their relationship to Maxwell's Equations. It then uses KVL and KCL to analyze simple resistive networks. This chapter also introduces another useful element called the dependent source.

Chapter 3 presents more sophisticated methods for network analysis.

Chapter 4 introduces the analysis of simple, nonlinear circuits.

Chapter 5 introduces the digital abstraction, and discusses the second major simplification by which electrical engineers manage the complexity of building large systems.²

Chapter 6 introduces the switch element and describes how digital logic elements are constructed. It also describes the implementation of switches using MOS transistors. Chapter 6 introduces the S (switch) and the SR (switch-resistor) models of the MOSFET and analyzes simple switch circuits using the network analysis methods presented earlier. Chapter 6 also discusses the relationship between amplification and noise margins in digital systems.

Chapter 7 discusses the concept of amplification. It presents the SCS (switch-current-source) model of the MOSFET and builds a MOSFET amplifier.

Chapter 8 continues with small signal amplifiers.

Chapter 9 introduces storage elements, namely, capacitors and inductors, and discusses why the modeling of capacitances and inductances is necessary in high-speed design.

Chapter 10 discusses first order transients in networks. This chapter also introduces several major applications of first-order networks, including digital memory.

Chapter 11 discusses energy and power issues in digital systems and introduces CMOS logic.

Chapter 12 analyzes second order transients in networks. It also discusses the resonance properties of RLC circuits from a time-domain point of view.

Chapter 13 discusses sinusoidal steady state analysis as an alternative to the time-domain transient analysis. The chapter also introduces the concepts of impedance and frequency response. This chapter presents the design of filters as a major motivating application.

Chapter 14 analyzes resonant circuits from a frequency point of view.

Chapter 15 introduces the operational amplifier as a key example of the application of abstraction in analog design.

Chapter 16 discusses diodes and simple diode circuits.

The book also contains appendices on trigonometric functions, complex numbers, and simultaneous linear equations to help readers who need a quick refresher on these topics or to enable a quick lookup of results.

2. The point at which to introduce the digital abstraction in this book and in a corresponding curriculum was arguably the topic over which we agonized the most. We believe that introducing the digital abstraction at this point in the course balances (a) the need for introducing digital systems as early as possible in the curriculum to excite and motivate students (especially with laboratory experiments), with (b) the need for providing students with enough of a tool chest to be able to analyze interesting digital building blocks such as combinational logic. Note that we recommend introduction of digital systems a lot sooner than suggested by Tsividis in his 1998 ISCA Paper, although we completely agree his position on the need to include some digital design.

COURSE ORGANIZATION

The sequence of chapters has been organized to suit a one or two semester integrated course on circuits and electronics. First and second order circuits are introduced as late as possible to allow the students to attain a higher level of mathematical sophistication in situations in which they are taking a course on differential equations at the same time. The digital abstraction is introduced as early as possible to provide early motivation for the students.

Alternatively, the following chapter sequences can be selected to organize the course around a circuits sequence followed by an electronics sequence. The circuits sequence would include the following: Chapter 1 (lumped circuit abstraction), Chapter 2 (KV and KCL), Chapter 3 (network analysis), Chapter 5 (digital abstraction), Chapter 6 (S and SR MOS models), Chapter 9 (capacitors and inductors), Chapter 10 (first-order transients), Chapter 11 (energy and power, and CMOS), Chapter 12 (second-order transients), Chapter 13 (sinusoidal steady state), Chapter 14 (frequency analysis of resonant circuits), and Chapter 15 (operational amplifier abstraction—optional).

The electronics sequence would include the following: Chapter 4 (nonlinear circuits), Chapter 7 (amplifiers, the SCS MOSFET model), Chapter 8 (small-signal amplifiers), Chapter 13 (sinusoidal steady state and filters), Chapter 15 (operational amplifier abstraction), and Chapter 16 (diodes and power circuits).

Supplementary sections and examples. We have used the icon  in the text to identify sections or examples.

Instructor's manual

A link to the MIT OpenCourseWare website for the authors' course, 6.002 Circuits and Electronics. On this site you will find:

Syllabus. A summary of the objectives and learning outcomes for course 6.002.

Readings. Reading assignments based on Foundations of Analog and Digital Electronic Circuits.

Lecture Notes. Complete sets of lecture notes, accompanying video lectures, and descriptions of the demonstrations made by the instructor during class.

Labs. A collection of four labs: Thevenin/Norton Equivalents and Logic Gates, MOSFET Inverting Amplifiers and First-Order Circuits, Second-Order Networks, and Audio Playback System. Includes an equipment handout and lab tutorial. Labs include pre-lab exercises, in-lab exercises, and post-lab exercises.

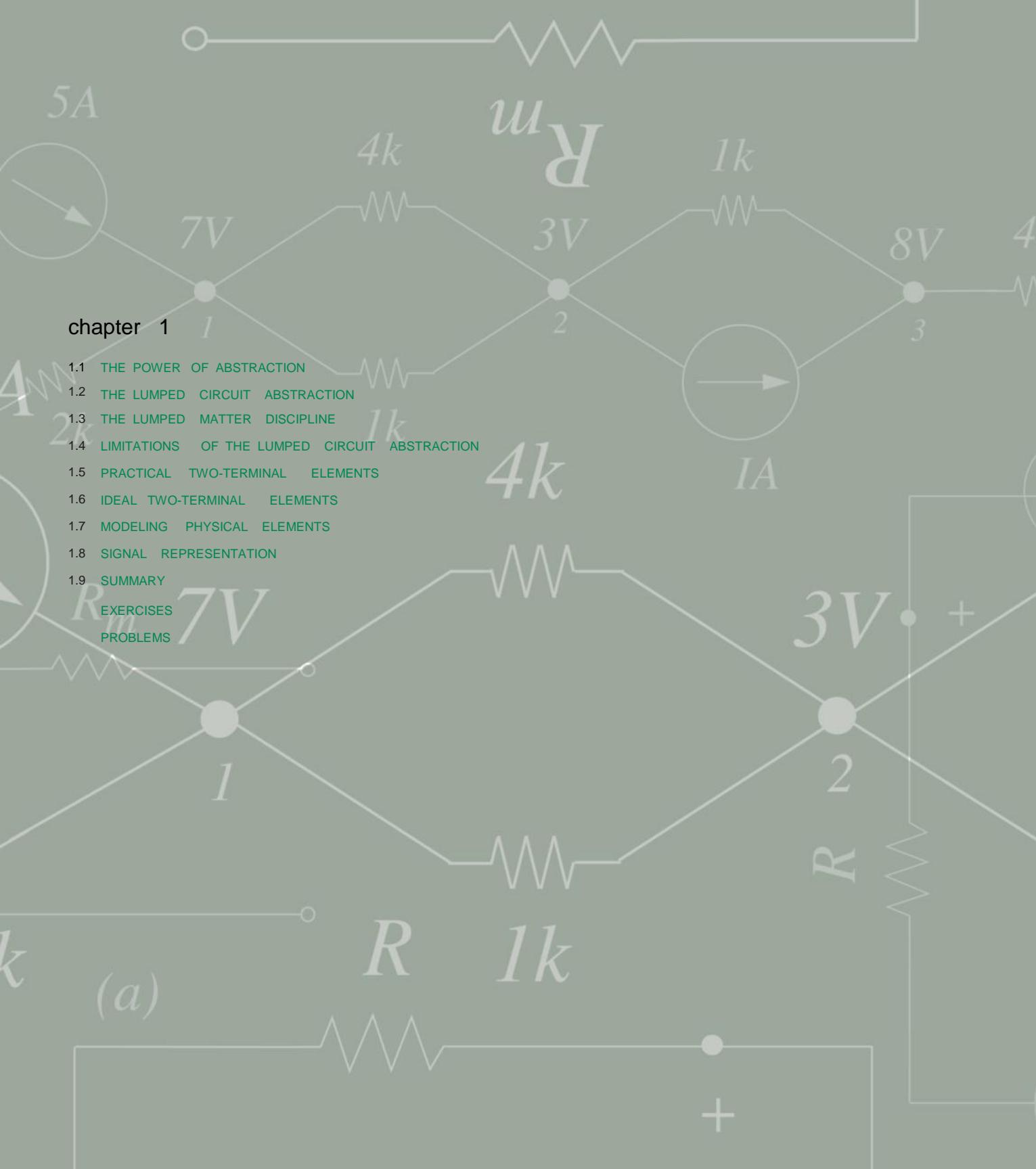
Assignments. A collection of eleven weekly homework assignments.

Exams. Two quizzes and a Final Exam.

Related Resources. Online exercises in Circuits and Electronics for demonstration and self-study.

ACKNOWLEDGMENTS

These notes evolved out of an initial set of notes written by Campbell Searle for 6.002 in 1991. The notes were also influenced by several who taught 6.002 at various times including Steve Senturia and Gerry Sussman. The notes have also benefited from the insights of Steve Ward, Tom Knight, Chris Terman, Ron Parker, Dimitri Antoniadis, Steve Umans, David Perreault, Karl Berggren, Gerry Wilson, Paul Gray, Keith Carver, Mark Horowitz, Yannis Tsividis, Cliff Pollock, Denise Penrose, Greg Schaffer, and Steve Senturia. We are also grateful to our reviewers including Timothy Trick, Barry Farbrother, John Pinkston, Stephane Lafortune, Gary May, Art Davis, Jeff Schowalter, John Uyemura, Mark Jupina, Barry Benedict, Barry Farbrother, and Ward Helms for their feedback. The help of Michael Zhang, Thit Minn, and Patrick Maurer in fleshing out problems and examples; that of Jose Oscar Mur-Miranda, Levente Jakab, Vishal Kapur, Matt Howland, Tom Kotwal, Michael Jura, Stephen Hou, Shelley Duvall, Amanda Wang, Ali Shoeb, Jason Kim, Charvak Karpe and Michael Jura in creating an answer key; that of Rob Geary, Yu Xinjie, Akash Agarwal, Chris Lang, and many of our students and colleagues in proofreading; and that of Anne McCarthy, Cornelia Colyer, and Jennifer Tucker in figure creation is also gratefully acknowledged. We gratefully acknowledge Maxim for their support of this book, and Ron Koo for making that support possible, as well as for capturing and providing us with numerous images of electronic components and chips. Ron Koo is also responsible for encouraging us to think about capturing and articulating the quick, intuitive process by which seasoned electrical engineers analyze circuits—our numerous sections on intuitive analysis are a direct result of his encouragement. We also thank Adam Brand and Intel Corp. for providing us with the images of the Pentium IV.



the circuit abstraction

1

“Engineering is the purposeful use of science.”

steve senturia

1.1 THE POWER OF ABSTRACTION

Engineering is the purposeful use of science. Science provides an understanding of natural phenomena. Scientific study involves experiment, and scientific laws are concise statements or equations that explain the experimental data. The laws of physics can be viewed as a layer of abstraction between the experimental data and the practitioners who want to use specific phenomena to achieve their goals, without having to worry about the specifics of the experiments and the data that inspired the laws. Abstractions are constructed with a particular set of goals in mind, and they apply when appropriate constraints are met. For example, Newton's laws of motion are simple statements that relate the dynamics of rigid bodies to their masses and external forces. They apply under certain constraints, for example, when the velocities are much smaller than the speed of flight. Scientific abstractions, or laws such as Newton's, are simple and easy to use, and enable us to harness and use the properties of nature.

Electrical engineering and computer science, or electrical engineering for short, is one of many engineering disciplines. Electrical engineering is the purposeful use of Maxwell's Equations (or Abstractions) for electromagnetic phenomena. To facilitate our use of electromagnetic phenomena, electrical engineering creates a new abstraction layer on top of Maxwell's Equations called the lumped circuit abstraction. By treating the lumped circuit abstraction layer, this book provides the connection between physics and electrical engineering. It unifies electrical engineering and computer science as the art of creating and exploiting successive abstractions to manage the complexity of building useful electrical systems. Computer systems are simply one type of electrical system.

The abstraction mechanism is very powerful because it can make the task of building complex systems tractable. As an example, consider the force equation:

$$F=ma. \quad (1.1)$$

The force equation enables us to calculate the acceleration of a particle with a given mass for an applied force. This simple force abstraction allows us to disregard many properties of objects such as their size, shape, density, and temperature, that are immaterial to the calculation of the object's acceleration. It also allows us to ignore the myriad details of the experiments and observations that led to the force equation, and accept it as given. Thus, scientific laws and abstractions allow us to leverage and build upon past experience and work. (Without the force abstraction, consider the pain we would have to go through to perform experiments to achieve the same result.)

Over the past century, electrical engineering and computer science have developed a set of abstractions that enable us to transition from the physical sciences to engineering and thereby to build useful, complex systems.

The set of abstractions that transition from science to engineering and insulate the engineer from scientific minutiae are often derived through the discretization discipline. Discretization is also referred to as lumping. A discipline is a self-imposed constraint. The discipline of discretization states that we choose to deal with discrete elements or ranges and ascribe a single value to each discrete element or range. Consequently, the discretization discipline requires us to ignore the distribution of values within a discrete element. Of course, this discipline requires that systems built on this principle operate within appropriate constraints so that the single-value assumption holds. As we will see shortly, the lumped circuit abstraction that is fundamental to electrical engineering and computer science is based on lumping or discretizing matter.¹ Digital systems use the digital abstraction, which is based on discretizing signal values. Clocked digital systems are based on discretizing both signals and time, and digital systolic arrays are based on discretizing signals, time and space.

Building upon the set of abstractions that define the transition from physics to electrical engineering, electrical engineering creates further abstractions to manage the complexity of building large systems. A lumped circuit element is often used as an abstract representation or a model of a piece of material with complicated internal behavior. Similarly, a circuit often serves as an abstract representation of interrelated physical phenomena. The operational amplifier composed of primitive discrete elements is a powerful abstraction that simplifies the building of bigger analog systems. The logic gate, the digital memory, the digital finite-state machine, and the microprocessor are themselves a succession of abstractions developed to facilitate building complex computer and control systems. Similarly, the art of computer programming involves the mastery of creating successively higher-level abstractions from lower-level primitives.

¹Notice that Newton's laws of physics are themselves based on discretizing matter. Newton's laws describe the dynamics of discrete bodies of matter by treating them as point masses. The spatial distribution of properties within the discrete elements are ignored.

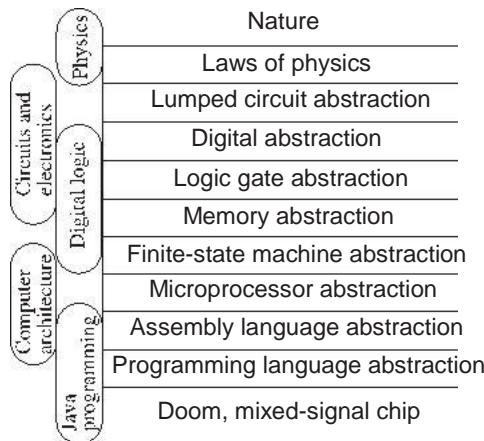


FIGURE 1.1 Sequence of courses and the abstraction layers introduced in a possible EECS course sequence that ultimately results in the ability to create the computer game “Doom,” or a mixed-signal (containing both analog and digital components) microprocessor supervisory circuit such as that shown in Figure 1.2.

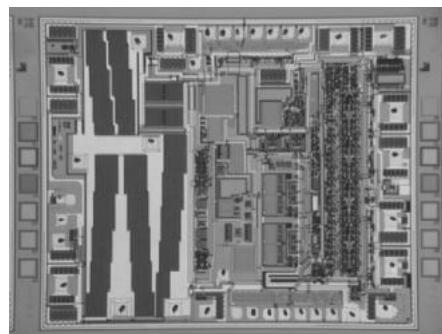


FIGURE 1.2 A photograph of the MAX807L microprocessor supervisory circuit from Maxim Integrated Products. The chip is roughly 2.5 mm by 3 mm. Analog circuits are to the left and center of the chip, while digital circuits are to the right. (Photograph Courtesy of Maxim Integrated Products.)

Figures 1.1 and 1.3 show possible course sequences that students might encounter in an EECS (Electrical Engineering and Computer Science) or an EE (Electrical Engineering) curriculum, respectively, to illustrate how each of the courses introduces several abstraction layers to simplify the building of useful electronics systems. This sequence of courses also illustrates how a circuits and electronics course using this book might fit within a general EE or EECS course framework.

1.2 THE LUMPED CIRCUIT ABSTRACTION

Consider the familiar lightbulb. When it is connected by a pair of cables to a battery, as shown in Figure 1.4a, it lights up. Suppose we are interested in finding out the amount of current flowing through the bulb. We might go about this by employing Maxwell’s equations and deriving the amount of current by

FIGURE 1.3 Sequence of courses and the abstraction layers that they introduce in a possible EE course sequence that ultimately results in the ability to create a wireless Bluetooth analog front-end chip.

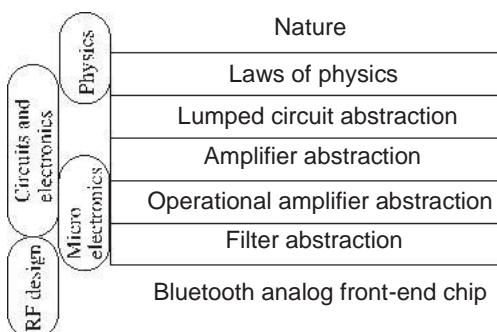
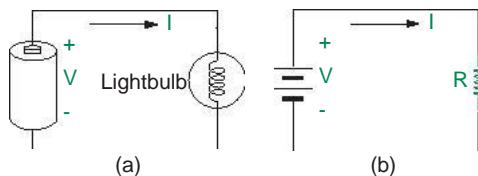


FIGURE 1.4 (a) A simple lightbulb circuit. (b) The lumped circuit representation.



a careful analysis of the physical properties of the bulb, the battery, and the cables. This is a horrendously complicated process.

As electrical engineers we are often interested in such computations in order to design more complex circuits, perhaps involving multiple bulbs and batteries. So how do we simplify our task? We observe that if we discipline ourselves to asking only simple questions, such as what is the net current flowing through the bulb, we can ignore the internal properties of the bulb and represent the bulb as a discrete element. Further, for the purpose of computing the current, we can create a discrete element known as a resistor and replace the bulb with it.² We define the resistance of the bulb R to be the ratio of the voltage applied to the bulb and the resulting current through it. In other words,

$$R = V/I.$$

Notice that the actual shape and physical properties of the bulb are irrelevant provided it offers the resistance R. We were able to ignore the internal properties and distribution of values inside the bulb simply by disciplining ourselves not to ask questions about those internal properties. In other words, when asking about the current, we were able to discretize the bulb into a single lumped element whose single relevant property was its resistance. This situation is

² We note that the relationship between the voltage and the current for a bulb is generally much more complicated.

analogous to the point mass simplification that resulted in the force relation in Equation 1.1, where the single relevant property of the object is its mass.

As illustrated in Figure 1.5, a lumped element can be idealized to the point where it can be treated as a black box accessible through a few terminals. The behavior at the terminals is more important than the details of the behavior internal to the blackbox. That is, what happens at the terminals is more important than how it happens inside the blackbox. Said another way, the blackbox is a layer of abstraction between the user of the bulb and the internal structure of the bulb.

The resistance is the property of the bulb of interest to us. Likewise, the voltage is the property of the battery that we most care about. Ignoring, for now, any internal resistance of the battery, we can lump the battery into a discrete element called by the same name supplying a constant voltage V , as shown in Figure 1.4b. Again, we can do this if we work with certain constraints to be discussed shortly, and provided we are not concerned with the internal properties of the battery, such as the distribution of the electrical field. In fact, the electric field within a real-life battery is horrendously difficult to chart accurately. Together, the collection of constraints that underlie the lumped circuit abstraction result in a marvelous simplification that allows us to focus on specifically those properties that are relevant to us.

Notice also that the orientation and shape of the wires are not relevant to our computation. We could even twist them or knot them in any way. Assuming for now that the wires are ideal conductors and offer zero resistance,³ we can rewrite the bulb circuit as shown in Figure 1.4b using lumped circuit equivalents for the battery and the bulb resistance, which are connected by ideal wires. Accordingly, Figure 1.4b is called the lumped circuit abstraction of the lightbulb circuit. If the battery supplies a constant voltage V and has zero internal resistance, and if the resistance of the bulb is R , we can use simple algebra to compute the current flowing through the bulb as

$$I = V/R.$$

Lumped elements in circuits must have a voltage V and a current I defined for their terminals.⁴ In general, the ratio of V and I need not be a constant.

The ratio is a constant (called the resistance R) only for lumped elements that

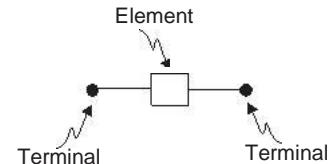


FIGURE 1.5 A lumped element.

3. If the wires offer non-zero resistance, then, as described in Section 1.6, we can separate each wire into an ideal wire reconnected in series with a resistor.

4. In general, the voltage and current can be time varying and can be represented in a more general form as $V(t)$ and $I(t)$. For devices with more than two terminals, the voltages are defined for any terminal with respect to any other reference terminal, and the currents are defined flowing into each of the terminals.

obey Ohm's law.⁵ The circuit comprising a set of lumped elements must also have a voltage defined between any pair of points, and a current defined into any terminal. Furthermore, the elements must not interact with each other except through their terminal currents and voltages. That is, the internal physical phenomena that make an element function must interact with the external electrical phenomena only at the electrical terminals of that element. As we will see in Section 1.3, lumped elements and the circuits formed using these elements must adhere to a set of constraints for these definitions and terminal interactions to exist. We name this set of constraints the lumped matter discipline.

The lumped circuit abstraction Capped a set of lumped elements that obey the lumped matter discipline using ideal wires to form an assembly that performs a specific function results in the lumped circuit abstraction.

Notice that the lumped circuit simplification is analogous to the point-mass simplification in Newton's laws. The lumped circuit abstraction represents the relevant properties of lumped elements using algebraic symbols. For example, we use R for the resistance of a resistor. Other values of interest, such as currents I and voltages V , are related through simple functions. The ease of using algebraic equations in place of Maxwell's equations to design and analyze complicated circuits will become much clearer in the following chapters.

The process of discretization can also be viewed as a way of modeling physical systems. The resistor is a model for a lightbulb if we are interested in finding the current flowing through the lightbulb for a given applied voltage. It can even tell us the power consumed by the lightbulb. Similarly, as we will see in Section 1.6, a constant voltage source is a good model for the battery when its internal resistance is zero. Thus, Figure 1.4 is also called the lumped circuit model of the lightbulb circuit. Models must be used only in the domain in which they are applicable. For example, the resistor model for a lightbulb tells us nothing about its cost or its expected lifetime.

The primitive circuit elements, the means for combining them, and the means of abstraction form the graphical language of circuits. Circuit theory is a well-established discipline. With maturity has come widespread utility. The language of circuit theory has become universal for problem-solving in many disciplines. Mechanical, chemical, metallurgical, biological, thermal, and even economic processes are often represented in circuit theory terms, because the mathematics for analysis of linear and nonlinear circuits is both powerful and well-developed. For this reason electronic circuit models are often used as analogs in the study of many physical processes. Readers whose main focus is some area of electrical engineering other than electronics should therefore review the material in this

⁵ Observe that Ohm's law itself is an abstraction for the electrical behavior of resistive material that allows us to replace tables of experimental data relating V and I by a simple equation.

book from the broad perspective of an introduction to the modeling of dynamic systems.

1.3 THE LUMPED MATTER DISCIPLINE

The scope of these equations is remarkable, including as it does the fundamental operating principles of all large-scale electromagnetic devices such as motors, cyclotrons, electronic computers, television, and microwave radar.

[halliday and resnick on maxwell's equations](#)

Lumped circuits comprise lumped elements (or discrete elements) connected by ideal wires. A lumped element has the property that a unique terminal voltage $V(t)$ and terminal current $I(t)$ can be defined for it. As depicted in Figure 1.6, for a two-terminal element, V is the voltage across the terminals of the element,⁶ and I is the current through the element.⁷ Furthermore, for lumped resistive elements, we can define a single property called the resistance R that relates the voltage across the terminals to the current through the terminals.

The voltage, the current, and the resistance are defined for an element only under certain constraints that we collectively call the lumped matter discipline (LMD). Once we adhere to the lumped matter discipline, we can make several simplifications in our circuit analysis and work with the lumped circuit abstraction. Thus the lumped matter discipline provides the foundation for the lumped circuit abstraction, and is the fundamental mechanism by which we are able to move from the domain of physics to the domain of electrical engineering. We will simply state these constraints here, but relegate the development of the constraints of the lumped matter discipline to Section A.1 in Appendix A. Section A.2 further shows how the lumped matter discipline results in the simplification of Maxwell's equations into the algebraic equations of the lumped circuit abstraction.

The lumped matter discipline imposes three constraints on how we choose lumped circuit elements:

1. Choose lumped element boundaries such that the rate of change of magnetic flux linked with any closed loop outside an element must be zero for all time. In other words, choose element boundaries such that

$$\frac{\partial \mathbf{B}}{\partial t} = 0$$

through any closed path outside the element.

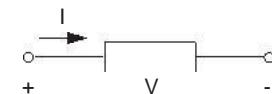


FIGURE 1.6 A lumped circuit element.

6. The voltage across the terminals of an element is defined as the work done in moving a unit charge (one coulomb) from one terminal to the other through the element against the electrical field. Voltages are measured in volts (V), where one volt is one joule per coulomb.

7. The current is defined as the rate of flow of charge from one terminal to the other through the element. Current is measured in amperes (A), where one ampere is one coulomb per second.

2. Choose lumped element boundaries so that there is no total time-varying charge within the element for all time. In other words, choose element boundaries such that

$$\frac{\partial q}{\partial t} = 0$$

where q is the total charge within the element.

3. Operate in the regime in which signal timescales of interest are much larger than the propagation delay of electromagnetic waves across the lumped elements.

The intuition behind the first constraint is as follows. The definition of the voltage (or the potential difference) between a pair of points across an element is the work required to move a particle with unit charge from one point to the other along some path against the force due to the electrical field. For the lumped abstraction to hold, we require that this voltage be unique, and therefore the voltage value must not depend on the path taken. We can make this true by selecting element boundaries such that there is no time-varying magnetic flux outside the element.

If the first constraint allowed us to define a unique voltage across the terminals of an element, the second constraint results from our desire to define a unique value for the current entering and exiting the terminals of the element. A unique value for the current can be defined if we do not have charge buildup or depletion inside the element over time.

Under the first two constraints, elements do not interact with each other except through their terminal currents and voltages. Notice that the first two constraints require that the rate of change of magnetic flux outside the elements and net charge within the elements is zero for all time.⁸ It directly follows that the magnetic flux and the electric fields outside the elements are also zero. Thus there are no fields related to one element that can exert influence on the other elements. This permits the behavior of each element to be analyzed independently.⁹ The results of this analysis are then summarized by the

8. As discussed in Appendix A, assuming that the rate of change is zero for all time ensures that voltages and currents can be arbitrary functions of time.

9. The elements in most circuits will satisfy the restriction of non-interaction, but occasionally they will not. As will be seen later in this text, the magnetic fields from two inductors in close proximity might extend beyond the material boundaries of the respective inductors inducing significant electric fields in each other. In this case, the two inductors could not be treated as independent circuit elements. However, they could perhaps be treated together as a single element, called a transformer, if their distributed coupling could be modeled appropriately. A dependent source is yet another example of a circuit element that we will introduce later in this text in which interacting circuit elements are treated together as a single element.

relation between the terminal current and voltage of that element, for example, $V=IR$. More examples of such relations, or element laws, will be presented in Section 1.6.2. Further, when the restriction of non-interaction is satisfied, the focus of circuit operation becomes the terminal currents and voltages, and not the electromagnetic fields within the elements. Thus, these currents and voltages become the fundamental signals within the circuit. Such signals are discussed further in Section 1.8.

Let us dwell for a little longer on the third constraint. The lumped element approximation requires that we be able to define a voltage V between a pair of element terminals (for example, the two ends of a bulb filament) and a current through the terminal pair. Defining a current through the element means that the current in must equal the current out. Now consider the following thought experiment. Apply a current pulse at one terminal of the filament at time instant t and observe both the current into this terminal and the current out of the other terminal at a time instant $t+dt$ very close to t . If the filament were long enough, or if dt were small enough, the finite speed of electromagnetic waves might result in our measuring different values for the current in and the current out.

We cannot make this problem go away by postulating constant currents and voltages, since we are very much interested in situations such as those depicted in Figure 1.7, in which a time-varying voltage source drives a circuit.

Instead, we fix the problem created by the finite propagation speeds of electromagnetic waves by adding the third constraint, namely, that the timescale of interest in our problem be much larger than electromagnetic propagation delays through our elements. Put another way, the size of our lumped elements must be much smaller than the wavelength associated with the V and I signals.¹⁰

Under these speed constraints, electromagnetic waves can be treated as if they propagated instantly through a lumped element. By neglecting propagation

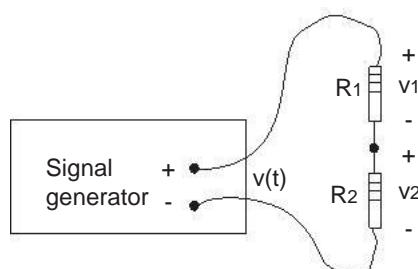


FIGURE 1.7 Resistor circuit connected to a signal generator.

¹⁰More precisely, the wavelength that we are referring to is that wavelength of the electromagnetic wave launched by the signals.

effects, the lumped element approximation becomes analogous to the point-mass simplification, in which we are able to ignore many physical properties of elements such as their length, shape, size, and location.

Thus far, our discussion focused on the constraints that allowed us to treat individual elements as being lumped. We can now turn our attention to circuits. As defined earlier, circuits are sets of lumped elements connected by ideal wires. Currents outside the lumped elements are confined to the wires. An ideal wire does not develop a voltage across its terminals, irrespective of the amount of current it carries. Furthermore, we choose the wires such that they obey the lumped matter discipline, so the wires themselves are also lumped elements.

For their voltages and currents to be meaningful, the constraints that apply to lumped elements apply to entire circuits as well. In other words, for voltages between any pair of points in the circuit and for currents through wires to be defined, any segment of the circuit must obey a set of constraints similar to those imposed on each of the lumped elements.

Accordingly, the lumped matter discipline for circuits can be stated as

1. The rate of change of magnetic flux linked with any portion of the circuit must be zero for all time.
2. The rate of change of the charge at any node in the circuit must be zero for all time. Anode is any point in the circuit at which two or more element terminals are reconnected using wires.
3. The signal timescales must be much larger than the propagation delay of electromagnetic waves through the circuit.

Notice that the first two constraints follow directly from the corresponding constraints applied to lumped elements. (Recall that wires are themselves lumped elements.) So, the first two constraints do not imply any new restrictions beyond those already assumed for lumped elements.¹¹

The third constraint for circuits, however, imposes a stronger restriction on signal timescales than for elements, because a circuit can have a much larger physical extent than a single element. The third constraint says that the circuit must be much smaller in all its dimensions than the wavelength of light at the highest operating frequency of interest. If this requirement is satisfied, then wave phenomena are not important to the operation of the circuit. The circuit operates quasi-statically, and information propagates instantaneously across it. For example, circuits operating in vacuum or air at 1 kHz, 1 MHz, and 1 GHz would have to be much smaller than 300 km, 300 m, and 300 mm, respectively.

¹¹As we shall see in Chapter 9, it turns out that voltages and currents in circuits result in electric and magnetic fields, thus appearing to violate the set of constraints to which we promised to adhere. In most cases these are negligible. However, when their effects cannot be ignored, we explicitly model them using elements called capacitors and inductors.

Most circuits satisfy such a restriction. But, interestingly, an uninterrupted 5000-km power grid operating at 60 Hz, and a 30-cm computer motherboard operating at 1 GHz, would not. Both systems are approximately one wavelength in size; wave phenomena are every important to their operation and they must be analyzed accordingly. Wave phenomena are now becoming important to microprocessors as well. We will address this issue in more detail in Section 1.4.

When a circuit meets these three constraints, the circuit can itself be abstracted as a lumped element with external terminals for which voltages and currents can be defined. Circuits that adhere to the lumped matter discipline yield additional simplifications in circuit analysis. Specifically, we will show in Chapter 2 that the voltages and currents across the collection of lumped circuit elements obey simple algebraic relationships stated as two laws: Kirchhoff's voltage law (KVL) and Kirchhoff's current law (KCL).

1.4 LIMITATIONS OF THE LUMPED CIRCUIT ABSTRACTION

We used the lumped circuit abstraction to represent the circuit pictured in Figure 1.4a by the schematic diagram of Figure 1.4b. We stated that it was permissible to ignore the physical extent and topology of the wires connecting the elements and define voltages and currents for the elements provided they met the lumped matter discipline.

The third postulate of the lumped matter discipline requires us to limit ourselves to signal speeds that are significantly lower than the speed of electromagnetic waves. As technology advances, propagation effects are becoming hard to ignore. In particular, as computer speed surpasses the gigahertz range, increasing signal speeds and fixed system dimensions tend to break our abstractions, so that engineers working on the forefront of technology must constantly revisit the disciplines upon which abstractions are based and prepare to resort to fundamental physics if the constraints are violated.

As an example, let us work out the numbers for a microprocessor. In a microprocessor, the conductors are typically encased in insulators such as silicon dioxide. These insulators have dielectric constants nearly four times that of free space, and so electromagnetic waves travel only half as fast through them. Electromagnetic waves travel at the speed of approximately 1 foot or 30 cm per nanosecond in vacuum, so they travel at roughly 6 inches or 15 cm per nanosecond in the insulators. Since modern microprocessors (for example, the Alpha microprocessor from Digital/Compaq) can approach 2.5 cm in size, the propagation delay of electromagnetic waves across the chip is on the order of 1/6 ns. These microprocessors are approaching a clock rate of 2 GHz in 2001. Taking the reciprocal, this translates to a clock cycle time of 1/2 ns. Thus, the wave propagation delay across the chip is about 33% of a clock cycle. Although techniques such as pipelining attempt to reduce the number of

elements (and therefore distance) a signal traverses in a clock cycle, certain clock or power lines in microprocessors can travel the full extent of the chip, and will suffer this large delay. Here, wave phenomena must be modeled explicitly.

In contrast, slower chips built in earlier times satisfied our lumped matter discipline more easily. For example, the MIPS microprocessor built in 1984 was implemented on a chip that was 1 cm on a side. It ran at a speed of 20 MHz, which translates to a cycle time of 50 ns. The wave propagation delay across the chip was 1/15 ns, which was significantly smaller than the chip's cycle time.

As another example, a Pentium II chip built in 1998 clocked at 400 MHz, but used a chip size that was more or less the same as that of the MIPS chip—namely, about 1 cm on a side. As calculated earlier, the wave propagation delay across a 1-cm chip is about 1/15 ns. Clearly the 2.5-ns cycle time of the Pentium II chip is still significantly larger than the wave propagation delay across the chip.

Now consider a Pentium IV chip built in 2004 that clocked at 3.4 GHz, and was roughly 1 cm on a side. The 0.29-ns cycle time is only four times the wave propagation delay across the chip!

If we are interested in signal speeds that are comparable to the speed of electromagnetic waves, then the lumped matter discipline is violated, and therefore we cannot use the lumped circuit abstraction. Instead, we must resort to distributed circuit models based on elements such as transmission lines and waveguides.¹² In these distributed elements, the voltages and currents at any instant of time are a function of the location within the elements. The treatment of distributed elements are beyond the scope of this book.

The lumped circuit abstraction encounters other problems with time-varying signals even when signal frequencies are small enough that propagation effects can be neglected. Let us revisit the circuit pictured in Figure 1.7 in which a signal generator drives a resistor circuit. It turns out that under certain conditions the frequency of the oscillator and the lengths and layout of the wires may have a profound effect on the voltages. If the oscillator is generating a sine wave at some low frequency, such as 256 Hz (Middle C in musical terms), then the voltage divider relation developed in Chapter 2 (Equation 2.138) could be used to calculate with some accuracy the voltage across R_2 . But if the frequency of the sine wave were 100 MHz (1×10^8 Hz), then we have a problem. As we will see later, capacitive and inductive effects in the resistors and the wires (resulting from electric fields and magnetic fluxes generated by the signal) will

¹² In case you are wondering how the Pentium IV and similar chips get away with high clock speeds, the key lies in designing circuits and laying them out on the chip in a way that most signals traverse a relatively small fraction of the chip in a clock cycle. To enable succeeding generations of the chip to be clocked faster, signals must traverse progressively shorter distances. A technique called pipelining is the key enabling mechanism that accomplishes this. The few circuits in which signals travel the length of the chip must be designed with extreme care using transmission line analysis.

seriously affect the circuit behavior, and these are not currently represented in our model. In Chapter 9, we will separate these effects into new lumped elements called capacitors and inductors so our lumped circuit abstraction holds at high frequencies as well.

All circuit model discussions in this book are predicated on the assumption that the frequencies involved are low enough that the effects of the fields can be adequately modeled by lumped elements. In Chapters 1 through 8, we assume that the frequencies involved are even lower so we can ignore real capacitive and inductive effects as well.

Are there other additional practical considerations in addition to the constraints imposed by the lumped matter discipline? For example, are we justified in neglecting contact potentials, and lumping all battery effects in V ? Can we neglect all resistance associated with the wires, and lump all the resistive effects in a series connected resistor? Does the voltage V change when the resistors are connected and current flows? Some of these issues will be addressed in Sections 1.6 and 1.7.

1.5 PRACTICAL TWO-TERMINAL ELEMENTS

Resistors and batteries are two of our most familiar lumped elements. Such lumped elements are the primitive building blocks of electronic circuits. Electronic access to an element is made through its terminals. At times, terminals are repaired together in a natural way to form ports. These ports offer an alternative view of how electronic access is made to an element. An example of an arbitrary element with two terminals and one port is shown in Figure 1.8. Other elements may have three or more terminals, and two or more ports.

Most circuit analyses are effectively carried out on circuits containing only two-terminal elements. This is due in part to the common use of two-terminal elements, and in part to the fact that most, if not all, elements having more than two terminals are usually modeled using combinations of two-terminal elements. Thus, two-terminal elements appear prominently in all electronic

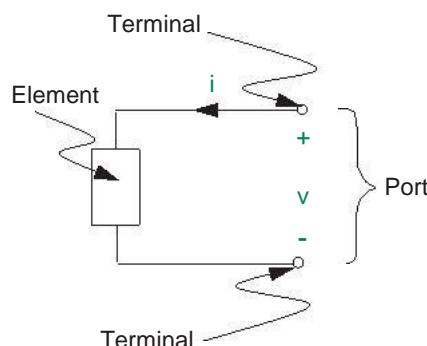


FIGURE 1.8 An arbitrary two-terminal circuit element.

circuit analyses. In this section, we discuss a couple of familiar examples of two-terminal elements—resistors and batteries.

1.5.1 BATTERIES

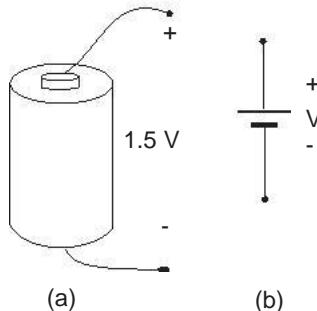


FIGURE 1.9 Symbol for battery.

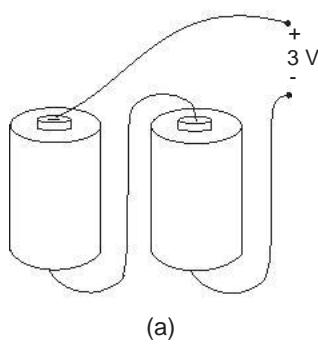


FIGURE 1.10 Cells in series.

Cellphone batteries, laptop batteries, flashlight batteries, watch batteries, car batteries, calculator batteries, are all common devices in our culture. All are sources of energy, derived in each case from an internal chemical reaction.

The important specifications for a battery are its nominal voltage, its total store of energy, and its internal resistance. In this section, we will assume that the internal resistance of a battery is zero. The voltage measured at the terminals of a single cell is fundamentally related to the chemical reaction releasing the energy. In a flashlight battery, for example, the carbon central rod is approximately 1.5 V positive with respect to the zinc case, as noted in Figure 1.9a. In a circuit diagram, such a single-cell battery is usually represented schematically by the symbol shown in Figure 1.9b. Of course, to obtain a larger voltage, several cells can be connected in series: the positive terminal of the first cell connected to the negative terminal of the second cell, and so forth, as suggested pictorially in Figure 1.10. Multiple-cell batteries are usually represented by the symbol in Figure 1.10b, (with no particular correspondence between the number of lines and the actual number of cells in series).

The second important parameter of a battery is the total amount of energy it can store, often measured in joules. However, if you pick up a camcorder or flashlight battery, you might notice ratings of ampere-hours or watt-hours. Let us reconcile these ratings. When a battery is connected across a resistive load in a circuit, it delivers power. The lightbulb in Figure 1.4 is an example of a resistive load.

The power delivered by the battery is the product of the voltage and the current:

$$P = VI. \quad (1.2)$$

Power is delivered by the battery when the current I flowing out of the positive voltage terminal of the battery is positive. Power is measured in watts. A battery delivers one watt of power when V is one volt and I is one ampere.

Power is the rate of delivery of energy. Thus the amount of energy w delivered by the battery is the time integral of the power.

If a constant amount of power P is delivered over an interval T , the energy w supplied is

$$w = P T. \quad (1.3)$$

The battery delivers one joule of energy if it supplies one watt of power over one second. Thus, joules and watt-seconds are equivalent units. Similarly,

If a battery delivers one watt for an hour, then we say that it has supplied one watt-hour (3600 joules) of energy.

Assuming that the battery terminal voltage is constant at V , because the power delivered by the battery is the product of the voltage and the current, an equivalent indication of the power delivered is the amount of current being supplied. Similarly, the product of current and the length of time the battery will sustain that current is an indication of the energy capacity of the battery. A car battery, for instance, might be rated at 12 V and 50 A-hours. This means that the battery can provide a 1-A current for 50 hours, or a 100-A current for 30 minutes. The amount of energy stored in such a battery is

$$\text{Energy} = 12 \times 50 = 600 \text{ watt-hours} = 600 \times 3600 = 2.16 \times 10^6 \text{ joules.}$$

example 1.1 a lithium-ion battery A lithium-ion (Li-Ion) battery pack for a camcorder is rated as 7.2 V and 5 W-hours. What are its equivalent ratings in mA-hours and joules?

Since a joule (J) is equivalent to a W-second, $5 \text{ W-hours} = 5 \times 3600 = 18000 \text{ J}$.

Since the battery has a voltage of 7.2 V, the battery rating in ampere-hours is $5/7.2 = 0.69$. Equivalently, its rating in mA-hours is 690.

example 1.2 energy comparison Does a Nickel-Cadmium (Ni-Cad) battery pack rated at 6 V and 950 mA-hours store more or less energy than a Li-Ion battery pack rated at 7.2 V and 900 mA-hours?

We can directly compare the two by converting their respective energies into joules. The Ni-Cad battery pack stores $6 \times 950 \times 3600 / 1000 = 20520 \text{ J}$, while the Li-Ion battery pack stores $7.2 \times 900 \times 3600 / 1000 = 23328 \text{ J}$. Thus the Li-Ion battery pack stores more energy.

When a battery is connected across a resistor, as illustrated in Figure 1.4, we saw that the battery delivers energy at some rate. The power was the rate of delivery of energy. Where does this energy go? Energy is dissipated by the resistor, through heat, and sometimes even light and sound if the resistor overheats and explodes! We will discuss resistors and power dissipation in Section 1.5.2.

If one wishes to increase the current capacity of a battery without increasing the voltage at the terminals, individual cells can be connected in parallel, as shown in Figure 1.11. It is important that cells to be connected in parallel be nearly identical in voltage to prevent one cell from destroying another. For example, a 2-V lead-acid cell connected in parallel with a 1.5-V flashlight cell will surely destroy the flashlight cell by driving a huge current through it.

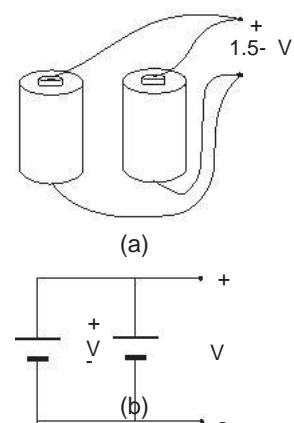


FIGURE 1.11 Cells in parallel.

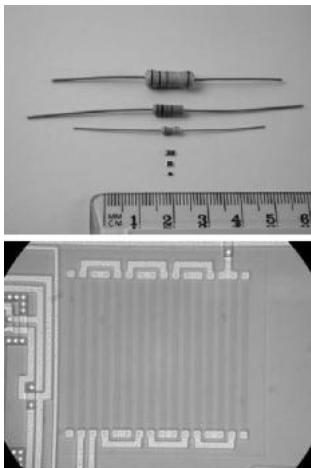


FIGURE 1.12 Discrete resistors (above), and Deposits integrated-circuit resistors (below). The image on the bottom shows a small region of the MAX807L microprocessor supervisory circuit from Maxim Integrated Products, and depicts an array of silicon-chromium thin-film resistors, each with $6\mu\text{m}$ width and $217.5\mu\text{m}$ length, and nominal resistance 50k . (Photograph Courtesy of Maxim Integrated Products.)

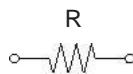


FIGURE 1.13 Symbol for resistor.

The corresponding constraint for cells connected in series is that the nominal current capacity be nearly the same for all cells. The total energy stored in a multicell battery is the same for series, parallel, or series-parallel interconnections.

1.5.2 LINEAR RESISTORS

Resistors come in many forms (see Figure 1.12), ranging from lengths of nichrome wire used inasters and electric stoves and planar layers of polysilicon in highly complex computer chips, to small rods of carbon particles encased in Bakelite commonly found in electronic equipment. The symbol for resistors in common usage is shown in Figure 1.13.

Over some limited range of voltage and current, carbon, wire and polysilicon resistors obey Ohm's law:

$$v = iR \quad (1.4)$$

that is, the voltage measured across the terminals of a resistor is linearly proportional to the current flowing through the resistor. The constant of proportionality is called the resistance. As we show shortly, the resistance of a piece of material is proportional to its length and inversely proportional to its cross-sectional area.

In our example of Figure 1.4b, suppose that the battery is rated at 1.5V . Further assume that the resistance of the bulb is $R=10\Omega$. Assume that the internal resistance of the battery is zero. Then, a current of $i=v/R=150\text{mA}$ will flow through the bulb.

example 1.3 more on resistance In the circuit in Figure 1.4b, suppose that the battery is rated at 1.5V . Suppose we observe through some means a current of 500mA through the resistor. What is the resistance of the resistor?

For a resistor, we know from Equation 1.4 that

$$R = \frac{v}{i}$$

Since the voltage across the resistor is 1.5V and the current through the resistor is 500mA , the resistance of the resistor is 3Ω .

The resistance of a piece of material depends on its geometry. As illustrated in Figure 1.14, assume the resistor has a conducting channel with cross-sectional area a , length l , and resistivity ρ . This channel is terminated at its extremes by two conducting plates that extend to form the two terminals of the resistor. If this cylindrical piece of material satisfies the lumped matter

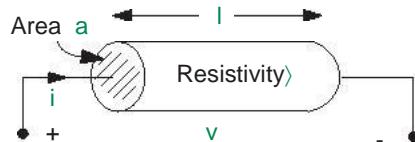


FIGURE 1.14 Acylindrical-wire shapedresistor.

disciplineandobey'sOhm'slaw,wecanwrite¹³

$$R = \rho \frac{l}{a} \quad (1.5)$$

Equation 1.5 shows that the resistance of a piece of material is proportional to its length and inversely proportional to its cross-sectional area.

Similarly, the resistance of a cuboid shaped resistor with length l , width w , and height h is given by

$$R = \rho \frac{l}{wh} \quad (1.6)$$

when the terminals are taken at the pair of surfaces with area wh .

example 1.4 resistance of a cube Determine the resistance of a cube with sides of length 1 cm and resistivity 10 ohm-cms, when a pair of opposite surfaces are chosen as the terminals.

Substituting $\rho = 10\text{-cm}$, $l = 1\text{cm}$, $w = 1\text{cm}$, and $h = 1\text{cm}$ in Equation 1.6, we get

$$R = 10.$$

example 1.5 resistance of a cylinder By what factor is the resistance of a wire with cross-sectional radius r greater than the resistance of a wire with cross-sectional radius $2r$?

A wire is cylindrical in shape. Equation 1.5 relates the resistance of a cylinder to its cross-sectional area. Rewriting Equation 1.5 in terms of the cross-sectional radius r we have

$$R = \rho \pi r^2 \frac{l}{a}$$

From this equation it is clear that the resistance of a wire with radius r is four times greater than that of a wire with cross-sectional radius $2r$.

13. See Appendix A.3 for a derivation.

example 1.6 carbon-core resistors The resistance of small carbon-core resistors can range from 1 to 10^6 . Assuming that the core of these resistors is 1 mm in diameter and 5 mm long, what must be the range of resistivity of the carbon cores?

Given a 1-mm diameter, the cross-sectional area of the core is $A = \pi r^2 = \pi (0.5\text{ mm})^2 \approx 7.9 \times 10^{-7} \text{ m}^2$. Further, its length is $l = 5 \times 10^{-3} \text{ m}$. Thus, $A/l \approx 1.6 \times 10^{-4} \text{ m}$.

Finally, using Equation 1.5, with $1 \leq R \leq 10^6$, it follows that the approximate range of its resistivity is $1.6 \times 10^{-4} \Omega \leq \rho \leq 1.6 \times 10^2 \Omega$.

example 1.7 poly-crystalline silicon resistor

A thin poly-crystalline silicon resistor is 1 μm thick, 10 μm wide, and 100 μm long, where 1 μm is 10^{-6} m . If the resistivity of its poly-crystalline silicon ranges from $10^{-6} \Omega \text{ m}$ to $10^2 \Omega \text{ m}$, what is the range of its resistance?

The cross-sectional area of the resistor is $A = 10^{-11} \text{ m}^2$, and its length is $l = 10^{-4} \text{ m}$. Thus $l/A = 10^7 \text{ m}^{-1}$. Using Equation 1.5, and the given range of resistivity, ρ , the resistance satisfies $10 \leq R \leq 10^9 \Omega$.

example 1.8 resistance of planar materials on a chip

Figure 1.15 shows several pieces of material with varying geometries. Assume all the pieces have the same thickness. In other words, the pieces of material are planar. Let us determine the resistance of these pieces between the pairs of terminals shown. For a given thickness, remember that the resistance of a piece of material in the shape of a cuboid is determined by the ratio of the length to the width of the piece of material (Equation 1.6). Assuming that R_0 is the resistance of a piece of planar material

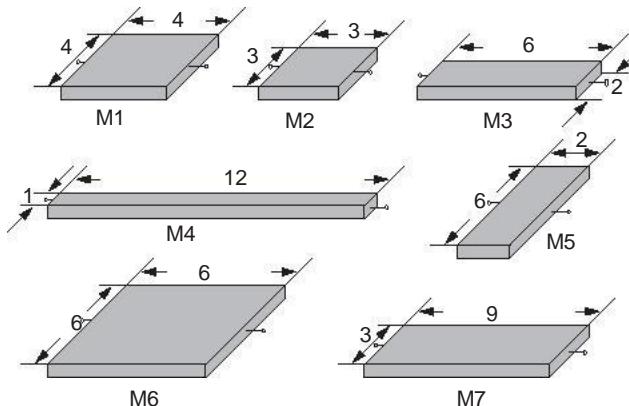


FIGURE 1.15 Resistors of various shapes.

with unit length and width, show that the resistance of a piece of planar material with length L and width W is $(L/W)R_o$.

From Equation 1.6, the resistance of a cuboid shaped material with length L , width W , height H , and resistivity ρ is

$$R = \rho \frac{L}{WH}. \quad (1.7)$$

We are given that the resistance of a piece of the same material with $L=1$ and $W=1$ is R_o . In other words,

$$R_o = \rho H L. \quad (1.8)$$

Substituting $R_o = \rho / H$ in Equation 1.7, we get

$$R = W L R_o. \quad (1.9)$$

Now, assume $R_o = 2k$ for our material. Recall that Ohms are the unit of resistance and are written as Ω . We denote a 1000-value as kilo- Ω . Assuming that the dimensions of the pieces of material shown in Figure 1.15 are in $\mu\text{-m}$, or micrometers, what are their resistances?

First, observe that pieces M1, M2, and M6 must have the same resistance of $2k$ because they are squares (in Equation 1.9, notice that $L/W=1$ for a square).

Second, M3 and M7 must have the same resistance because both have the same ratio $L/W=3$. Therefore, both have a resistance of $3 \times 2 = 6k$. Among them, M 4 has the biggest L/W ratio of 12. Therefore it has the largest resistance of $24k$. M5 has the smallest L/W ratio of $1/3$, and accordingly has the smallest resistance of $2/3k$.

Because all square pieces made out of a given material have the same resistance (provided, of course, the pieces have the same thickness), we often characterize the resistivity of planar material of a given thickness with

$$R_P = R_o, \quad (1.10)$$

where R_o is the resistance of a piece of the same material with unit length and width. Pronounced "Rsquare," R_P is the resistance of a square piece of material.

example 1.9 more on planar resistances

Referring back to Figure 1.15, suppose an error in the material fabrication process results in each dimension (L and W) increasing by a fraction ϵ . By what amount will the resistances of each of the pieces of material change?

Recall that the resistance R of a planar rectangular piece of material is proportional to L/W . If each dimension increases by a fraction e , the new length becomes $L(1+e)$ and the new width becomes $W(1+e)$. Notice that the resistance given by

$$R = \frac{WL}{WLR_0} = \frac{L}{L_0}$$

is unchanged.

example 1.10 ratio of resistances

Referring again to Figure 1.15, suppose the material fabrication process undergoes a “shrink” to decrease each dimension (this time around, increasing the thickness H in addition to L and W) by a fraction α (e.g., $\alpha = 0.8$). Assume further, that the resistivity ρ changes by some other fraction to ρ . Now consider a pair of resistors with resistances R_1 and R_2 , and original dimensions L_1, W_1 and L_2, W_2 respectively, and the same thickness H . By what fraction does the ratio of the resistance values change after the process shrink?

From Equation 1.7, the ratio of the original resistance values is given by

$$\frac{R_1}{R_2} = \frac{\rho L_1/(W_1 H)}{\rho L_2/(W_2 H)} = \frac{L_1 W_2}{L_2 W_1}$$

Let the resistance values after the process shrink be R_1' and R_2' . Since each dimension shrinks by the fraction α , each new dimension will be at most the original value. Thus, for example, the length L_1 will change to αL_1 . Using Equation 1.7, the ratio of the new resistance values is given by

$$\frac{R_1'}{R_2'} = \frac{\rho \alpha L_1 / (\alpha W_1 \alpha H)}{\rho \alpha L_2 / (\alpha W_2 H)} = \frac{L_1 W_2}{L_2 W_1}$$

In other words, the ratio of the resistance values is unchanged by the process shrink.

The ratio property of planar resistance—that is that the ratio of the resistances of rectangular pieces of material with a given thickness and resistivity is independent of the actual values of the length and the width provided the ratio of the length and the width is fixed—enables us to perform process shrinks (for example, from a 0.25-μm process to a 0.18-μm process) without needing to change the chip layout. Process shrinks are performed by scaling the dimensions of the chip and its components by the same factor, thereby resulting in a smaller chip. The chip is designed such that relevant

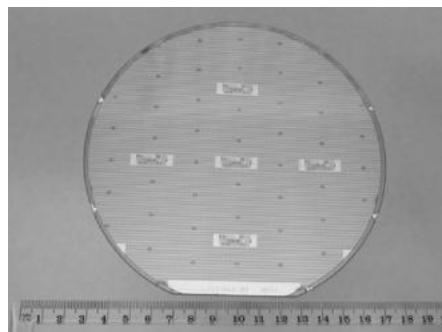


FIGURE 1.16 A silicon wafer.
(Photograph Courtesy of Maxim Integrated Products.)

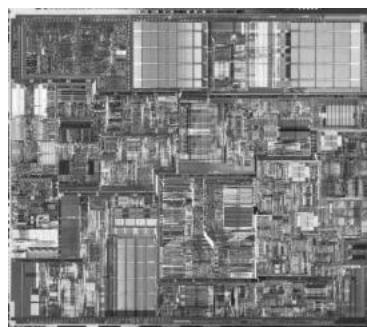


FIGURE 1.17 A chip photo of Intel's 2-GHz Pentium IV processor implemented in 0.18 μm -technology. The chip is roughly 1 cm on a side.
(Photograph courtesy of Intel Corp.)

signal values are derived as a function of resistance ratios,¹⁴ thereby ensuring that the chip manufactured after a process shrink continues to function as before.

VLSI stands for "Very Large Scale Integration." Silicon-based VLSI is the technology behind most of today's computer chips. In this technology, lumped planar elements such as wires, resistors, and a host of other stuff we will soon encounter, are fabricated on the surface of a planar piece of silicon called a wafer (for example, see Figures 1.15 and 1.16). A wafer has roughly the shape and size of a Mexican tortilla or an Indian chapati (see Figure 1.16). The planar elements are connected together using planar wires to form circuits. After fabrication, each wafer is diced into several hundred chips or "dies," typically, each the size of a thumbnail. A Pentium chip, for example, contains hundreds of millions of planar elements (see Figure 1.17). Chips are attached, or bonded, to packages (for example, see Figure 12.3.4), which are in turn mounted on a printed-circuit board along with other discrete components such as resistors and capacitors (for example, see Figure 1.18) and wired together.

14. We will study many such examples in the ensuing sections, including the voltage divider in Section 2.3.4 and the inverter in Section 6.8.

FIGURE 1.18 A printed-circuit board containing several interconnected chip packages and discrete components such as resistors (tiny box-like objects) and capacitors (tall cylindrical objects). (Photograph Courtesy of Anant Agarwal, the Raw Group.)



As better processes become available, VLSI fabrication processes undergo periodic shrinks to reduce the size of chips without needing significant design changes. The Pentium III, for example, initially appeared in the 0.25- μm process, and later in the 0.18- μm process. The Pentium IV chip shown in Figure 1.17 initially appeared in a 0.18- μm process in the year 2000, and later in 0.13- μm and 0.09- μm processes in 2001 and 2004, respectively.

There are two important limiting cases of the linear resistor: open circuits and short circuits. An open circuit is an element through which no current flows, regardless of its terminal voltage. It behaves like a linear resistor in the limit $R \rightarrow \infty$ circuit. It is at the opposite extreme. It is an element across which no voltage can appear regardless of the current through it. It behaves like a linear resistor in the limit $R \rightarrow 0$. Observe that the short circuit element is the same as an ideal wire. Note that neither the open circuit nor the short circuit dissipate power since the product of their terminal variables (v and i) is identically zero.

Most often, resistances are thought of as time-invariant parameters. But if the temperature of a resistor changes, then so does its resistance. Thus, a linear resistor can be a time-varying element.

The linear resistor is but one example of a larger class of resistive elements. In particular, resistors need not be linear; they can be nonlinear as well. In general, a two-terminal resistor is any two-terminal element that has an algebraic relation between its instantaneous terminal current and its instantaneous terminal voltage. Such a resistor could be linear or nonlinear, time-invariant or time-varying. For example, elements characterized by the following element relationships are all general resistors:

$$\text{Linear resistor: } v(t) = i(t)R(t)$$

$$\text{Linear, time-invariant resistor: } v(t) = i(t)R$$

$$\text{Nonlinear resistor: } v(t) = K_i(t)^3$$

However, as introduced in Chapter 9, elements characterized by these relationships are not general resistors:

$$v(t) = L \frac{di(t)}{dt}$$

$$v(t) = C_1 \int_{-\infty}^t i(t) dt$$

What is important about the general resistor is that its terminal current and voltage depend only on the instantaneous values of each other. For our convenience, however, an unqualified reference to a resistor in this book means a linear, time-invariant resistor.

1.5.3 ASSOCIATED VARIABLES CONVENTION

Equation 1.4 implies a specific relation between referenced directions chosen for voltage and current. This relation is shown explicitly in Figure 1.19: the arrow that defines the positive flow of current (flow of positive charge) is directed in at the resistor terminal assigned to be positive in voltage. This convention, referred to as associated variables, is generalized to an arbitrary element in Figure 1.20 and will be followed whenever possible in this text. The variables v and i are called the terminal variables for the element. Note that the values of each of these variables may be positive or negative depending on the actual direction of current flow or the actual polarity of the voltage.

Associated Variables Convention Define current to flow in at the device terminal assigned to be positive in voltage.

When the voltage v and current i for an element are defined under the associated variables convention, the power into the element is positive when both v and i are positive. In other words, energy is pumped into an element when a positive current i is directed into the voltage terminal marked positive. Depending on the type of element, the energy is either dissipated or stored. Conversely, power is supplied by an element when a positive current i is directed out of the voltage terminal marked positive. When the terminal variables for a resistor are defined according to associated variables, the power dissipated in the resistor is a positive quantity, an intuitively satisfying result.

While Figure 1.20 is quite simple, it nonetheless makes several important points. First, the two terminals of the element in Figure 1.20 form a single port through which the element is addressed. Second, the current circulates through that port. That is, the current that enters one terminal is instantaneously equal to the current that exits the other terminal. Thus, according to the lumped matter discipline, net charge cannot accumulate within the element. Third, the voltage of the element is defined across the port. Thus, the element is assumed to respond only to the difference of the electrical potentials at its two terminals,

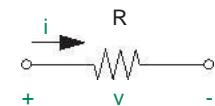


FIGURE 1.19 Definition of terminal variables v and i for the resistor.

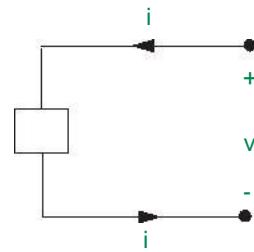


FIGURE 1.20 Definition of the terminal variables v and i for a two-terminal element under the associated variables convention.

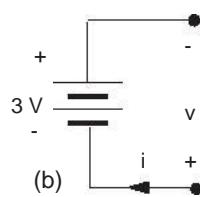
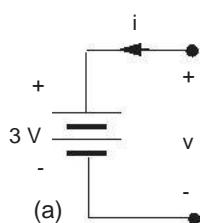


FIGURE 1.21 Terminal variable assignments for a battery.

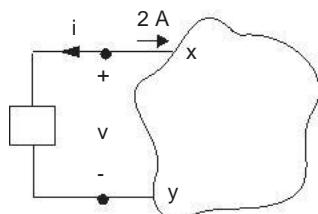


FIGURE 1.22 Terminal variable assignments for a two-terminal element.

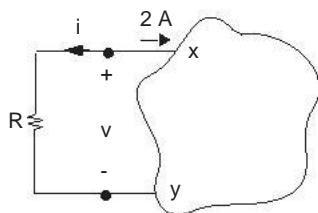


FIGURE 1.23 Terminal variable assignments for a resistor.

and not to the absolute electric potential at either terminal. Fourth, the current is defined to circulate positively through the port by entering the positive voltage terminal and exiting the negative voltage terminal. Which terminal is chosen as the positive voltage terminal is arbitrary, but the relation defined between the current and voltage is not. Lastly, for brevity, the current that exits the negative voltage terminal is usually never labeled, but it is always understood to be equal to the current that enters the positive voltage terminal.

example 1.11 terminal variables versus element properties

Figures 1.21a and b show two possible legal definitions for terminal variables for a 3 V battery. What is the value of terminal variable v in each case?

For Figure 1.21a, we can see that terminal variable $v = 3V$. For Figure 1.21b, however, $v = -3V$.

This example highlights the distinction between a terminal variable and an element property. The battery voltage of 3 V is an element property, while v is a terminal variable that we have defined. Element properties are usually written inside the element symbol, or if that is inconvenient, they are written next to the element (e.g., the battery voltage). Terminal polarities and terminal variables are written closest to the terminals.

example 1.12 fun with terminal variables

Figure

1.22 shows some two-terminal elements connected to an arbitrary circuit at the points x and y . The element terminal variables v and i are defined according to the associated variables convention. Suppose that a current of 2 A flows into the circuit terminal marked x . What is the value of terminal variable v ?

Since the chosen direction of the terminal variable i is opposite to that of the 2 A current, $i = -2A$.

Now suppose that the two-terminal element is a resistor (see Figure 1.23) with resistance $R = 10\text{ Ohms}$. Determine the value of v .

We know that under the associated variables convention the terminal variables for a resistor are related as

$$v = iR$$

Given that $R = 10$ and $i = -2A$,

$$v = (-2)10 = -20V$$

Next, suppose that the two-terminal element is a 3 V battery with the polarity shown in Figure 1.24a. Determine the values of terminal variables v and i .

As determined earlier, $i = -2A$. For the polarity of the battery shown in Figure 1.24a, $v = 3V$.

Now, suppose the 3V battery is connected with the polarity shown in Figure 1.24b. Determine the values of v and i .

As before, $i = -2A$. With the reversed battery connections shown in Figure 1.24b, $v = -3V$.

Under the associated variables convention, the instantaneous power supplied into an element is given by

$$p = vi \quad (1.11)$$

with units of watts (W).

Note that both v and i , and therefore the instantaneous power p , can be functions of time. For a resistor, $p = vi$ represents the instantaneous power dissipated by the resistor.

Correspondingly, the amount of energy (in units of joules) supplied to an element during an interval of time between t_1 and t_2 under the associated variables convention is given by

$$w = \int_{t_1}^{t_2} vi dt. \quad (1.12)$$

for a Fortwo-

terminal resistor, by element noting (Equation that $v = iR$) from can Equation bee equivalent 1.4, the written power relation as of

$$p = vR. \quad (1.13)$$

example 1.13 power into a resistor Determine the power for the resistor in Figure 1.23. Confirm mathematically that the power is indeed supplied into the resistor.

We know that $i = -2A$ and $v = -20V$. Therefore, the power is given by

$$p = vi = (-20V)(-2A) = 40W$$

By your associated variables convention, the product $p = vi$ yields the power supplied into the element. Thus, we can confirm that 40W of power is being supplied into the resistor. From the properties of a resistor, we also know that this power is dissipated in the form of heat.

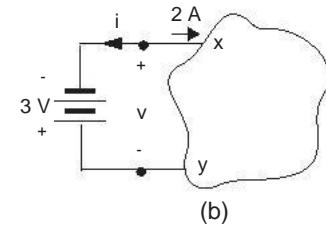
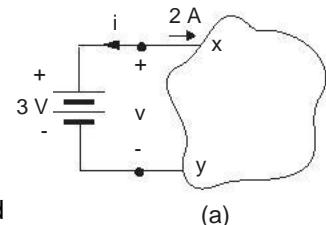


FIGURE 1.24 The two-terminal element is a battery.

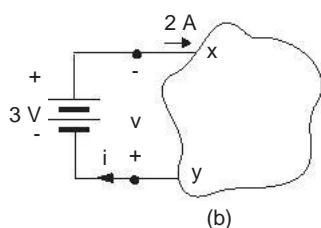
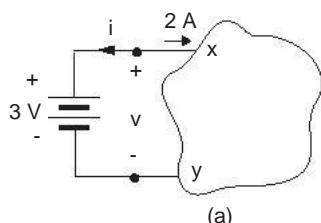


FIGURE 1.25 Alternative assignments of terminal variables.

example 1.14 power supplied by a battery Determine the power for the battery using the two assignments of terminal variables in Figures 1.25a and 1.25b.

For the assignment of terminal variables in Figure 1.25a, $i = 2\text{ A}$ and $v = 3\text{ V}$. Thus, by associated variables, power into the battery is given by

$$p = vi = (3\text{ V})(2\text{ A}) = +6\text{ W}$$

Since the power into the battery is negative, the power supplied by the battery is positive. Thus, in the circuit of Figure 1.25a, the battery is delivering power.

Next, let us analyze the same circuit with the assignment of terminal variables in Figure 1.25b. For this assignment, $i = -2\text{ A}$ and $v = -3\text{ V}$. Thus, by associated variables, power into the battery is given by

$$p = vi = (-3\text{ V})(-2\text{ A}) = +6\text{ W}$$

In other words, the battery is delivering 6 watts of power. Since the circuit is the same, it is not surprising that our result has not changed when the terminal variable assignments are reversed.

example 1.15 power supplied versus power absorbed by a battery In simple circuits, for example, circuits containing a single battery, we do not have to undergo the rigor of associated variables to determine whether power is being absorbed or supplied by an element. Let us work out such an example. In our lightbulb circuit of Figure 1.4b, suppose that the battery is rated at 1.5 V and 1500 J . Assume that the internal resistance of the battery is zero. Further assume that the resistance of the bulb is $R = 10\Omega$. What is the power dissipated in the resistor?

The power dissipated in the resistor is given by

$$p = VI = \frac{V^2}{R} = \frac{(1.5\text{ V})^2}{10\Omega} = 0.225\text{ W}$$

Since the entire circuit comprises a battery and a resistor, we can state without a lot of analysis that the resistor dissipates power and the battery supplies it. How much power does the battery provide when it is connected to the 10Ω -resistor? Suppose the battery supplies a current I . We can quickly compute the value of this current as:

$$I = \frac{V}{R} = \frac{1.5\text{ V}}{10\Omega} = 0.15\text{ A}$$

Thus the power delivered by the battery is given by

$$P = VI = 1.5 \times 0.15 = 0.225 \text{ W}$$

Not surprisingly, the power delivered by the battery is the same as the power dissipated in the resistor. Note that since the circuit current has been defined to be directed out of the positive battery terminal in Figure 1.4b, and since the current is positive, the battery is supplying power.

How long will our battery last when it is connected to the 10- resistor? Since the battery is supplying 0.225 W of power, and since a watt represents energy dissipation at the rate of one joule per second, the battery will last $1500 / 0.225 = 6667 \text{ s}$.

example 1.16 power rating of a resistor In a circuit such as that shown in Figure 1.4b, the battery is rated at 7.2 V and 10000 J. Assume that the internal resistance of the battery is zero. Further assume that the resistance in the circuit is $R = 1 \text{ k}\Omega$. You are given that the resistor can dissipate a maximum of 0.5 W of power. (In other words, the resistor will overheat if the power dissipation is greater than 0.5 W.) Determine the current through the resistor. Further, determine whether the power dissipation in the resistor exceeds its maximum rating.

The current through the resistor is given by

$$I = \frac{V}{R} = \frac{7.2}{1000} = 7.2 \text{ mA}$$

The power dissipation in the resistor is given by

$$P = I^2 R = (7.2 \times 10^{-3})^2 \times 10^3 = 0.052 \text{ W}$$

Clearly, the power dissipation in the resistor is well within its capacity.

1.6 IDEAL TWO-TERMINAL ELEMENTS

As we saw previously, the process of discretization can be viewed as a way of modeling physical systems. For example, the resistor is a lumped model for a lightbulb. Modeling physical systems is a major motivation for studying electronic circuits. In our lightbulb circuit example, we used lumped electrical elements to model electrical components such as bulbs and batteries. In general, modeling physical systems involves representing real-world physical processes, whether they are electrical, chemical, or mechanical, in terms of a set of ideal electric elements. This section introduces a set of ideal two-terminal elements including voltage and current sources, and ideal wires and resistors, which form our primitives in the vocabulary of circuits.

The same set of ideal two-terminal elements serve to build either information processing or energy processing systems as well. Information and energy processing include the communication, storage, or transformation of information or energy, and is a second major motivation for studying electronic circuits. Whether we are interested in modeling systems or in information and energy processing, it is essential to be able to represent five basic processes in terms of our lumped circuit abstraction.

1. Sources of energy or information
2. Flow of energy or information in a system
3. Loss of energy or information in a system
4. Control of energy flow or information flow by some external force
5. Storage of energy or information

We will discuss ideal two-terminal elements that represent the first three of these in this section, deferring control and storage until Chapters 6 and 9, respectively.

1.6.1 IDEAL VOLTAGE SOURCES, WIRES, AND RESISTORS

Familiar primary sources of energy in our daily lives are sunlight, oil, and coal. Secondary sources would be power plants, gasoline engines, home-heating furnaces, or flashlight batteries. In heating systems, energy flows through air ducts or heating pipes; in electrical systems the flow is through copper wires.¹⁵ Similarly, information sources include speech, books, compact discs, videos, and the web (some of it, anyway!). Information flow in speech systems is through media such as air and water; in electronics systems, such as computers or phones, the flow relies on conducting wires. Sensors such as microphones, magnetic tape heads, and optical scanners convert information from various forms into an electrical representation. None of these elements is ideal, so our first task is to invent ideal energy or information sources and ideal conductors for energy or information flow.

Conceptually, it is relatively easy to extrapolate from known properties of a battery to postulate an ideal voltage source as a device that maintains a constant voltage at its terminals regardless of the amount of current drawn from those terminals. To distinguish such an ideal element from a battery¹⁶ (see Figure 1.26a), we denote a voltage source by a single circle with polarity

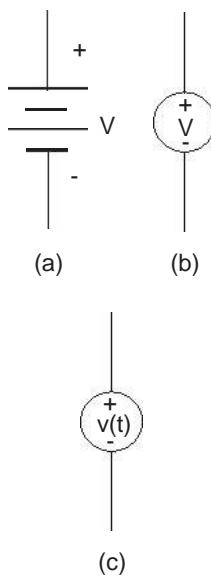


FIGURE 1.26 Circuit symbol for a voltage source: (a) battery; (b) voltage source; (c) voltage source.

15. Or, more accurately, in the fields between the wires.

16. In general, a physical battery has some internal resistance, which we ignore in our previous examples. A more precise relationship between the ideal voltage source and the battery is developed in Section 1.7.

markings inside it, as in Figure 1.26b. If the voltage source supplies a voltage V , then we also include the V symbol inside the circle (or just outside the circle if there is not enough room to write the symbol inside). In the same manner, we might also represent an information source, such as a microphone or a sensor, as a voltage source providing a time-varying voltage $v(t)$ at its output (Figure 1.26c). We can assume that the voltage $v(t)$ depends solely on the microphone signal and is independent of the amount of current drawn from the terminals. (Note that V and $v(t)$ in Figure 1.26 are element values and not terminal variables.)

We will see two types of voltage sources: independent and dependent. An independent voltage source supplies a voltage independent of the rest of the circuit. Accordingly, independent sources are meant through which inputs can be made to a circuit. Powers supplies, signal generators, and microphones are examples of independent voltage sources. The circle symbol in Figure 1.26b represents an independent voltage source. In contrast to an independent voltage source, a dependent voltage source supplies a voltage as commanded by a signal from within the circuit of which the source is a part. Dependent sources are most commonly used to model elements having more than two terminals. They are represented with a diamond symbol; we shall see examples of these in future chapters.

In a manner similar to our invention of the ideal voltage source, we postulate an ideal conductor to be one in which any amount of current can flow without loss of voltage or power. The symbol for an ideal conductor is shown in Figure 1.27a. Notice that the symbol is just a line. The ideal conductor is no different from the ideal wire we saw earlier. Ideal conductors can be used to represent a channel for fluid flow in hydrodynamic systems.

Any physical length of wire will have some nonzero resistance. The resistance dissipates energy and represents a loss of energy from the system. If this resistance is important in a particular application, then we can model the wire as an ideal conductor in series with a resistor, as suggested in Figure 1.27b. To be consistent, we now state that the resistor symbol introduced in Figure 1.19 represents an ideal linear resistor, which by definition obeys Ohm's law

$$v = iR \quad (1.15)$$

for all values of voltage and current. Resistors can be used to model processes such as friction that result in energy loss in a system. Note that because this element law is symmetric, it is unchanged if the polarities of the current and voltage definitions are reversed. Sometimes it is convenient to work with reciprocal resistance, namely the conductance G having the units of Siemens (S). In this case,

$$G = R^{-1} \quad (1.16)$$

and

$$i = Gv. \quad (1.17)$$

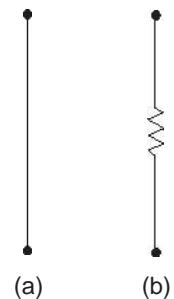


FIGURE 1.27 Circuits symbol for an ideal conductor: (a) perfect conductor; (b) wire with nonzero resistance.

Most often, resistances and conductances are thought of as time-invariant parameters. But if the temperature of a resistor changes, then so too can its resistance and conductance. Thus, a linear resistor can be a time-varying element.

1.6.2 ELEMENT LAWS

From the viewpoint of circuit analysis, the most important characteristic of a two-terminal element is the relation between the voltage across and the current through its terminals, or the v - i relationship for short. This relation, called the element law, represents the lumped-parameter summary of the electronic behavior of the element. For example, as seen in Equation 1.15,

$$v = iR$$

is the element law for the resistor. The element law is also referred to as the constituent relation, or the element relation. In order to standardize the manner in which element laws are expressed, the current and voltage for all two-terminal elements are defined according to the associated variables conventions shown in Figure 1.19. Figure 1.28 shows a plot of the v - i relationship for a resistor when v and i are defined according to the associated variables convention.

The constituent relation for the independent voltage source in Figure 1.26b supplying a voltage V is given by

$$v = V \quad (1.18)$$

when its terminal variables are defined as in Figure 1.29a. A plot of the v - i relationship is shown in Figure 1.29b. Observe the clear distinction between the element parameter V and its terminal variables v and i .

Similarly, the element law for the ideal wire (or a short circuit) is given by

$$v = 0. \quad (1.19)$$

Figure 1.30a shows the assignment of terminal variables and Figure 1.30b plots the v - i relationship.

Finally, the element law for an open circuit is given by

$$i = 0. \quad (1.20)$$

Figure 1.31a shows the assignment of terminal variables and Figure 1.31b plots the v - i relationship.

Comparing the v - i relationship for the resistor in Figure 1.28 to those for a short circuit in Figure 1.30a and an open circuit in Figure 1.31, it is evident that the short circuit and open circuit are limiting cases for a resistor. The resistor approaches the short circuit case as its resistance approaches zero. The resistor approaches the open circuit case as its resistance approaches infinity.

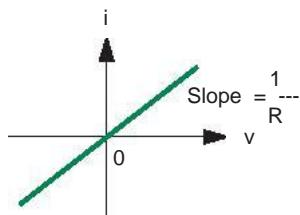


FIGURE 1.28 Plot of the v - i relationship for a resistor.

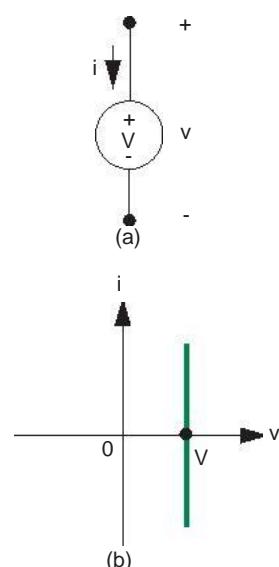


FIGURE 1.29 (a) Independent voltage source with assigned terminal variables, (b) v - i relationship for the voltage source.

example 1.17 more on terminal variables versus element properties Figure 1.32 shows a 5-V voltage source connected to an arbitrary circuit at the points x and y. Its terminal variables v and i are defined according to the associated variables convention as indicated in the figure. Suppose that a current of 2 A flows into the circuit terminal marked x. What are the values of v and i?

For the assignment of terminal variables shown in Figure 1.32, $i = 2 \text{ A}$ and $v = -5\text{V}$.

Notice the distinction between terminal variables and element properties in this example. The source voltage of 5 V is an element property, while v is a terminal variable that we have defined. Similarly, the polarity markings inside the circle are a property of the source, while the polarity markings outside the circle represent the source relative to the terminal variable v . When possible, we attempt to write the element values inside the element symbol, while the terminal variables are written outside.

example 1.18 charting $v - i$ relationships An experimental way of charting the $v - i$ relationship for a two-terminal element is to connect an oscilloscope and an oscillator (or a signal generator set to produce an oscillatory output) in a curve plotter configuration as suggested in Figure 1.33. The oscillator produces a voltage given by

$$v_i = V \cos(\omega t).$$

The basic concept is to use the oscillator to drive current into some arbitrary two-terminal device, and measure the resulting voltage v_D and current i_D . Notice that the terminal variables for the two-terminal device, v_D and i_D , are defined according to the associated variables convention. As can be seen from the circuit, the horizontal deflection will be proportional to v_D , and the vertical deflection will be proportional to v_R , and hence to i_D , assuming resistor R obeys Ohm's law, and the horizontal and vertical amplifier inputs to the oscilloscope draw negligible current.

1.6.3 THE CURRENT SOURCE—ANOTHER IDEAL TWO-TERMINAL ELEMENT

In some fields of engineering, there are two obvious sources of power that appear to have dual properties. Think, for example, of air pumps. For an ordinary tire pump, the higher the air pressure, the harder the person at the pump handle has to work. But with a household vacuum cleaner, also an air pump of sorts, you can hear the motor actually speed up if the airflow out of the machine is blocked, and a measurement of motor current would confirm that the power to the motor goes down under these conditions.

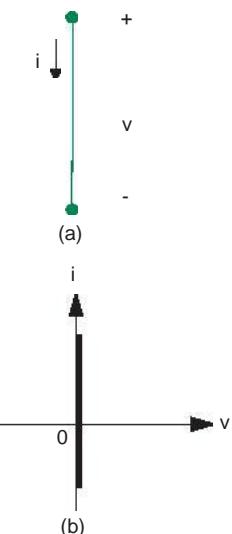


FIGURE 1.30 (a) Ideal wire with terminal variables, (b) v - i relationship for the wire.

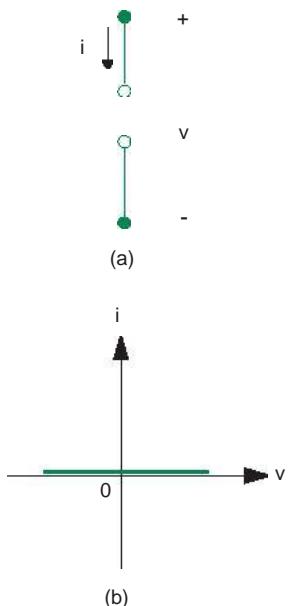


FIGURE 1.31 (a) An open circuit element with terminal variables, (b) v - i relationship for the open circuit.

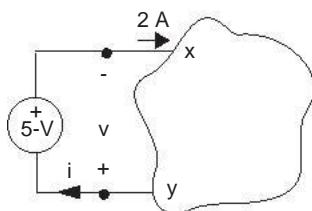


FIGURE 1.32 Terminal variables versus element properties.

It seems reasonable, then, to look for an electrical source that has characteristics that are the dual of those of the battery, in that the roles of current and voltage are interchanged. From the point of view of v - i characteristics, this is a simple task. The ideal voltage source appears as a vertical line in v - i space, so this other source, which we call an ideal current source, should appear as a horizontal line, as in Figure 1.34. Such a source maintains its output current at some constant value regardless of what voltage appears across the terminals.

The element law for a current source supplying a current is given by

$$i = I. \quad (1.21)$$

If the source were left with nothing connected across its terminals, then, in theory at least, the terminal voltage must rise to infinity because the constant current flowing through an infinite resistance gives infinite voltage. Recall the analogous problem with the ideal voltage source: If a short circuit is applied, the terminal current must become infinite.

It is difficult at first to have an intuitive grasp of the current source, principally because there is no familiar device available at the electronic parts counter that has these properties. However, one can still find special devices that deliver constant current to the arc lamps to illuminate the streets of Old Montreal, and we will show later that MOSFETs and Op Amps make excellent current sources. But these are not as familiar as the flashlight battery.

example 1.19 current source power

Determine the

power for the 3-A current source in Figure 1.35 if measurements show that $v = 5V$.

For the assignment of terminal variables in Figure 1.35, $i = -3A$. Further, we are given that $v = 5V$. Power into the current source is given by

$$P = vi = (5V)(-3A) = -15W.$$

Since the power into the current source is negative, we determine that power is being supplied by the current source.

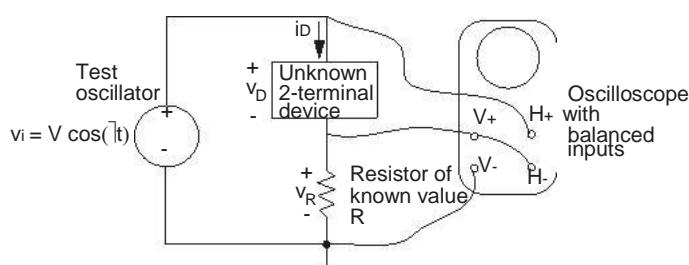


FIGURE 1.33 Charting on an oscilloscope the v - i relationship for a two-terminal element.

Before proceeding further, it is important to distinguish between the model of a two-terminal element and the element itself. The models, or element laws, presented in this section are idealized. They describe a simplified behavior of the real elements (a voltage source for a battery, for instance). From this point forward, we will focus on circuits comprising only ideal elements, and make only occasional reference to reality. Nonetheless, it is important to realize in practice that the result of a circuit analysis is only as good as the models on which the analysis is based. Part of any discrepancy between theory and experiment may be a result of the fact that the elements do not really behave as the element laws predict.

The v - i relation is useful to describe other systems as well, not just primitive two-terminal elements such as sources and resistors. When creating circuit models for these systems, it is often the case that an electronic circuit can be abstracted as a black box accessible through a few terminals. As with any abstraction, the details of behavior at the interfaces (terminals, in our case) are more important than the details of behavior internal to the black box. That is, what happens at the terminals is more important than how it happens inside the black box. Furthermore, it is often the case that the terminals can be paired into ports in a natural way following the function of the circuit. For example, a complex amplifier or filter is often described by the relation between an input signal presented to the amplifier or filter at one pair of terminals or port, and an output signal presented by the amplifier or filter at a second port. In this case, the terminal pairs or ports take on special significance, and the voltage across the port and the current through the port become the port variables in terms of which the electronic circuit behavior is described.

In principle, an electronic circuit can have one or more reports, although in practice it is common to define only a few ports to simplify matters. For example, an amplifier may be described in terms of its input port, its output port, and one or more reports for connection to power supplies. Even simple network elements such as sources, resistors, capacitors, and inductors can be thought of as one-port devices. Voltages are redefined across the ports and currents through the ports as illustrated in Figure 1.36. Observe that the assignment of referenced directions related to v and i follows the associated variables convention discussed in Section 1.5.2.

The notion of a port is much more general than its use in electronic circuit analysis would indicate. Many physical systems, such as mechanical, fluid, or thermal systems can be characterized by their behavior at a few ports. Furthermore, as depicted in Table 1.1 they have through-hand-across parameters analogous to currents and voltages. Circuit models for these systems would use voltages and currents to model the corresponding through-and-across variables in those systems.

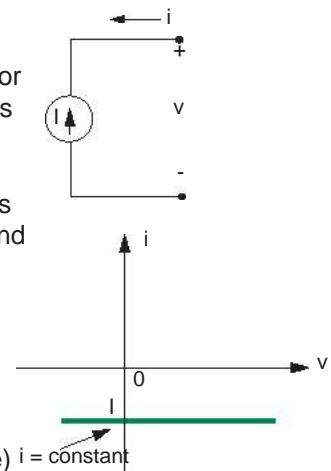


FIGURE 1.34 v - i plot for current source.

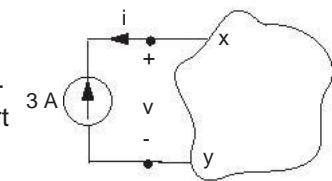


FIGURE 1.35 Power for the current source.

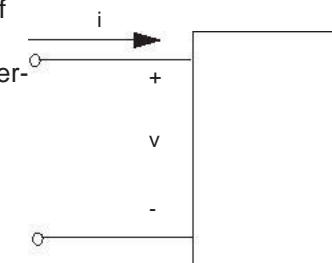


FIGURE 1.36 Definition of the voltage and current for a port.

TABLE 1.1 Through and across variables in physical and economic systems.

Current	Voltage
Force	Motion
Flow	Pressure
Heat Flux	Temperature
Consumption	Wealth

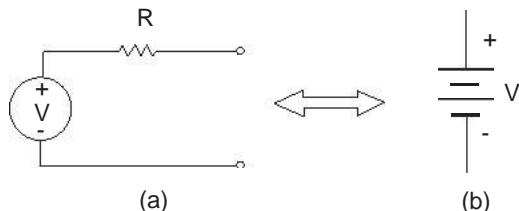
1.7 MODELING PHYSICAL ELEMENTS

Thus far, we have invented four ideal, primitive elements and studied their $v-i$ characteristics. These ideal elements included the independent voltage source, the independent current source, the linear resistor, and the perfect conductor. Let us now return to building models for some of the physical elements we have seen thus far in terms of the four ideal elements.

Indeed, Figure 1.27b is one example of a model. We have modeled a physical device, namely, a length of copper wire, by a pair of ideal two-terminal elements: a perfect conductor and a linear resistance. Obviously this model is not exact. For example, if 1000 A of current flowed through a piece of 14-gauge copper wire (standard house wire designed to carry 15 A), the wire would become hot, glow brightly, and probably melt, thereby converting itself from a resistor with a very small resistance, for example, 0.001, to an infinite resistor. Our model, consisting of an ideal conductor in series with an ideal 0.001-resistor, shows no such behavior: With 1000 A flowing, a one-volt drop would develop across the resistor, and one thousand watts of power would be dissipated, presumably in heat, as long as the current flowed. No smoke, no burnout.

In a similar way we can devise a model for a battery out of our ideal elements. When a flashlight bulb is connected to a new nominally 6-V battery, the voltage at the terminals of the battery (usually called the terminal voltage) drops from 6.2 V to perhaps 6.1 V. This drop results from the internal resistance of the battery. To represent this effect, we model the battery as an ideal voltage source in series with some small resistor R as shown in Figure 1.37a. The drop in

FIGURE 1.37 One model for a battery.



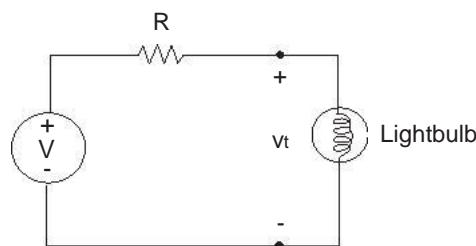


FIGURE 1.38 Battery model and lightbulb.

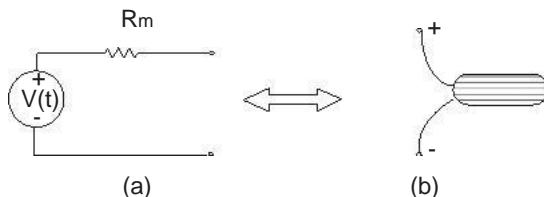


FIGURE 1.39 A microphone model.

terminal voltage when the bulb is initially connected will be properly represented in the circuit model of Figure 1.38 if the value of R is appropriately chosen. However, the model is still not exact. For example, if a lightbulb is connected to a battery for sometime, the battery voltage will slowly drop as the energy is drained from the battery. The model battery will not “rundown,” but will continue to light the bulb indefinitely.

A similar model might apply for a microphone. When an information processing system such as an amplifier is connected to the microphone, its output might drop from a 1-mV peak-to-peak signal to a 0.5-mV peak-to-peak signal due to the internal resistance of the microphone. As with the battery, we can model the microphone as a voltage source in series with a resistance R_m as depicted in Figure 1.39. Although the output voltage of the microphone will not rundown over time, its model is not exact for other reasons. For example, the voltage drop in the signal might be related to the signal frequency.

It is obvious that these “defects” in the models could be corrected by making the models more complicated. But the considerable increase in complexity might not be justified by the improvement in model accuracy. Unfortunately, it is not always obvious in a given problem how to find a reasonable balance between simplicity and accuracy. In this text we will always strive for simplicity on the following basis: Computer solutions for any of the problems we discuss are always available, and these can be structured to have great accuracy. So it makes sense in modeling with circuit elements, as opposed to computer modeling, to strive for insight rather than accuracy, for simplicity rather than complexity.

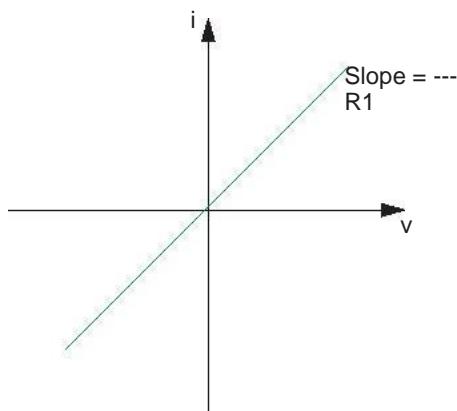


FIGURE 1.40 i - v plot for a resistor.

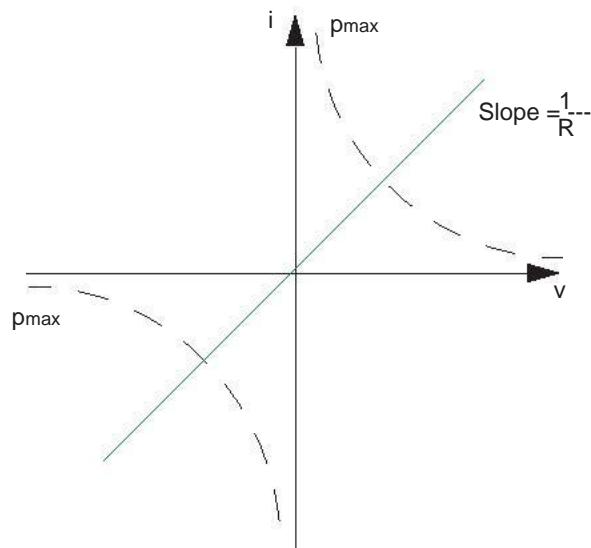
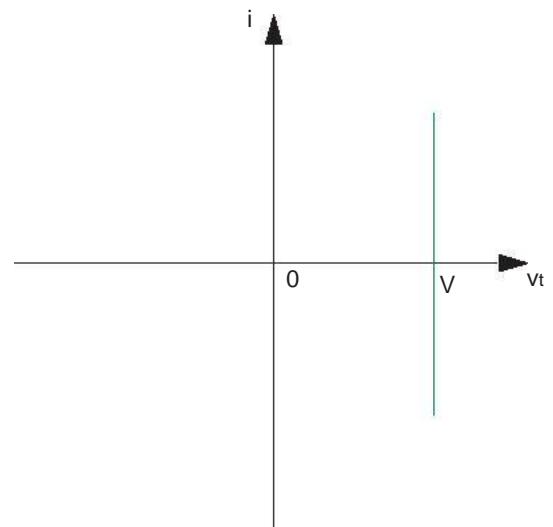
It is appropriate at this point to check experimentally the validity of the models developed here by plotting their v – i characteristics. The v – i characteristics can be plotted using the setup shown in Figure 1.33. First, use a 100-1/10-W resistor as the “unknown” two-terminal device. If the oscillator voltage is a few volts, a straight line passing through the origin with slope $1/R$ will appear on the screen (see Figure 1.40), showing that Ohm’s law applies. However, if the voltage is increased so that v is 5 or 10 V, then the 1/10-W resistor will heat up, and its value will change. If the oscillator is set to a very low frequency, say 1 Hz, the resistor heats up and cools down in the source of each cycle, so the trace is decidedly nonlinear. If the oscillator is in the mid-audiorange, say 500 Hz, thermal inertia prevents the resistor from changing temperature rapidly, so some average temperature is reached. Thus the line will remain straight, but its slope will change as a function of the amplitude of the applied signal.

Resistor self-heating, with the associated change in value, is obviously undesirable in most circuit applications. For this reason manufacturers provide power ratings for resistors, to indicate maximum power dissipation (p_{max}) without significant value change or burnout. The power dissipated in a resistor is

$$p = vi, \quad (1.22)$$

which is the hyperbola in v – i space, as indicated in Figure 1.41. Our ideal-resistor model – ohmic with constant value – matches the actual resistor behavior only in the region between the hyperboli.

The plot on the oscilloscope face will also deviate from a straight line if the oscillator frequency is made high enough. Under this condition, capacitive and inductive effects in the circuit will generate an elliptical pattern. These will be discussed in later chapters.

FIGURE 1.41 Power constraint for a resistor in the i - v plane.FIGURE 1.42 i - v characteristic of a battery at low current levels.

Now plot the i v characteristic of a battery. At low current levels, the curve appears as a vertical line in i - v space (see Figure 1.42). But if the oscillator amplitude is increased so that substantial currents are flowing, and we make an appropriate change in scope vertical sensitivity, the line remains straight, but now has a definite tip, as suggested by Figure 1.43a, indicating a nonzero series resistance. If the battery terminal voltage and current are defined as in

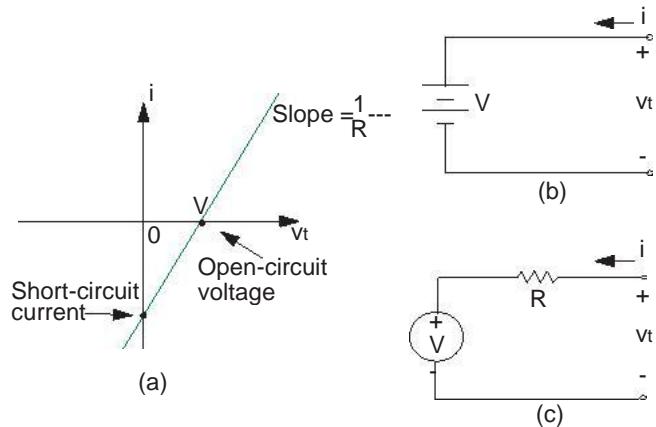


FIGURE 1.43 Battery characteristic, larger currents scale.

Figure 1.43b, then from the model in Figure 1.43c, an appropriate expression for the terminal voltage is¹⁷

$$v_t = V + iR \quad (1.23)$$

Note that because of our choice of variables, in the first quadrant current is flowing into the positive terminal, that is, the battery is being charged, hence the terminal voltage is actually larger than the nominal voltage. The fact that the plot is almost a straight line validates our assumption that the battery can be modeled as a voltage source in series with a linear resistor. Note further that graphs such as Figure 1.43a can be characterized by only two numbers, a slope and an intercept. The slope is $1/R$ where R is the series resistance in the model. The intercept can be specified either in terms of a voltage or a current. If we choose a voltage, then because the intercept is by definition at zero current, it is called the open-circuit voltage. If the intercept is specified in terms of current, it is called the short-circuit current, because by definition the voltage is zero at that point. These terms reappear in Chapter 3 from a very different perspective: Thevenin's Theorem.

This section described how we model physical elements such as batteries and wires in terms of ideal two-terminal elements such as independent voltage sources, resistors, and ideal wires. Our ideal circuit elements such as independent voltage sources and resistors also serve as models for physical entities such as water reservoirs and friction in water tubes, respectively. In the circuit model for a physical system, water pressure is naturally represented using a voltage, and water flow using a current. Water pressure and water flow, or the corresponding voltage and current, are fundamental quantities. In such systems, we will also be concerned with the amount of energy stored in the system, and the rate at which energy is being dissipated.

1.8 SIGNAL REPRESENTATION

The previous sections discussed how lumped circuit elements could serve as models for various physical systems or be used to process information. This section draws the correspondence between variables in physical systems and those in the electrical circuit model. It also discusses how electrical systems represent information and energy.

As discussed earlier, one of the motivations for building electronic circuits is to process information or energy. Processing includes communication, storage, and computation. Stereo amplifiers, computers, and radios are examples of commonplace electronic systems for processing information. Power supplies

17. For now, we simply state the equation, and postpone the derivation to Chapter 2 (see the example related to Figure 2.61) after we have mastered a few basic circuit analysis techniques.

and our familiar lightbulb circuit are examples of electronic circuits that process energy.

In both cases, the physical quantity of interest, either the information or the energy, is represented in the circuit by an electrical signal, namely a current or a voltage, and circuit networks are used to process these signals. Thus, the manner in which a circuit fulfills its purpose is effectively the manner in which it treats the signals that are at its terminal currents and voltages.

1.8.1 ANALOG SIGNALS

Signals in the physical world are most commonly analog, that is, spanning a continuum of values. Sound pressure is such a signal. The electromagnetic signal picked up by a mobile phone antenna is another example of an analog signal. Not surprisingly, most circuits that interact with the physical world must be able to process analog signals.

Figure 1.44 shows several examples of analog signals. Figure 1.44b shows a DC current signal, while the remainder are various forms of voltage signals.

Figure 1.44a shows a sinusoidal signal with frequency 1 MHz and phase offset (or phase shift) $\pi/4$ rad. The same frequency can also be expressed as 10⁶ Hz, or $2\pi \times 10^6$ rad/s, and the phase offset as 45 degrees. The reciprocal of the frequency gives the period of oscillation or the cycle time, which is 1 μ s for our sinusoid. Our sinusoid has an average value of zero. This signal can be described as a sinusoid with an amplitude (or magnitude, or maximum value) of 10 V, or equivalently as a sinusoid with a peak-to-peak swing of 20 V.

Sinusoids are an important class of signals that we will encounter frequently in this book. In general, a sinusoidal signal v can be expressed as

$$v = A \sin(\omega t + \varphi)$$

where A is the amplitude, ω is the frequency in radians per second, t is the time, and φ is the phase offset in radians.

Figures 1.44c and d show square wave signals. The square wave in Figure 1.44c has a peak-to-peak value of 10 V and an average value (or DC offset) of 5 V, while the square wave signal in Figure 1.44d has the same peak-to-peak value, but zero offset.

Information can be represented in one of many forms, for example, the amplitude, phase, or frequency. Figure 1.44e shows a signal (for example, from a microphone) that carries information in its amplitude, and Figure 1.44f shows a signal that carries information in its frequency.

To complete this section, we briefly touch on the concept of root mean square value to describe signals. Recall that our signal in Figure 1.44a was described as a sinusoid with an amplitude of 10 V. The same signal can be described as a sinusoid with rms (root mean square) value of $10/\sqrt{2}$. For a

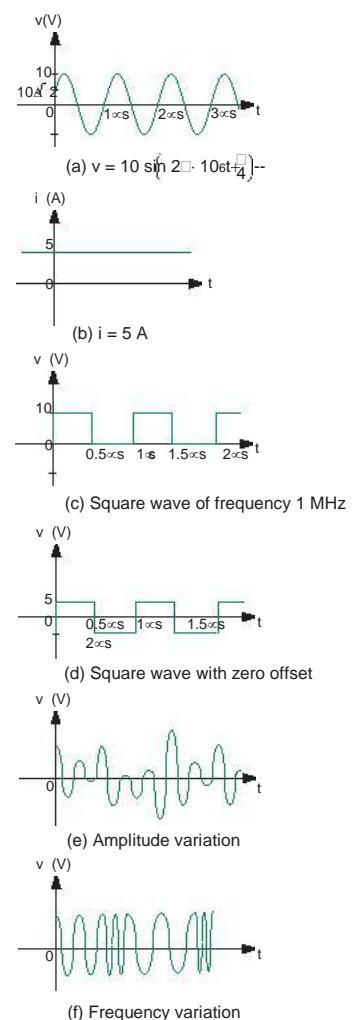


FIGURE 1.44 Several examples of analog signals: (a) a 1-MHz sinusoidal signal with an amplitude of 10 V and a phase offset of $\pi/4$; (b) a 5-ADC signal; (c) a 1-MHz square wave signal with a 5-V offset; (d) a 1-MHz square wave signal with zero offset; (e) a signal carrying information in its amplitude; (f) a signal carrying information in its frequency.

sinusoidal signal, or for that matter, any periodic signal v with period T , the rms is computed as follows:

$$V_{\text{rms}} = \sqrt{\frac{1}{T} \int_{t_1}^{t_1+T} v^2(t) dt} \quad (1.24)$$

where the integration is performed over one cycle.

The significance of the rms value of a periodic signal can be seen by computing the average power p^- delivered to a resistance of value R by a periodic voltage signal $v(t)$ with period T . For periodic signals, the average power can be obtained by integrating the power over one cycle and dividing by the cycle time:

$$p^- = \frac{1}{T} \int_{t_1}^{t_1+T} \frac{v^2(t) dt}{R} \quad (1.25)$$

For a linear, time-invariant resistor, we can pull R out of the integral to write

$$p^- = \frac{1}{R} \frac{1}{T} \int_{t_1}^{t_1+T} v^2(t) dt \quad (1.26)$$

By defining the rms value of a periodic signal as in Equation 1.24 we can rewrite Equation 1.26 as

$$p^- = R V_{\text{rms}}^2 \quad (1.27)$$

By the artful definition of Equation 1.24, we have managed to obtain an expression for power resembling that due to a DC signal. In other words, the rms value of a periodic signal is the value of a DC signal that would have resulted in the same average power dissipation.¹⁸ In like manner, the rms value of a DC signal is simply the constant value of the signal itself.

Thus, as in a sinusoidal voltage with rms value V_{rms} applied across a resistor of value R will result in an average power dissipation of V_{rms}^2 / R .

For example, 120-V 60-Hz wall outlets in the United States are rated by their rms values. Thus, they supply a sinusoidal voltage with a peak amplitude of $120 \times \sqrt{2} = 170$ V.

Native Signal Representation

Sometimes, circuit signals provide a native representation of physical quantities, as was the case with our lightbulb example in Figure 1.4. The circuit in Figure 1.4b was a model of the physical circuit in Figure 1.4a, which comprised

¹⁸This new voltage unit, called the rms, was originally defined by the pioneers of the electric power industry to avoid (or possibly perpetuate) confusion between DC power and AC power.

a battery, wires, and a lightbulb. The purpose of the original circuit was to convert chemical energy stored in the battery into light. To do so, the battery converted the chemical energy to electrical energy, the wires then guided the electrical energy to the lightbulb, and the lightbulb converted at least some of this electrical energy to light. Thus, the circuit in Figure 1.4 performed a very primitive form of energy processing.

The circuit in Figure 1.4 was proposed to model the original circuit, and to help determine such quantities as the current flowing through the lightbulb and the power dissipated in it. In this case, the signal representations in the lumped-parameter circuit were chosen naturally. The quantities of interest in the physical circuit, namely its voltages and currents, were represented by the same voltages and currents in the circuit model. This is an example of native signal representation.

Non-Native Signal Representation

A more interesting occurrence is that of non-native signal representation. In this case, electrical signals are used to represent non-electrical quantities, which is common in electronics signal processing. For example, consider an electronic sound amplifier. Such a system might begin with a front-end transducer, such as a microphone, that converts sound into an electrical signal that represents the sound. This electrical signal is then amplified, and possibly filtered, to produce a signal representing the desired output sound. Finally, a back-end transducer, such as a speaker, converts the processed electrical signal back into sound. Because electrical signals can be transduced and processed with ease, electronic circuits provide an amazingly powerful means for information processing, and have all but replaced native processing. For example, electronic amplifiers have now replaced megaphones.

The choice of signal type, for example current or voltage, often depends on the availability of convenient transducers (elements that convert from one form of energy to another — for example, sound to electricity), power considerations, and the availability of appropriate circuit elements. Voltage is a popular representation and is used throughout this book. We will also see several situations later in which a voltage signal is converted to a current signal and vice versa as it is being processed in an electronics system.

1.8.2 DIGITAL SIGNALS—VALUE DISCRETIZATION

In contrast to the continuous representation of analog signals, we can quantize signals into discrete or lumped signal values. Value discretization forms the basis of the digital abstraction, which yields a number of advantages such as better noise immunity compared to an analog signal representation. Although most physical signals are analog in nature, it is worth noting that there are a few physical signals that are naturally quantized, and so would have

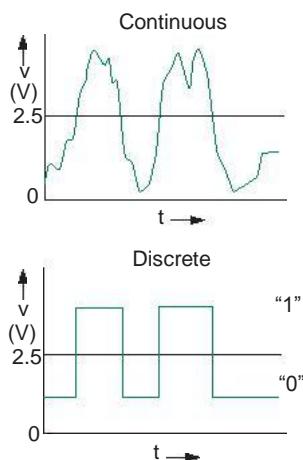


FIGURE 1.45 Voltage value discretization into two levels.

a naturally quantized signal representation. Wealth is an example of such a signals since monetary currencies are not generally considered to be infinitely divisible.¹⁹

To illustrate valuediscretization, consider the discretization of voltage as shown in Figure 1.45. Here, we discretize voltage into a finite number of information levels, for example, the two levels named “0” and “1.” Under this quantization, if a voltage is observed to be below 2.5 V we interpret its value as representing the information level “0.” If its value is above 2.5 V, we interpret it as representing the information level “1.” Correspondingly, to produce the information level “0,” we use any voltage less than 2.5 V. For example, we might use 1.25 V. Correspondingly, to produce the information level “1,” we might use the voltage 3.75 V.

As discussed in Chapter 5, discrete signals offer better noise immunity than analog signals, but they do so at the expense of precision. If the noise that corrupts a discrete signal does not move its physical value past a discretization threshold, then the noise will be ignored. For example, suppose the information level “0” in Figure 1.45 is represented by a 1.25-V signal, and the information level “1” in Figure 1.45 is represented by a 3.75-V signal. Provided the voltage does not rise above 2.5 V for “0,” or does not fall below 2.5 V for a “1,” it will be interpreted correctly. Thus, this discrete signal representation is two-level immune to representation ± 1.25 -

V noise. is unable to however, distinguish the loss between imprecisions small changes or coarse in the voltage.²⁰

In general, we can discretize values into any number of levels, for example, four. Thus the representation discussed thus far is a special case of value discretization called the binary representation where we discretize the voltage (or current for that matter) into two information levels: “0” and “1.” Because systems using more than two levels are difficult to build, most digital systems in use today use the binary representation. Accordingly, the digital representation has become synonymous with the binary representation.

19. Notice that before the advent of currencies, the barter system prevailed, and wealth was indeed analog in nature, since a loaf of bread, or a plot of land for that matter, theoretically is infinitely divisible!

20. For applications that care only about whether a signal is above or below some threshold, the loss in precision is of no consequence, and a two-level representation is sufficient. However, for other applications that care about small changes in a signal, the basic two-level representation of a signal must be extended. We show in Chapter 5 that practical digital systems can offer both arbitrary degrees of precision and noise immunity through a process of discretization and coding. Briefly, to recover some precision while retaining noise immunity, digital systems quantize signals into a large number of levels—for example, ~~256~~ these levels into a few binary digits—8, in our example, where each binary digit can be represented as a two-level voltage on a single wire. This method converts an analog signal on a single wire into a binary encoded signal on several wires, where each wire carries a voltage that can vary between two levels.

NativeandNon-NativeSignalRepresentation

As with analog signals, discrete signals can provide both native and non-native signal representations. The discrete binary values of 0 and 1 are a native representation for logic because they correspond naturally to the logical TRUE and FALSE values. Non-native signal representations can be derived from discrete signals by using sequences of digits having the value 0 or 1 to encode numbers whose values correspond to signal values of interest. Chapter 5 covers this topic in greater detail.

When designing a non-native information processing system, there are many choices for signal representation. For example, the use of voltage versus current, or analog versus discrete signals are two such choices. Each representation has its advantages and disadvantages, and facilitates a certain kind of processing. For example, digital representations offer noise immunity at the expense of precision. How these choices are made is usually application specific, and often depends on the availability of convenient transducers, power and noise considerations, and the availability of appropriate elements. The use of voltage to represent signals is probably most common, and is used routinely here. However, we will also encounter situations in which the signal representations switches from a voltage to a current and back again as the signal is processed.

1.9 SUMMARY

The discretization of matter into lumped elements such as batteries and resistors that obey the lumped matter discipline and connecting them using ideal wires is the essence of the lumped circuit abstraction.

The lumped matter discipline for lumped elements includes the following constraints:

1. The boundaries of the discrete elements must be chosen so that

$$\frac{\partial B}{\partial t} = 0$$

through any closed path outside the element for all time.

2. The elements must not include any net time-varying charge for all time. In other words,

$$\frac{\partial q}{\partial t} = 0$$

where q is the total charge within the element.

3. We must operate in the regime in which timescales of interest are much larger than the propagation delay of electromagnetic waves through the elements.

The lumped matter discipline for lumped circuits includes the following constraints:

1. The rate of change of magnetic flux linked with any portion of the circuit must be zero for all time.
2. The rate of change of the charge at any node in the circuit must be zero for all time.
3. The signal timescales must be much larger than the propagation delay of electromagnetic waves through the circuit.

The associated variables convention defines current to flow in at the device terminal assigned to be positive in voltage.

The instantaneous power consumed by a device is given by $p(t) = v(t)i(t)$, where $v(t)$ and $i(t)$ are defined using the associated variables discipline. Similarly, the instantaneous power delivered by a device is given by $p(t) = -v(t)i(t)$. The unit of power is the watt.

The amount of energy $w(t)$ consumed by a device over an interval of time $t_1 \rightarrow t_2$, is given by

$$w(t) = \int_{t_1}^{t_2} v(t)i(t)dt$$

where $v(t)$ and $i(t)$ are defined using the associated variables discipline. The unit of energy is the joule.

Ohm's law states that resistors that obey Ohm's law satisfy the equation $v = iR$, where R is constant. The resistance of a piece of homogeneous material is proportional to its length and inversely proportional to its cross-sectional area.

The resistance of a planar piece of material with length L and width W is given by $w_L \times R_P$, where R_P is the resistance of a square piece of material.

The four ideal circuit elements are the ideal conductor, the ideal linear resistor, the voltage source, and the current source. The element law for the ideal conductor is

$$v=0,$$

for the resistor with resistance R is

$$v=iR,$$

for the voltage source supplying a voltage V is

$$v=V,$$

and for the current source supplying a current I is

$$i=I.$$

The representation of parameters in physical systems by their equivalent electrical circuit parameters has been discussed.

The representation of information in terms of analog and digital electrical signals has been discussed.

In the process of introducing the elements and their element laws, we defined the symbols and units for various physical quantities. These definitions are summarized in Table 1.2. The units can be further modified with engineering multipliers. Several common multipliers and their corresponding prefix symbols and values are given in Table 1.3.

TABLE 1.2 Electrical engineering quantities, their units, and symbols for both.

Time	<i>t</i>	Second	s
Frequency	<i>f</i>	Hertz	Hz
Current	<i>i</i>	Ampere	A
Voltage	<i>v</i>	Volt	V
Power	<i>p</i>	Watt	W
Energy	<i>w</i>	Joule	J
Resistance	R	Ohm	
Conductance	G	Siemen	S

TABLE 1.3 Common engineering multipliers.

peta	P	10^{15}
tera	T	10^{12}
giga	G	10^9
mega	M	10^6
kilo	k	10^3
milli	m	10^{-3}
micro	μ	10^{-6}
nano	n	10^{-9}
pico	p	10^{-12}
femto	f	10^{-15}

EXERCISES

exercise 1.1 Quartz heaters are rated according to the average power drawn from a 120-V AC 60-Hz voltage source. Estimate the resistance (when operating) a 1200-W quartz heater.

NOTE: The voltage waveform for a 120-V AC 60-Hz waveform is

$$v(t) = \sqrt{2} 120 \cos(2\pi 60t).$$

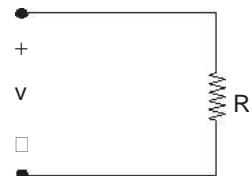
The factor of $\sqrt{2}$ in the peak amplitude cancels when the average power is computed. One result is that the peak amplitude of the voltage from a 120-volt wall outlet is about 170 volts.

exercise 1.2

a) The battery on your car has a rating stated in ampere-hours that permits you to estimate the length of time a fully charged battery could deliver any particular current before discharge. Approximately how much energy is stored by a 50A-hour 12-V battery?

b) Assuming 100% efficient energy conversion, how much water stored behind a 30 m high hydroelectric dam would be required to charge the battery?

exercise 1.3 In the circuit in Figure 1.46, R is a linear resistor and $v = V_{DC}$ a constant (DC) voltage. What is the power dissipated in the resistor, in terms of R and V_{DC} ?



exercise 1.4 In the circuit of the previous exercise (see Figure 1.46), $v = V_{AC} \cos \omega t$, a sinusoidal (AC) voltage with peak amplitude A_V and frequency ω , in radians/sec.

FIGURE 1.46

a) What is the average power dissipated in R ?

b) What is the relationship between V_{DC} and V_{AC} in Figure 1.46 when the average power in R is the same for both waveforms?

problem 1.1 Determine the resistance of a cube with sides of length l cm's and resistivity 10-cm , when a pair of opposite surfaces are chosen as the terminals.

PROBLEMS

problem 1.2 Sketch the伏-ampere characteristic of a battery rated at 10 V with an internal resistance of 10 Ohms.

problem 1.3 A battery rated at 7.2 V and 10000 J is connected across a lightbulb. Assume that the internal resistance of the battery is zero. Further assume that the resistance of the lightbulb is 100.

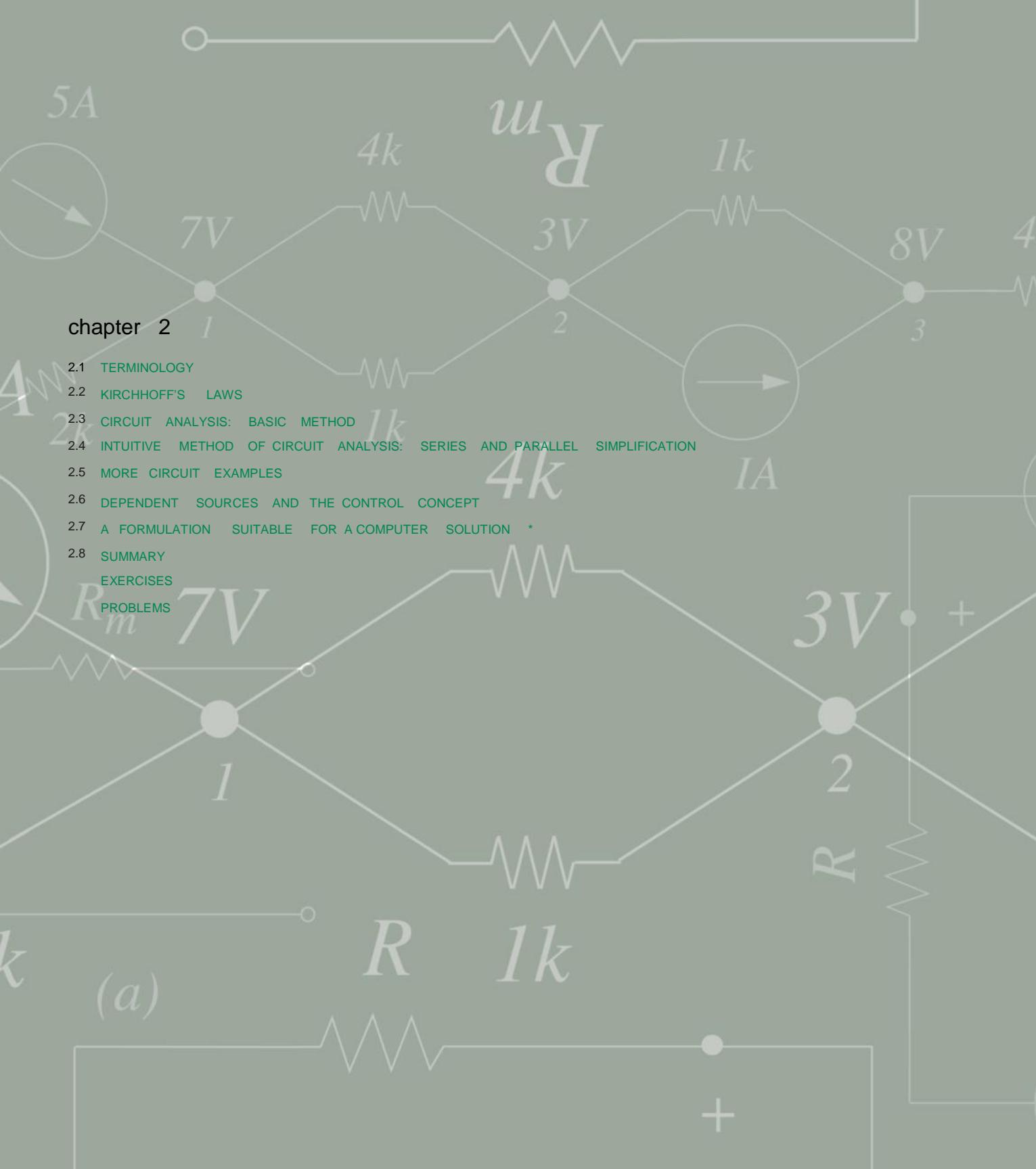
1. Draw the circuit containing the battery and the lightbulb and label the terminal variables for the battery and the lightbulb according to the associated variables discipline.
2. What is the power into the lightbulb?
3. Determine the power into the battery.
4. Show that the sum of the power into the battery and the power into the bulb is zero.
5. How long will the battery last in the circuit?

problem 1.4 A sinusoidal voltage source

$$v=10V\sin(\omega t)$$

is connected across a $1\text{ k}\Omega$ resistor.

1. Make a sketch of $p(t)$, the instantaneous power supplied by the source.
2. Determine the average power supplied by the source.
3. Now, suppose that a square wave generator is used as the source. If the square wave signal has a peak-to-peak of 20 V and a zero average value, determine the average power supplied by the source.
4. Next, if the square wave signal has a peak-to-peak of 20 V and a 10 V average value, determine the average power supplied by the source.



resistive networks

2

A simple electrical network made from a voltage source and four resistors is shown in Figure 2.1. This might be an abstract representation of some real electrical network, or a model of some other physical system, for example, a heat flow problem in a house. We wish to develop systematic general methods for analyzing circuit such as this, so that circuits of arbitrary complexity can be solved with dispatch. Solving or analyzing a circuit generally involves finding the voltage across, and current through, each of the circuit elements. Systematic general methods will also enable us to automate the solution techniques so that computers can be used to analyze circuits. Later on in this chapter and in the next, we will show how our problem formulation facilitates direct computer analysis.

To make the problem specific, suppose that we wish to find the current i_4 in Figure 2.1, given the values of the voltage source and the resistors. In general, we can resort to Maxwell's Equations to solve the circuit. But this approach is really impractical. Instead, when circuits obey the lumped matter discipline, Maxwell's Equations can be dramatically simplified into two algebraic relationships stated as Kirchhoff's voltage law (KVL) and Kirchhoff's current law (KCL). This chapter introduces these algebraic relationships and then uses them to develop a systematic approach to solving circuits, thereby finding the current i_4 in our specific example.

This chapter first reviews some terminology that will be useful in our discussions. We will then introduce Kirchhoff's laws and work out some examples to develop our facility with these laws. We will then introduce a systematic method for solving circuits based on Kirchhoff's laws using a very simple,

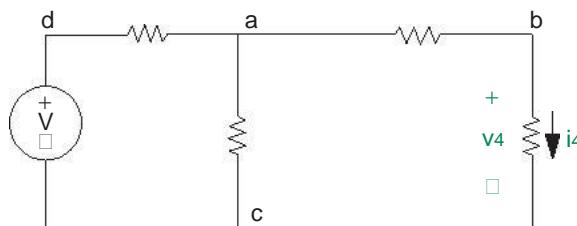


FIGURE 2.1 Simple resistive network.

illustrative circuit. We will then apply the same systematic method to solve more complicated examples, including the one shown in Figure 2.1.

2.1 TERMINOLOGY

Lumped circuit elements are the fundamental building blocks of electronic circuits. Virtually all of our analyses will be conducted on circuits containing two-terminal elements; multi-terminal elements will be modeled using combinations of two-terminal elements. We have already seen several two-terminal elements such as resistors, voltage sources, and current sources. Electronic access to an element is made through its terminals.

An electronic circuit is constructed by connecting together a collection of separate elements at their terminals, as shown in Figure 2.2. The junction points at which the terminals of two or more elements are connected are referred to as the nodes of a circuit. Similarly, the connections between the nodes are referred to as the edges or branches of a circuit. Note that each element in Figure 2.2 forms a single branch. Thus an element and a branch are the same for circuits comprising only two-terminal elements. Finally, circuit loops are defined to be closed paths through a circuit along its branches.

Several nodes, branches, and loops are identified in Figure 2.2. In the circuit in Figure 2.2, there are 10 branches (and thus, 10 elements) and 6 nodes.

As another example, *a* is a node in the circuit depicted in Figure 2.1 at which three branches meet. Similarly, *b* is a node at which two branches meet. *a* and *b* are examples of branches in the circuit. The circuit has five branches and four nodes.

Since we assume that the interconnections between the elements in a circuit are perfect (i.e., the wires are ideal), then it is not necessary for a set of elements to be joined together at a single point in space for their interconnection to be considered a single node. An example of this is shown in Figure 2.3. While the four elements in the figure are connected together, their connection does not occur at a single point in space. Rather, it is a distributed connection.

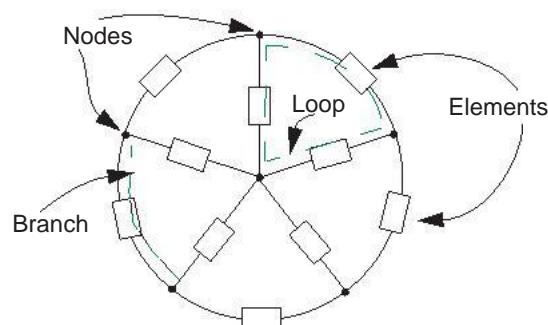


FIGURE 2.2 An arbitrary circuit.

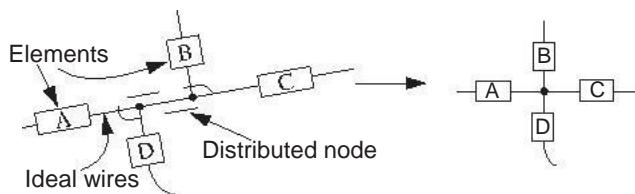


FIGURE 2.3 Distributed interconnections of four circuit elements that nonetheless occur at a single node.

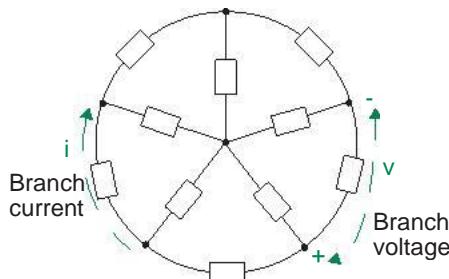


FIGURE 2.4 Voltage and current definitions illustrated on a branch in a circuit.

Nonetheless, because the interconnections are perfect, the connection can be considered to be a single node, as indicated in the figure.

The primary signals within a circuit are its currents and voltages, which we denote by the symbols i and v , respectively. We define a branch current as the current along a branch of the circuit (see Figure 2.4), and a branch voltage as the potential difference measured across a branch. Since elements and branches are the same for circuits formed of two-terminal elements, the branch voltages and currents are the same as the corresponding terminal variables for the elements forming the branches. Recall, as defined in Chapter 1, the terminal variables for an element are the voltage across and the current through the element.

As an example, i_4 is a branch current that flows through branch b_c in the circuit in Figure 2.1. Similarly, v_4 is the branch voltage for the branch b_c .

2.2 KIRCHHOFF'S LAWS

Kirchhoff's current law and Kirchhoff's voltage law describe how lumped-parameter circuit elements couple at their terminals when they are assembled into a circuit. KCL and KVL are themselves lumped-parameter simplifications of Maxwell's Equations. This section defines KCL and KVL and justifies that they are reasonable using intuitive arguments.¹ These laws are employed in circuit analysis throughout this book.

1. The interested reader can refer to Section A.2 in Appendix A for a derivation of Kirchhoff's laws from Maxwell's Equations under the lumped matter discipline.

2.2.1 KCL

Let us start with Kirchhoff's current law (KCL).

KCL The current flowing out of any node in a circuit must equal the current flowing in. That is, the algebraic sum of all branch currents flowing into any node must be zero.

Put another way, KCL states that the net current that flows into anode through some of its branches must flow out from that node through its remaining branches.

Referring to Figure 2.5, if the currents through the three branches in node a are i_a , i_b , and i_c , then KCL states that

$$i_a + i_b + i_c = 0.$$

Similarly, the currents into node b must sum to zero. Accordingly, we must have

$$-i_b - i_4 = 0.$$

KCL has a simple intuitive justification. Referring to the closed box-like surface depicted in Figure 2.5, it is easy to see that the currents i_a , i_b , and i_c must sum to zero, for otherwise, there would be a continuous charge buildup at node a . Thus, KCL is simply a statement of the conservation of charge.

Let us now illustrate the different interpretations of KCL with the help of Figure 2.6. Which interpretation you use depends upon convenience and the specific circuitry you are trying to analyze. Figure 2.6 shows anode joining N branches. Each of the branches contains some two-terminal element, the specifics of which are not relevant to our discussion. Note that all branch currents are defined to be positive into the node. Since KCL states that no net

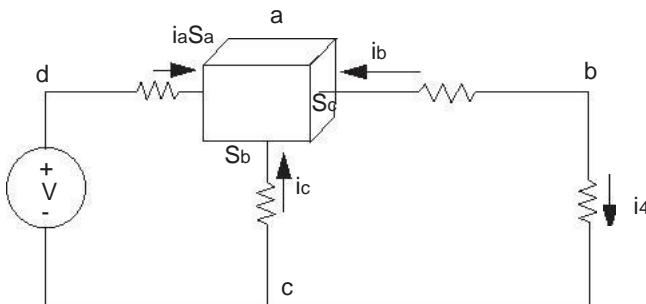


FIGURE 2.5 Currents into anode in the network.

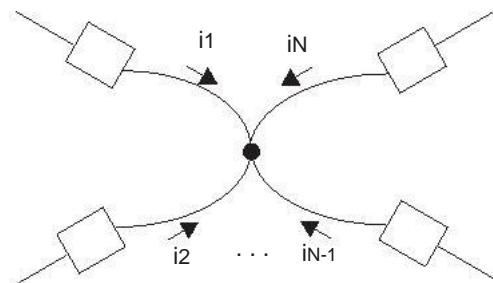


FIGURE 2.6 Anode at which N branches join.

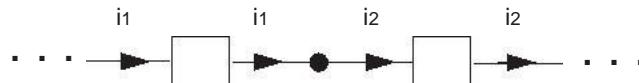


FIGURE 2.7 Two series-connected circuit elements.

current can flow into anode, it follows for the node in Figure 2.6 that

$$\sum_{n=1}^N i_n = 0. \quad (2.1)$$

Next, by negating Equation 2.1, KCL becomes

$$\sum_{n=1}^N (-i_n) = 0. \quad (2.2)$$

Since $-i_n$ is a current defined to be positive out from the node in Figure 2.6, this second form of KCL states that no net current can flow out from anode. Finally, Equation 2.1 can be rearranged to take the form

$$\sum_{n=1}^M i_n = \sum_{n=M+1}^N (-i_n), \quad (2.3)$$

which demonstrates that the current flowing into anode through one set of branches must flow out from the node through the remaining branches.

An important simplification of KCL focuses on the two series-connected circuit elements shown in Figure 2.7. Taking KCL to state that no net current can flow into a node, the application of KCL at the node between the two elements yields

$$i_1 - i_2 = 0 \Rightarrow i_1 = i_2. \quad (2.4)$$

This result is important because it shows that the branch currents passing through two series-connected elements must be the same. That is, there is nowhere for the current i_1 to go as it enters the node connecting the two elements except to exit that node as i_2 . In fact, with multiple applications of KCL, this observation is extendible to a longer string of series-connected elements. Such an extension would show that a common branch current passes through a string of series-connected elements.

example 2.1 a more general use of kcl To illustrate the more general use of KCL consider the circuit in Figure 2.8, which has six branches

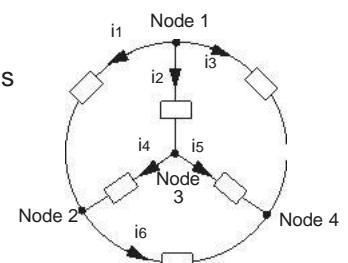


FIGURE 2.8 A circuit illustrating a more general use of KCL.

connecting four nodes. Again, taking KCL to state that no net current can flow into a node, the application of KCL to the four nodes in the circuit yields

$$\text{Node1: } 0 = -i_1 - i_2 - i_3 \quad (2.5)$$

$$\text{Node2: } 0 = i_1 + i_4 - i_6 \quad (2.6)$$

$$\text{Node3: } 0 = i_2 - i_4 - i_5 \quad (2.7)$$

$$\text{Node4: } 0 = i_3 + i_5 + i_6. \quad (2.8)$$

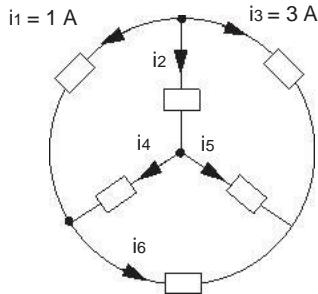


FIGURE 2.9 The circuit in Figure 2.8 with two branch currents numerically defined.

Note that because each branch current flows into exactly one node and out from exactly one node, each branch current appears exactly once in Equations 2.5 through 2.8 positively, and exactly once negatively. This would also be true if Equations 2.5 through 2.8 were all written to state that no net current can flow out from a node. Such patterns can often be used to spot errors.

It is also because each branch current flows into exactly one node and out from exactly one node that summing Equations 2.5 through 2.8 yields $0 = 0$. This in turn shows that the four KCL equations are dependent. In fact, a circuit with N nodes will have only $N-1$ independent statements of KCL. Therefore, when fully analyzing a circuit it is both necessary and sufficient to apply KCL to all but one node.

If some of the branch currents in a circuit are known, then it is possible that KCL alone can be used to find other branch currents in the circuit. For example, consider the circuit in Figure 2.8 with $i_1 = 1$ A and $i_3 = 3$ A, as shown in Figure 2.9. Using Equation 2.5, namely KCL for Node 1, it can be seen that $i_2 = -4$ A. This is all that can be learned from KCL alone given the information in Figure 2.9.

But, if we further know that $i_4 = -2$ A, for example, we can learn from KCL applied to the other nodes that $i_5 = -6$ A and $i_6 = 1$ A.

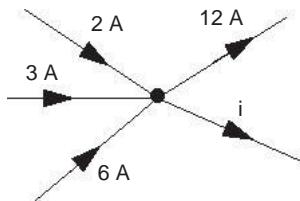


FIGURE 2.10 Five branches meeting at a node.

example 2.2 using kcl to determine an unknown branch current

Figure 2.10 shows five branches meeting at a node in some circuit. As shown in the figure, four of the branch currents are given. Determine i .

By KCL, the sum of all the currents entering a node must equal the sum of all the currents exiting the node. In other words,

$$2A + 3A + 6A = 12A + i$$

Thus, $i = -1$ A.

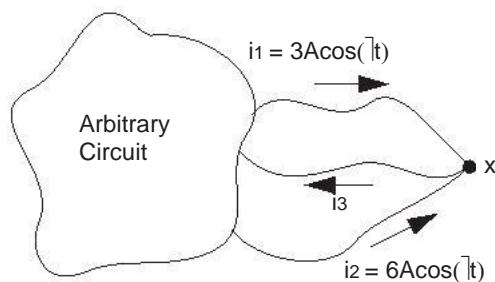


FIGURE 2.11 Node *x* in a circuit pulled out for display.

example 2.3 kcl applied to an arbitrary node

in a circuit Figure 2.11 shows an arbitrary circuit from which we have grabbed a node *x* and pulled it out for display. The node is a junction point for three wires with currents i_1 , i_2 , and i_3 . For the given values of i_1 and i_2 , determine the value of i_3 .

By KCL, the sum of all currents entering a node must be 0. Thus,

$$i_1 + i_2 - i_3 = 0$$

Note that i_3 is negated in this equation because it is defined to be positive for a current exiting the node. Thus i_3 is the sum of i_1 and i_2 and is given by

$$i_3 = i_1 + i_2 = 3\cos(\omega t) + 6\cos(\omega t) = 9\cos(\omega t)$$

example 2.4 even more kcl Figure 2.12 shows a node connecting three branches. Two of the branches have current sources that supply the currents shown. Determine the value of i .

By KCL, the sum of all the currents entering a node must equal 0. Thus

$$2A + 1A + i = 0$$

$$\text{and } i = -3A.$$

Finally, it is important to recognize that current sources can be used to construct circuits in which KCL is violated. Several examples of circuits constructed from current sources in which KCL is violated date every node are shown in Figure 2.13. We will not be concerned with such circuit shapes for two reasons. First, if KCL does not hold at a node, the electric charge must accumulate at that node. This is inconsistent with the constraint of the lumped matter discipline that $dq/dt = 0$. Second, if a circuit were actually built to violate KCL, something would ultimately give. For example, the current sources might cease

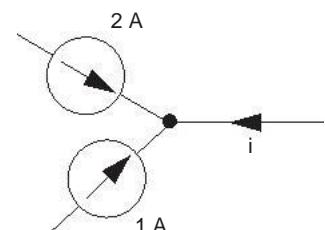


FIGURE 2.12 Node connecting three branches.

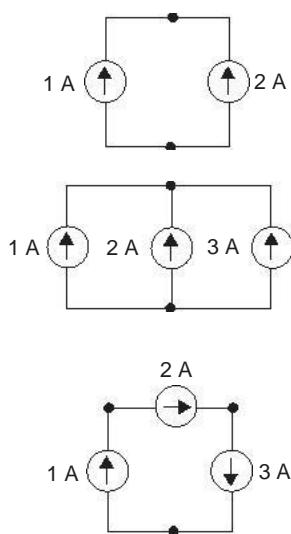


FIGURE 2.13 Circuits that violate KCL.

to function as ideal sources as they oppose one another. In any case, the behavior of the real circuit would not be well modeled by the type of circuit shown in Figure 2.13, and so there is no reason to study the latter.

2.2.2 KVL

Let us now turn our attention to Kirchhoff's voltage law (KVL). KVL is applied to circuit loops, that is, to interconnections of branches that form closed paths through a circuit. In a manner analogous to KCL, Kirchhoff's voltage law can be stated as:

KVL The algebraic sum of the branch voltages around any closed path in a network must be zero.

Alternatively, it states that the voltage between two nodes is independent of the path along which it is accumulated.

In Figure 2.14, the loop starting at node a , proceeding through nodes b and c , and returning to a , is a closed path. In other words, the closed loop defined is a closed $abcab$ path. The three circuit branches $a \rightarrow b$, $b \rightarrow c$, and $c \rightarrow a$ in Figure 2.14

According to KVL, the sum of the branch voltages around this loop is zero. That is,

$$V_{ab} + V_{bc} + V_{ca} = 0$$

In other words,

$$V_1 + V_4 + V_3 = 0$$

where we have taken the positive sign for each voltage when going from the positive terminal to the negative terminal. It is important that we are consistent in how we assign polarities to voltages as we go around the loop.

A helpful mnemonic for writing KVL equations is to assign the polarity to a given voltage in accordance with the first sign encountered when traversing that voltage around the loop.

Like KCL, KVL has an intuitive justification as well. Recall that the definition of the voltage between a pair of nodes in a circuit is the potential

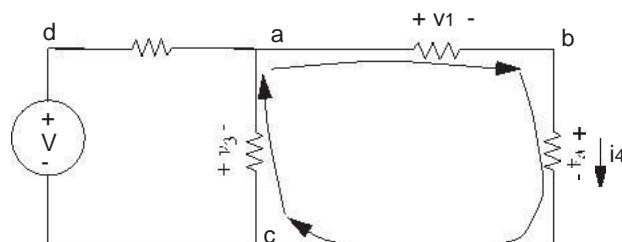


FIGURE 2.14 Voltages in a closed loop in the network.

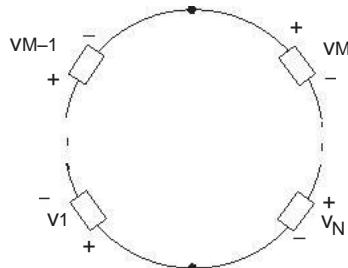


FIGURE 2.15 A loop containing N branches.

difference between the two nodes. The potential difference between two nodes is the sum of the potential differences for the set of branches along any path between the two nodes. For a loop, the start and end nodes are one and the same, and there cannot be a potential difference between a node and itself. Thus, since potential differences equate to voltages, the sum of branch voltages along a loop must equal zero. By the same reasoning, since the voltage between any pair of nodes must be unique, it must be independent of the path along which branch voltages are added. Notice from the definition of voltage that KVL is simply an expression of the principle of conservation of energy.

The different interpretations of KVL are illustrated with the help of Figure 2.15, which shows a loop containing N branches. Consider first the loop in Figure 2.15 in which all branch voltages decrease in the clockwise direction. Since KVL states that the sum of the branch voltages around a loop is zero, it follows for the loop in Figure 2.15 that

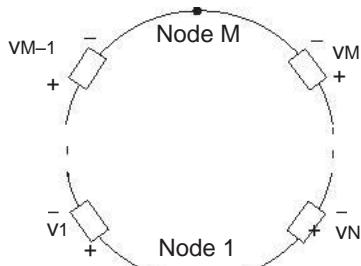
$$\sum_{n=1}^N v_n = 0. \quad (2.9)$$

Note that in summing voltages along a loop we have adopted the convention proposed earlier: A positive branch voltage is added to the sum if the path enters the positive end of a branch. Otherwise a negative branch voltage is added to the sum. Therefore, to arrive at Equation 2.9, we have traversed the loop in the clockwise direction. Next, by negating Equation 2.9, KVL becomes

$$\sum_{n=1}^N (-v_n) = 0. \quad (2.10)$$

Since $-v_n$ is a voltage defined to be positive in the opposite direction, this second form of KVL shows that KVL holds whether it is applied along the clockwise or counterclockwise path around the loop.

FIGURE 2.16 A loop containing N branches with some of the voltage definitions reversed.



example 2.5 path independence of kvl Consider the loop in Figure 2.16 in which some of the voltage definitions are reversed for convenience. Applying KVL to this loop yields

$$\begin{array}{c} \text{M-1} & \text{N} \\ \text{vn+} & (-vn)=0 \\ \text{n=1} & \text{n=M} \end{array} \Rightarrow \begin{array}{c} \text{M-1} & \text{N} \\ \text{vn=} & \text{vn.} \\ \text{n=1} & \text{n=M} \end{array} \quad (2.11)$$

The second equality in Equation 2.11 demonstrates that the voltage between two nodes is independent of the path along which it accumulated. In this case, the second equality shows that the voltage between Nodes 1 and M is the same whether accumulated along the path up the left side of the loop or the path up the right side of the loop.

An important simplification of KVL focuses on the two parallel-connected circuit elements shown in Figure 2.17. Starting from the upper node and applying KVL in the counterclockwise direction around the loop between the two circuit elements yields

$$v_1 - v_2 = 0 \Rightarrow v_1 = v_2. \quad (2.12)$$

This result is important because it shows that the voltages across two parallel-connected elements must be the same. In fact, with multiple applications of KVL, this observation is extendible to a longer string of parallel-connected elements. Such an extension would show that a common voltage appears across all parallel-connected elements in the string.

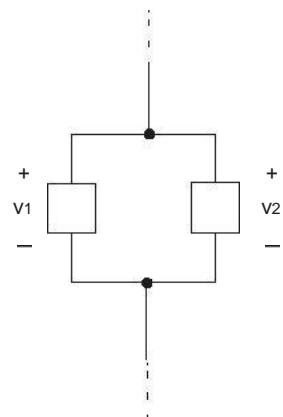


FIGURE 2.17 Two parallel-connected circuit elements.

example 2.6 a more general use of kvl To illustrate the more general use of KVL consider the circuit in Figure 2.18, which has six branches connecting four nodes. Four paths along the loops through the circuit are also defined in the figure; note that the external loop, Loop 4, is distinct from the other three. Applying

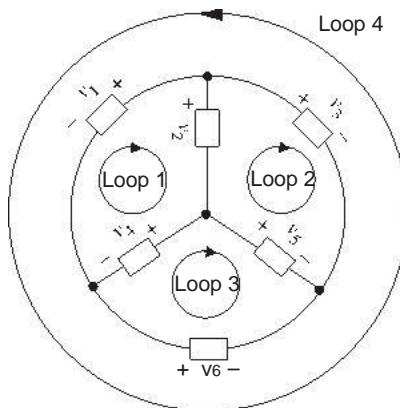


FIGURE 2.18 A circuit having four nodes and six branches.

KVL to the four loops yields

$$\text{Loop 1: } 0 = -v_1 + v_2 + v_4 \quad (2.13)$$

$$\text{Loop 2: } 0 = -v_2 + v_3 - v_5 \quad (2.14)$$

$$\text{Loop 3: } 0 = -v_4 + v_5 - v_6 \quad (2.15)$$

$$\text{Loop 4: } 0 = v_1 + v_6 - v_3 \quad (2.16)$$

Note that the paths along the loops have been defined so that each branch voltage is traversed positively around exactly one loop and negatively around exactly one loop.

It is for this reason that each branch voltage appears exactly once in Equations 2.13 through 2.16 positively, and exactly once negatively. As with the application of KCL, such patterns can often be used to spot errors.

It is also because each branch voltage is traversed exactly once positively and once negatively that summing Equations 2.13 through 2.16 yields $0 = 0$. This in turn shows that the four KVL equations are dependent. In general, a circuit with N nodes and B branches will have $B - N + 1$ loops around which independent applications of KVL can be made. Therefore, while analyzing a circuit it is necessary to apply KVL only to these loops, which will in total, traverse each branch at least once in the process.

If some of the branch voltages in a circuit are known, then it is possible that KVL alone can be used to find other branch voltages in the circuit. For example, consider the circuit in Figure 2.18 with $v_1 = 1\text{ V}$ and $v_3 = 3\text{ V}$, as shown in Figure 2.19. Using

Equation 2.16, namely KVL for Loop 4, it can be seen that $v_4 = -2\text{ V}$. This is all that can be learned from KVL alone given the information in Figure 2.19. But, if we further know that $v_2 = 2\text{ V}$, for example, we can learn from KVL applied to the other loops that $v_4 = -1\text{ V}$ and $v_5 = 5\text{ V}$.

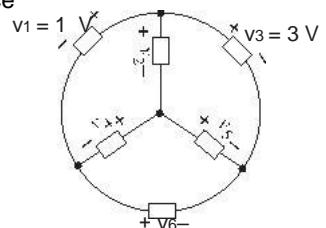


FIGURE 2.19 The circuit in Figure 2.18 with two branch voltages numerically defined.

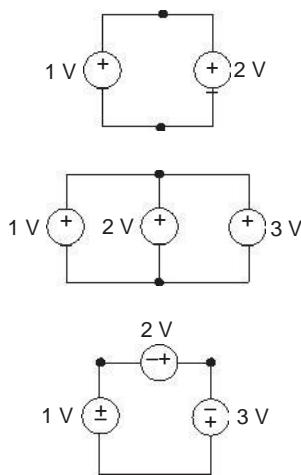


FIGURE 2.20 Circuits that violate KVL.

Finally, it is important to recognize that voltage sources can be used to construct circuits in which KVL is violated. Several examples of circuits constructed from voltage sources in which KVL is violated around every loop are shown in Figure 2.20. As with circuits that violate KCL, we will not be concerned with circuits that violate KVL, for two reasons. First, if KVL does not hold around a loop, then magnetic flux linkage will accumulate through that loop. This is inconsistent with the constraint of the lumped matter discipline that $\frac{dB}{dt} = 0$ outside the elements. Second, if a circuit were actually built to violate KVL, something would ultimately give. For example, the voltage sources might cease to function as ideal sources as they oppose one another. Alternatively, the loop inductance might begin to accumulate flux linkage, leading to high currents that would damage the voltage sources or their interconnections. In any case, the behavior of the real circuit would not be well modeled by the type of circuit shown in Figure 2.20, and so there is no reason to study the latter.

example 2.7 voltage sources in series

Two 1.5-V volt-

ages sources are reconnected in series as shown in Figure 2.21. What is the voltage at their terminals?

To determine v , employ, for example, a counterclockwise application of KVL around the circuit, treating the port formed by the two terminals as an element having voltage v . In this case, $1.5V + 1.5V - v = 0$, which has for its solution $v = 3V$.

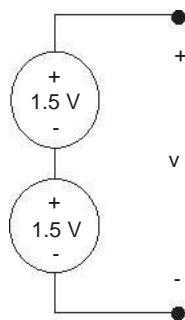


FIGURE 2.21 The series connection of two 1.5-V batteries.

example 2.8 kvl The voltages across two of the elements in the circuit in Figure 2.22 are measured as shown. What are the voltages, v_1 and v_2 , across the other two elements?

Since element #1 is connected in parallel with element #4, the voltages across them must be the same. Thus, $v_1 = 5V$. Similarly, the voltage across the series connection of elements #2 and #3 must also be 5V, so $v_2^2 = 3V$. This latter result can also be obtained through the counterclockwise application of KVL around the loop including elements #2, #3, and #4, for example. This yields, $v_2 + 2V - 5V = 0$. Again, $v_2 = 3V$.

example 2.9 verifying kvl for a circuit Verify that the branch voltages shown in Figure 2.23 satisfy KVL.

Summing the voltages in the loop e,d,a,b,e, we get

$$-3 - 1 + 3 + 1 = 0.$$

Similarly, summing the voltages in the loop f,c,b,e, we get

$$+1 - (-2) - 4 + 1 = 0.$$

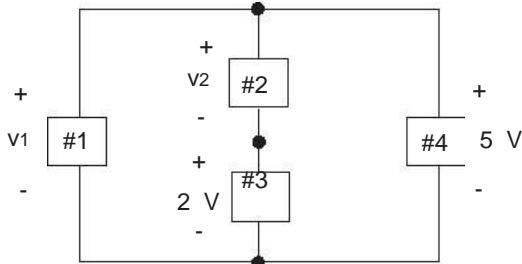


FIGURE 2.22 A circuit with two measured and two unmeasured voltages.

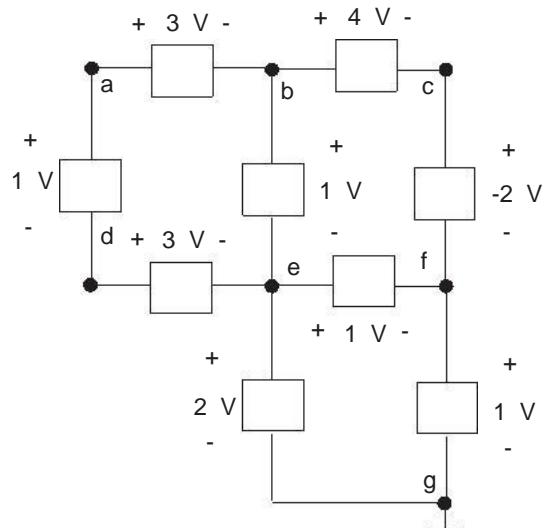


FIGURE 2.23 A circuit with element voltages as shown.

Finally, summing the voltages in the loop g,e,f,g, we get

$$-2 + 1 + 1 = 0.$$

KVL is satisfied since the sum of the voltages around each of the three circuit loops is zero.

example 2.10 summing voltages along different paths

Next, given the branch voltages shown in Figure 2.23, determine the voltage v_{ga} between the nodes g and a by summing the branch voltages along the path g,e,d,a. Then, show that v_{ga} is the same if path g,f,c,b,a is chosen.

Summing the voltage increases along the path g,e,d,a, we get

$$v_{ga} = -2V - 3V - 1V = -6V.$$

Similarly, summing the voltage increases along the path g,f,c,b, we get

$$v_{ga} = -1V - (-2V) - 4V - 3V = -6V.$$

Clearly, both paths yield -6V for v_{ga} .

Thus far, Chapters 1 and 2 have shown that the operation of a lumped system is described by two types of equations: equations that describe the behavior of its individual elements, or element laws (Chapter 1), and equations that describe how its elements interact when they are connected to form the system, or KCL and KVL (Chapter 2). For an electronic circuit, the element laws relate the branch currents to the branch voltages of the elements. The interactions between its elements are described by KCL and KVL, which are also expressed in terms of branch currents and voltages. Thus, branch currents and voltages become the fundamental signals within a lumped electronic circuit.

2.3 CIRCUIT ANALYSIS: BASIC METHOD

We are now ready to introduce a systematic method of solving circuits. It is framed in the context of a simple class of circuits, namely circuits containing only sources and linear resistors. Many of the important analysis issues can be understood through the study of these circuits. Solving a circuit involves determining all the branch currents and branch voltages in the circuit. In practice, some currents or voltages may be more important than others, but we will not make that distinction yet.

Before we return to the specific problem of analyzing the electrical network shown in Figure 2.1, let us first develop the systematic method using a few simpler circuits and build up our insight into the technique. We saw previously that under the lumped matter discipline, Maxwell's Equations reduce to the basic element laws and the algebraic KVL and KCL. Accordingly, a systematic solution of the network involves the assembly and subsequent joint solution of two sets of equations. The first set of equations comprises the constituent relations for the individual elements in the network. The second set of equations results from the application of Kirchhoff's current and voltage laws.

This basic method of circuit analysis, also called the KVL and KCL method or the fundamental method, is outlined by the following steps:

1. Define each branch current and voltage in the circuit in a consistent manner. The polarities of these definitions can be arbitrary from one branch to the next. However, for any given branch, follow the associated variables convention (see Section 1.5.3 in Chapter 1). In other words, the branch current should be defined as positive into the positive voltage terminal of the branch. By following the associated variables, element laws can be applied consistently, and the solutions will follow a much clearer pattern.
2. Assemble the element laws for the elements. These element laws will specify either the branch current or branch voltage in the case of an independent source, or specify the relation between the branch current

and voltage in the case of a resistor. Examples of these element laws were represented in Section 1.6.

3. Apply Kirchhoff's current and voltage laws as discussed in Section 2.2.
4. Jointly solve the equations assembled in Steps 2 and 3 for the branch variables defined in Step 1.

The remainder of this chapter is devoted to circuit analysis examples that rigorously follow these steps.

Once the two sets of equations are assembled, which is a relatively easy task, the analysis of a circuit essentially becomes a problem of mathematics, as indicated by Step 4. That is, the equations assembled earlier must be combined and used to solve for the branch currents and voltages of interest. However, because there is more than one way to approach this problem, our study of circuit analysis does not end with the direct approach outlined here. Considerable time can be saved, and considerable insight can be gained, by approaching circuit analyses in different ways. These gains are important subjects of this and future chapters.

2.3.1 SINGLE-RESISTOR CIRCUITS

To illustrate our basic approach to circuit analysis, consider the simple circuit shown in Figure 2.24. The circuit has one independent source and one resistor, and so has two branches, each with a current and a voltage. The goal of our circuit analysis is to find these branch variables.

Step 1 in the analysis is to label the branch variables. We do so in Figure 2.25. Since there are two branches, there are two sets of variables. Notice that the branch variables for the current source branch and for the resistor branch each follow the associated variables convention.

Now, we proceed with Steps 2 through 4: assemble the element laws, apply KCL and KVL, and then simultaneously solve the two sets of equations to complete the analysis.

The circuit has two elements. Following Step 2 we write the two element laws for these elements as

$$i_1 = -I, \quad (2.17)$$

$$v_2 = R i_2, \quad (2.18)$$

respectively. Here, v_1 , i_1 , v_2 , and i_2 are the branch variables. Note the distinction between the branch variable i_1 and the source amplitude I . Here, the independent source amplitude I is assumed to be known.

Next, following Step 3, we apply KCL and KVL to the circuit. Since the circuit has two nodes, it is appropriate to write KCL for one node, as discussed

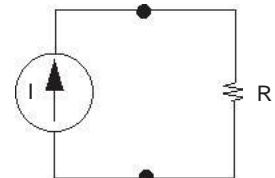


FIGURE 2.24 A circuit with only one independent current source and one resistor.

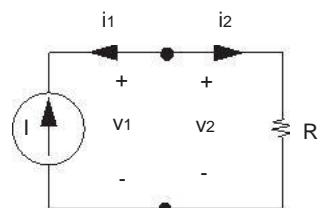


FIGURE 2.25 Assignment of branch variables.

in Section 2.2.1. The application of KCL at either node yields

$$i_1 + i_2 = 0. \quad (2.19)$$

The circuit also has two branches that form one loop. So, following the discussion in Section 2.2.2 it is appropriate to write KVL for one loop. Starting at the upper node and traversing the loop in a clockwise manner, the application of KVL yields

$$v_2 - v_1 = 0. \quad (2.20)$$

Notice we have used our mnemonic discussed in Section 2.2.2 for writing KVL equations. For example, in Equation 2.20, we have assigned a + polarity to v_2 since we first encounter the + sign when traversing the branch with variable v_2 . Similarly, we have assigned a - polarity to v_1 since we first encounter the - sign when traversing the v_1 branch.

Finally, following Step 4, we combine Equations 2.17 through 2.20 and solve jointly to determine all four branch variables in Figure 2.25. This yields

$$-i_1 = i_2 = I, \quad (2.21)$$

$$v_1 = v_2 = RI, \quad (2.22)$$

and completes the analysis of the circuit in Figure 2.25.

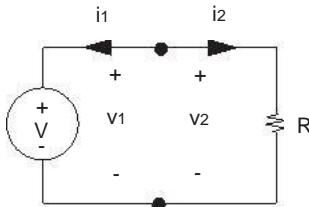


FIGURE 2.26 A circuit with only one independent voltage source and one resistor.

example 2.11 single-resistor circuit with one independent voltage source Now consider another simple circuit shown in Figure 2.26. This circuit can be analyzed in an identical manner. It too has two elements, namely a voltage source and a resistor. Figure 2.26 already shows the definitions of branch variables, and so accomplishes Step 1.

Next, following Step 2 we write the element laws for these elements as

$$v_1 = V \quad (2.23)$$

$$v_2 = RI_2, \quad (2.24)$$

respectively. Here, the independent source amplitude V is assumed to be known.

Next, following Step 3, we apply KCL and KVL to the circuit. Since the circuit has two nodes, it is again appropriate to write KCL for one node. The application of KCL at either node yields

$$i_1 + i_2 = 0. \quad (2.25)$$

The circuit also has two branches that form one loop, so it is again appropriate to write KVL for one loop. The application of KVL around the one loop in either direction yields

$$v_1 = v_2. \quad (2.26)$$

Finally, following Step 4, we combine Equations 2.23 through 2.26 to determine all four branch variables in Figure 2.26. This yields

$$-i_1 = i_2 = \frac{V}{R}, \quad (2.27)$$

$$v_1 = v_2 = V, \quad (2.28)$$

and completes the analysis of the circuit in Figure 2.26.

For the circuit in Figure 2.25, there are four equations to solve for four unknown branch variables. In general, a circuit having B branches will have $2B$ unknown branch variables: B branch currents and B branch voltages. To find these variables, $2B$ independent equations are required, B of which will come from element laws, and B of which will come from the application of KVL and KCL. Moreover, if the circuit has N nodes, then $N - 1$ equations will come from the application of KCL and $B - N + 1$ equations will come from the application of KVL.

While the two examples of circuit analysis presented here are admittedly very simple, they nonetheless illustrate the basic steps of circuit analysis: label the branch variables, assemble the element laws, apply KCL and KVL, and solve the resulting equations for the branch variables of interest. While we will not always follow these steps explicitly and in exactly the same order in future chapters, it is important to know that we will nonetheless process exactly the same information.

It is also important to realize that the physical results of the analysis of the circuit in Figure 2.25, and of any other circuit for that matter, cannot depend on the polarities of the definitions of the branch variables. We will work an example to illustrate this point.

example 2.12 polarities of branch variables

Consider the analysis of the circuit in Figure 2.27, which is physically the same as the circuit in Figure 2.25. The only difference in the two figures is the reversal of the polarities of i_2 and v_2 . The circuit in Figure 2.27 circuit has the same two elements, and their element laws are still

$$i_1 = -I \quad (2.29)$$

$$v_2 = R i_2. \quad (2.30)$$

Note that the polarity reversal of i_2 and v_2 has not changed the element law for the resistor from Equation 2.18 because the element law for a linear resistor is symmetric when the terminal variables are defined according to the associated variables convention. The circuit also has the same two nodes and the same loop. The application of KCL at

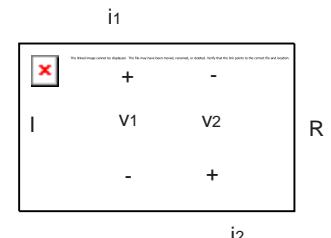


FIGURE 2.27 A circuit similar to the one shown in Figure 2.24.

either node now yields

$$i_1 - i_2 = 0, \quad (2.31)$$

and the application of KVL around the loop now yields

$$v_1 + v_2 = 0. \quad (2.32)$$

Note that Equations 2.31 and 2.32 differ from Equations 2.19 and 2.20 because of the polarity reversal of i_2 and v_2 . Finally, combining Equations 2.29 through 2.32 yields

$$-i_1 = -i_2 = I \quad (2.33)$$

$$v_1 = -v_2 = RI, \quad (2.34)$$

which completes the analysis of the circuit in Figure 2.27.

Now compare Equations 2.33 and 2.34 to Equations 2.21 and 2.22. The important observation here is that they are the same except for the polarity reversal of the solutions for i_2 and v_2 . This must be the case because the circuits in Figures 2.25 and 2.27 are physically the same, and so their branch variables must also be physically the same. Since we have chosen to define two of these branch variables with different polarities in the two figures, the signs of their values must differ accordingly so that they describe the same physical branch current and voltage.

2.3.2 QUICK INTUITIVE ANALYSIS OF SINGLE-RESISTOR CIRCUITS

Before moving on to more complex circuits, it is worthwhile to analyze the circuit in Figure 2.25 in a more intuitive and efficient manner. Here, the element law for the current source directly states that $i_1 = -I$. Next, the application of KCL to either node reveals that $i_2 = -i_1 = I$. In other words, the current from the source flows entirely through the resistor. Next, from the element law for the resistor, it follows that $v_2 = R_i_2 = RI$. Finally the application of KVL to the one loop yields $v_1 = v_2 = RI$ to complete the analysis.

example 2.13 quick intuitive analysis of a single-resistor circuit This example considers the circuit in Figure 2.26. Here, the element law for the voltage source directly states that $v_1 = V$. Next, the application of KVL around the one loop reveals that $v_2 = v_1 = V$. In other words, the voltage from the source is applied directly across the resistor. Next, from the element law for the resistor, it follows that $i_2 = v_2/R = V/R$. Finally, the application of KCL to either node yields $i_1 = -i_2 = -V/R$ to complete the analysis. Notice that we had made use of a similar intuitive analysis in solving our battery and lightbulb example in Chapter 1.

The important message here is that it is not necessary to first assemble all the circuit equations, and then solve them all at once. Rather, using a little

intuition, it is likely to be much faster to approach the analysis in a different manner. We will have more to say about this in Section 2.4 and in Chapter 3.

2.3.3 ENERGY CONSERVATION

Once the branch variables of a circuit have been determined, it is possible to examine the flow of energy through the circuit. This is often a very important part of circuit analysis. Among other things, such an examination should show that energy is conserved in the circuit. This is the case for the circuits in Figures 2.25 and 2.26. Using Equations 2.21 and 2.22 we see that the power into the current source in Figure 2.25 is

$$i_1 v_1 = -R i_2 \quad (2.35)$$

and that the power into the resistor is

$$i_2 v_2 = R i_2. \quad (2.36)$$

The negative sign in Equation 2.35 indicates that the current source actually supplies power.

Similarly, using Equations 2.27 and 2.28 we see that the power into the voltage source in Figure 2.26 is

$$i_1 v_1 = -R \frac{V_2}{-} \quad (2.37)$$

and that the power into the resistor is

$$i_2 v_2 = V_R. \quad (2.38)$$

In both cases, the power generated by the source is equal to the power dissipated in the resistor. Thus, energy is conserved in both circuits.

Conservation of energy is itself an extremely powerful method for obtaining many types of results in circuits. It is particularly useful in dealing with complicated circuits that contain energy storage elements such as inductors and capacitors that we will introduce in later chapters. Energy methods can often allow us to obtain powerful results without a lot of mathematical grunge. We will use two energy-based approaches in this book.

- One energy approach equates the energy supplied by a set of elements in a circuit to the energy absorbed by the remaining set of elements in a circuit. Usually, this method involves equating the power generated by the devices in a circuit to the power dissipated in the circuit.
- Another energy approach equates the total amount of energy in a system at two different points in time (assuming that there are no dissipative elements in the circuit).

We will illustrate the use of the first method using a few examples in this section, and Section 9.5 in Chapter 9 will highlight examples using the second method.

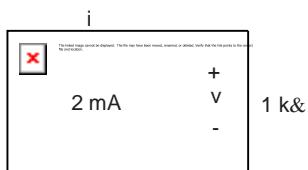


FIGURE 2.28 Energy conservation example.

example 2.14 energy conservation Determine the value of v in the circuit in Figure 2.28 using the method of energy conservation.

We will show that the mathematical grunge of the basic method can be eliminated using the energy method and some intuition. In Figure 2.28, the current source maintains a current $i = 0.002 \text{ A}$ through the circuit. To determine v , we equate the power supplied by the source to the power dissipated by the resistor. Since the current source and the resistor share terminals, the voltage v appears across the current source as well. Thus, the power into the source is given by

$$v \times (-0.002) = -0.002v.$$

In other words, the power supplied by the source is $0.002v$.

Next, the power into the resistor is given by

$$\frac{v^2}{1\text{k}} = 0.001v^2.$$

Finally, equating the power supplied by the source to the power dissipated by the resistor, we have

$$0.002v = 0.001v^2.$$

In other words, $v = 0.5 \text{ V}$.

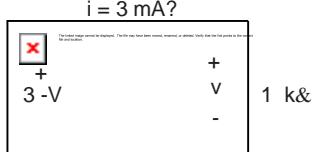


FIGURE 2.29 Another energy conservation example.

example 2.15 using an energy-based approach to verify a result A student applies the basic method to the circuit in Figure 2.29 and obtains $i = 3 \text{ mA}$. Determine whether this answer is correct by using the method of energy conservation.

By energy conservation, the power supplied by the source must be equal to the power dissipated by the resistor. Using the value of the current obtained by the student, the

energy dissipated by the resistor is given by

$$i_2 \times 1\text{K} = 9\text{mW}.$$

The energy into the voltage source is given by

$$3V \times 3\text{mA} = 9\text{mW}.$$

In other words, the energy supplied by the source is given by -9 mW . Clearly the energy supplied by the source is not equal to the energy dissipated by the resistor, and so $i = 3\text{ mA}$ is incorrect. Notice that if we reverse the polarity of i , energy will be conserved. Thus, $i = -3\text{ mA}$ is the correct answer.

2.3.4 VOLTAGE AND CURRENT DIVIDERS

We will now tackle several circuits called dividers that are slightly more complex than the simple single-loop, two-node, two-element circuit of the previous section. These circuits will comprise a single loop and three or more elements, or two nodes and three or more elements. Dividers produce fractions of input currents or voltages and will be encountered often in subsequent chapters. For the moment, however, they are good examples on which to practice circuit analysis, and we can use them to gain important insight into circuit behavior.

Voltage Dividers

A voltage divider is an isolated loop that contains two or more resistors and a voltage source in series. A physical voltage divider circuit is illustrated pictorially in Figure 2.30a. We have connected two resistors in series, and connected the pair by some wires to a battery. Such a circuit is useful if we wish to obtain some arbitrary fraction, say 10%, of the battery voltage at the terminals marked v_2 . To find the relation between v_2 and the battery voltage and resistor values, we draw the circuit in schematic form, as shown in Figure 2.30b. We then follow the basic four-step method outlined in Section 2.3 to solve the circuit.

1. The circuit has three elements, or branches, and hence it will have six branch variables. Figure 2.31 shows one possible assignment of branch variables. To find these branch variables, we again assemble the element laws and the appropriate applications of KCL and KVL, and then simultaneously solve the resulting equations.
2. The three element laws are

$$v_0 = -V \quad (2.39)$$

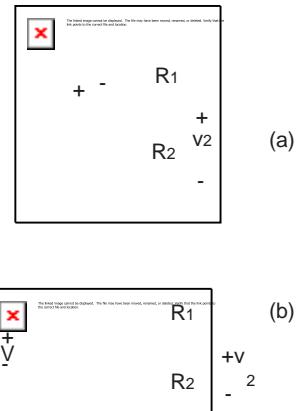


FIGURE 2.30 Voltage-divider circuit.

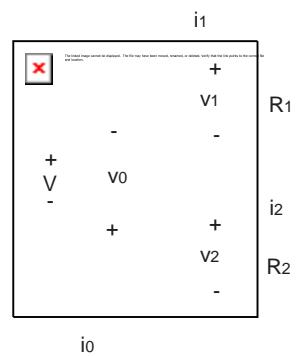


FIGURE 2.31 Assignment of branch variables to the voltage divider.

$$v_1 = R_1 i_1 \quad (2.40)$$

$$v_2 = R_2 i_2. \quad (2.41)$$

3. Next, we apply KCL and KVL. The application of KCL to the two upper nodes yields

$$i_0 = i_1 \quad (2.42)$$

$$i_1 = i_2 \quad (2.43)$$

and the application of KVL to the one loop yields

$$v_0 + v_1 + v_2 = 0. \quad (2.44)$$

4. Finally, Equations 2.39 through 2.44 can be solved for the six unknown branch variables. This yields

$$i_0 = i_1 = i_2 = \frac{1}{R_1 + R_2} V \quad (2.45)$$

and

$$v_0 = -V \quad (2.46)$$

$$v_1 = \frac{R_1}{R_1 + R_2} V \quad (2.47)$$

$$v_2 = \frac{R_2}{R_1 + R_2} V. \quad (2.48)$$

This completes the analysis of the two-resistor voltage divider.

From the results of this analysis it should be apparent why the circuit in Figure 2.31 is called a voltage divider. Notice that v_2 is some fraction (specifically, $R_2/(R_1+R_2)$) of the source voltage V , as desired. The fraction is the ratio of the resistance about which the voltage is measured and the sum of the resistances. By adjusting the relative values of R_1 and R_2 we can make this fraction adjust anywhere from 0 to 1. If, for example, we wish v_2 to be one-tenth of V , as suggested at the start of this example, then R_1 should be nine times as big as R_2 .

Notice also that $v_1 + v_2 = V$, and that the two resistors divide the voltage V in proportion to their resistances since $v_1/V = R_1/R_2$. For example, if R_1 is twice R_2 then v_1 is twice v_2 .

The voltage-divider relationship in terms of conductance can be found from Equation 2.48 by substituting the conductances in place of the resistances:

$$v_2 = \frac{1/G_2}{1/G_1 + 1/G_2 V} \quad (2.49)$$

$$= \frac{G}{G_1 + G_2 V}. \quad (2.50)$$

Hence the voltage-divider relation expressed in terms of conductances involve the conductance opposite the desired voltage, divided by the sum of the two conductances.

The simple circuit topology of Figure 2.30 is so common that the voltage-divider relation given by Equation 2.48 will become a primitive in our circuit vocabulary. It is helpful to build up a set of such primitives, which are really solved simple cases, to speed up circuit analysis, and to facilitate intuition.

A simple mnemonic: For the voltage v_2 , take the resistance associated with v_2 divided by the sum of the two resistances, multiplied by the voltage applied to the pair.

example 2.16 voltage divider A voltage divider circuit such as that in Figure 2.30 has $V = 10\text{V}$ and $R_2 = 1\text{k}$. Choose R_1 such that v_2 is 10% of V .

By the voltage-divider relation of Equation 2.48, we have

$$v_2 = \frac{R_2}{R_1 + R_2 V}.$$

For v_2 to be 10% of V we must have

$$\frac{v_2}{V} = 0.1 = \frac{R_2}{R_1 + R_2}.$$

For $R_2 = 1\text{k}$, we must choose R_1 such that

$$\frac{1\text{k}}{0.1} = \frac{1\text{k}}{R_1 + 1\text{k}}$$

or $R_1 = 9\text{k}$.

The correct answer cannot be displayed. The box you have chosen is marked, however, as incorrect. Verify that the box you wanted to be correct is the one selected.

example 2.17 temperature variation Consider the circuit in Figure 2.31 in which $V = 5\text{V}$, $R_1 = 10\text{k}$, and $R_2 = 10\text{k}(1 + T/(500^\circ\text{C}))$, where T is the temperature of the second resistor. Over what range does v_2 vary if T varies over the range $-100^\circ\text{C} \leq T \leq 100^\circ\text{C}$?

Given the temperature range, R_2 varies over the range:

$$0.8 \times 10^3 \leq R_2 \leq 1.2 \times 10^3.$$

Therefore, following Equation 2.48, $2.2 \text{ V} \leq v_2 \leq 2.7 \text{ V}$, with the higher voltage occurring at the higher temperature.

Having determined its branch variables we can now examine the flow of energy through the two-resistor voltage divider. Using Equations 2.45 through 2.48 we see that the power into the source is

$$i_{0V0} = -\frac{V_2}{R_1 + R_2} \quad (2.51)$$

and that the power into each resistor is

$$i_{1V1} = \frac{R_1 V_2}{(R_1 + R_2)^2} \quad (2.52)$$

$$i_{2V2} = \frac{R_2 V_2}{(R_1 + R_2)^2}. \quad (2.53)$$

Since the power into the voltage source is the opposite of the total power into the two resistors, energy is conserved in the two-resistor voltage divider. That is, the power generated by the voltage source is exactly dissipated in the two resistors.

Resistors in Series

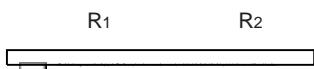


FIGURE 2.32 Resistors in series.

In electronic circuits one often finds resistors connected in series, as shown in Figures 2.31 and 2.32. For example, in our lightbulb example of Chapter 1, suppose the wire had a nonzero resistance, then the current through the wire would be related to the value of several resistances—including those of the wires and the bulb—in series. Our lumped circuit abstraction and the resulting Kirchhoff's laws allow us to calculate the equivalent resistance of such combinations using simple algebra.

Specifically, the analysis of the voltage dividers shows that two resistors in series act as a single resistor having a resistance R_s equal to the sum of the two individual resistances R_1 and R_2 . In other words, series resistances add.

$$R_s = R_1 + R_2 \quad (2.54)$$

To see this, observe that the voltage source in Figure 2.31 applies the voltage V to two series resistors R_1 and R_2 , and that from Equation 2.43 these resistors respond with the common current $i_1 = i_2$ through their branches. Further, observe from Equation 2.45 that this common current, $i = i_1 = i_2$

is linearly proportional to the voltage from the source. Specifically, from Equation 2.45, the common current is given by

$$i = \frac{1}{R_1 + R_2} V. \quad (2.55)$$

By comparing Equation 2.55 to Equation 1.4, we conclude that for two resistors in series, the equivalent resistance of the pair when viewed from their outer terminals is the sum of the individual resistance values. Specifically, if R_s is the resistance of the series resistor pair, then, from Equation 2.55, we find that

$$R_s = \frac{V}{i} = R_1 + R_2. \quad (2.56)$$

This is consistent with the physical derivation of resistance in Equation 1.6 since placing resistors in series essentially increases their combined length.

By substituting their conductances, we can also obtain the equivalent conductance of a pair of conductances in series as

$$\frac{1}{G_s} = \frac{1}{G_1} + G \frac{1}{2}. \quad (2.57)$$

Simplifying,

$$G_s = \frac{G_1 G_2}{G_1 + G_2}. \quad (2.58)$$

As shown in the ensuing example, we can generalize our result for two series resistors to N resistors in series as:

$$R_s = R_1 + R_2 + R_3 + \dots + R_N. \quad (2.59)$$

Remember this result as another common circuit primitive.

example 2.18 an N -resistor voltage divider

Now consider a more general voltage divider having N resistors, as shown in Figure 2.33. It can be analyzed in the same manner as the two-resistor voltage divider. The only difference is that there are now more unknowns to find, and hence more equations to work with. To begin, suppose we assign the branch variables as shown in Figure 2.33.

The element laws are

$$v_0 = -V \quad (2.60)$$

$$v_n = R_n i_n, \quad 1 \leq n \leq N. \quad (2.61)$$

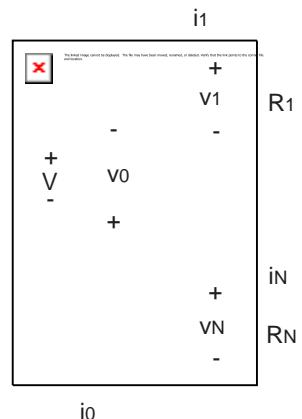


FIGURE 2.33 A voltage divider with N resistors.

Next, the application of KCL to the N-1 upper nodes yields

$$i_n = i_{n-1}, \quad 1 \leq n \leq N \quad (2.62)$$

and the application of KVL to the one loop yields

$$v_0 + v_1 + \dots + v_N = 0. \quad (2.63)$$

Finally, Equations 2.60 through 2.63 can be solved to yield

$$i_n = \frac{1}{R_1 + R_2 + \dots + R_N} V, \quad 0 \leq n \leq N \quad (2.64)$$

$$v_0 = -V \quad (2.65)$$

$$v_n = \frac{R_n}{R_1 + R_2 + \dots + R_N} V, \quad 1 \leq n \leq N. \quad (2.66)$$

This completes the analysis.

As was the case for the two-resistor voltage divider, the preceding analysis shows that series resistors divide voltage in proportion to their resistances. This follows from the R_n in the numerator of the right-hand side of Equation 2.66.

Additionally, the analysis again shows that series resistances add. To see this, let R_s be the equivalent resistance of the N series resistors. Then, from Equation 2.64 we see that

$$R_s = \frac{V}{i_n} = R_1 + R_2 + \dots + R_N. \quad (2.67)$$

This result is summarized in Figure 2.34.

Finally, the two voltage-divider examples illustrate an important point, namely that series elements all carry the same branch current because the terminals from these elements are reconnected end-to-end without connection to additional branches through which the current can divert. This results in the KCL seen in Equations 2.42, 2.43, and 2.62, which state the equivalence of the branch currents.

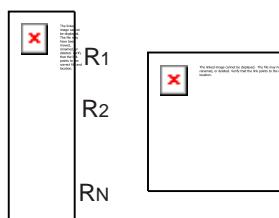


FIGURE 2.34 The equivalence of series resistors.

example 2.19 voltage-divider circuit Determine v_1 and v_2 for the voltage-divider circuit in Figure 2.35 with $R_1 = 10 \Omega$, $R_2 = 20 \Omega$, and $v(t) = 3V$ using (a) the basic method and (b) the results from voltage dividers.

(a) Let us first analyze the circuit using the basic method.

1. Assign variables as in Figure 2.36.

2. Write the constituent relations

$$v_0 = 3V \quad (2.68)$$

$$v_1 = 10i_1 \quad (2.69)$$

$$v_2 = 20i_2. \quad (2.70)$$

3. Write KCL

$$i_1 - i_2 = 0. \quad (2.71)$$

4. Write KVL

$$-v_0 + v_1 + v_2 = 0. \quad (2.72)$$

Now eliminate i_1 and i_2 from Equations 2.69, 2.70, and 2.71, to obtain

$$v_1 = \frac{v_2}{2}. \quad (2.73)$$

Substituting this result and $v_0 = 3V$ into Equation 2.72, we obtain

$$-3V + \frac{v_2}{2} + v_2 = 0. \quad (2.74)$$

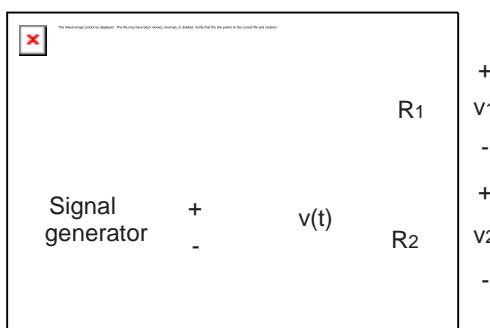


FIGURE 2.35 Voltage-divider circuit.

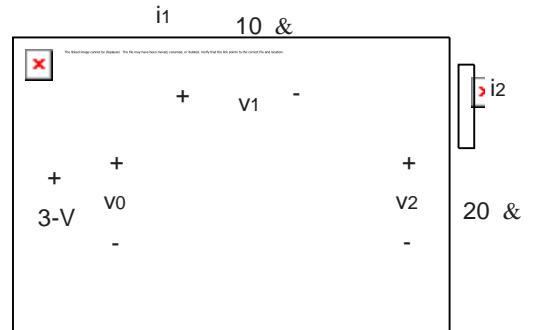


FIGURE 2.36 Voltagedividerwithvariablesassigned.

Hence,

$$v_2 = \frac{2}{3}V = 2V \quad (2.75)$$

and from Equation 2.73, $v_1 = 1V$.

(b) Using the voltage-divider relation, we can write by inspection the value v_2 as a function of the source voltage as follows:

$$v_2 = \frac{20}{10+20}V = 2V.$$

Similarly,

$$v_1 = \frac{10}{10+20}V = 1V.$$

CurrentDividers

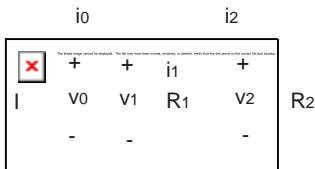


FIGURE 2.37 A currentdivider with two resistors.

A current divider is a circuit with two nodes joining two or more parallel resistors and a current source. Two current dividers are shown in Figures 2.37 and 2.38, the first with two resistors and the second with N resistors. In these circuits, the resistors share, or divide, the current from the source in proportion to their conductances. It turns out that the equations for voltage dividers comprising voltages and resistances, and those for current dividers comprising currents and conductances, are very similar. Therefore, to highlight the duality between these two types of circuits, we will attempt to mirror the steps from our voltage divider discussion.

Consider the two-resistor current divider shown in Figure 2.37. It has three elements, or branches, and hence six unknown branch variables. To find these branch variables we again assemble the element laws and the appropriate applications of KCL and KVL, and then simultaneously solve the resulting equations. First, the three element laws are

$$i_0 = -I \quad (2.76)$$

$$v_1 = R_1 i_1 \quad (2.77)$$

$$v_2 = R_2 i_2. \quad (2.78)$$

Next, the application of KCL to either node yields

$$i_0 + i_1 + i_2 = 0 \quad (2.79)$$

and the application of KVL to the two internal loops yields

$$v_0 = v_1 \quad (2.80)$$

$$v_1 = v_2. \quad (2.81)$$

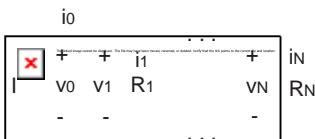


FIGURE 2.38 A currentdivider with N resistors.

Finally, Equations 2.76 through 2.81 can be solved for the six unknown branch variables. This yields

$$i_0 = -I \quad (2.82)$$

$$i_1 = \frac{R_2}{R_1 + R_2} I \quad (2.83)$$

$$i_2 = \frac{R_1}{R_1 + R_2} I \quad (2.84)$$

and

$$V_0 = V_1 = V_2 = \frac{R_1 R_2}{R_1 + R_2} I \quad (2.85)$$

This completes the analysis of the two-resistor current divider.

The nature of the current division in Equations 2.83 and 2.84 is more obvious if they are expressed in terms of the conductances G_1 and G_2 where $G_1 \equiv 2.841/R$ become i_1 and $G_2 \equiv 1/R_2$. With these definitions, i_1 and i_2 in Equations 2.83

$$i_1 = \frac{G_1}{G_1 + G_2} I \quad (2.86)$$

$$i_2 = \frac{G_2}{G_1 + G_2} I \quad (2.87)$$

It is now apparent that $i_1 + i_2 = I$, and that the two resistors divide the current in proportion to their conductances since $i_1/I = G_1/G_1 + G_2$. For example, if $G_1 = 1$ twice G_2 then i_1 is twice i_2 .

To summarize our current divider discussion:

The current i_2 is equal to the input current I multiplied by a factor, this time made up of the opposite resistor, R_1 , divided by the sum of the two resistors (see Equation 2.84).

This relation will also become a useful primitive in our analysis vocabulary.

As we did with voltage dividers, we can now examine the flow of energy through the two-resistor current divider. Using Equations 2.82 through 2.85 we see that the power into the source is

$$i_0 V_0 = -\frac{R_1 R_2 I_2}{R_1 + R_2} \quad (2.88)$$

and that the power into each resistor is

$$i_1 V_1 = \frac{R_1 R_2 I_2}{(R_1 + R_2)^2} \quad (2.89)$$

$$i_2v_2 = \frac{R_{21}R_{22}I_2}{(R_{11}+R_{22})^2} \quad (2.90)$$

Since the power into the current source is the opposite of the total power into the two resistors, energy is conserved in the two-resistor current divider. That is, the power generated by the current source is exactly dissipated in the two resistors.

Resistors in Parallel

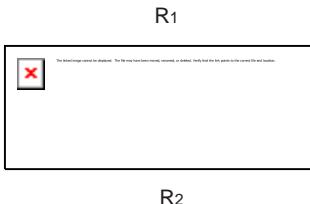


FIGURE 2.39 Resistors in parallel.

Resistors in parallel occur as commonly as resistors in series. Two resistors in parallel are shown in Figures 2.37 and 2.39.

Our preceding analysis shows that the two resistors in parallel act as a single resistor R_P having a conductance G_P (where $G_P = 1/R_P$) equal to the sum of the two individual conductances. In other words, parallel conductances add:

$$G_P = G_1 + G_2 \quad (2.91)$$

To see this, observe that the current source in Figure 2.37 applies the current I to two parallel resistors, and that from Equation 2.85 these resistors respond at their terminals with the common voltage $v = v_1 = v_2$ that is linearly proportional to the current from the source. Thus, the resistors behave together as a single resistor when viewed from their common terminals.

Let G_P be the conductance of the parallel resistor pair. Then, from Equation we can 2.85, write with the substitution of $G_1 \equiv 1/R_1$ and $G_2 \equiv 1/R_2$, and $v = v_1 = v_2$,

$$v = \frac{R_1 R_2}{R_1 + R_2} \quad (2.92)$$

Or, in terms of conductances,

$$v = \frac{1}{G_1 + G_2} \quad (2.93)$$

In other words,

$$G_P = \frac{1}{\frac{1}{G_1} + \frac{1}{G_2}} \quad (2.94)$$

Hence, the equivalent conductance of the two parallel resistors is the sum of their individual conductances. This is consistent with the physical derivation of resistance in Equation 1.6 since placing resistors in parallel essentially increases their combined cross-sectional area.

In practice, it is more common to work with resistances than it is to work with conductances, although conductances are sometimes more convenient. For this reason, it is worthwhile to find the equivalent resistance of two parallel

resistors in terms of the individual resistances. Let the equivalent resistance be R_P . Then, from Equation 2.94 it follows that

$$\frac{1}{R_P} = G_P = G_1 + G_2 = \frac{1}{R_1} + \frac{1}{R_2} \quad (2.95)$$

from which it follows that the equivalent resistance of two resistances in parallel is given by

$$R_P = \frac{R_1 R_2}{R_1 + R_2} \quad (2.96)$$

which is the product of the two resistor values divided by their sum. This relation can also be observed in 2.92, which has a form analogous to Ohm's law (Equation 1.4).

Parallel resistors occur frequently enough to merit shorthand notation: the two resistor values separated by two parallel vertical lines

$$R_{12} = \frac{R_1 R_2}{R_1 + R_2} \quad (2.97)$$

As we show shortly, we can generalize this result to N resistors connected in parallel. If the equivalent resistance for N resistors connected in parallel is given by R_P , then the reciprocal of R_P is given in terms of $R_1, R_2, R_3, \dots, R_n$ as

$$\frac{1}{R_P} = \frac{1}{R_1} + \frac{1}{R_2} + \frac{1}{R_3} + \frac{1}{R_4} + \dots + \frac{1}{R_n} \quad (2.98)$$

The equivalent resistance of N resistors in parallel is yet another example of a useful primitive that is worth remembering.

The shorthand notation for N resistances in parallel is

$$R_P = R_1 R_2 R_3 \dots R_N \quad (2.99)$$

As an example, when N resistors, each with resistance R , are connected in parallel, the effective resistance is simply

$$R_P = N R \quad (2.100)$$



FIGURE 2.41 AVLSIresistor.



FIGURE 2.42 AVLSIresistor depicted asseriesconnected squares.

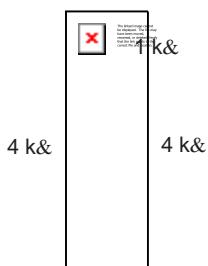


FIGURE 2.43 Aseries-parallel resistorcombination.

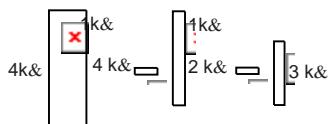


FIGURE 2.44 Equivalent resistanceof a series-parallel resistorcombination.

example 2.21 planar resistor Figure 2.41 depicts a planar resistor fabricated on a VLSI chip. Suppose $R_P=10$, find the effective resistance between terminals A and B.

Recalling that the resistance of any square piece of the given material is R_P , we can view the planar resistor as being composed of three series-connected squares, each with resistance R_P as depicted in Figure 2.42.

Thus the effective resistance between A and B is simply $3R_P$. In practice, however, the resistance of such a piece of material is likely to be larger than $3R_P$ due to fringing effects. Section 1.4 discusses several such effects that limit the accuracy of our lumped circuit model.



example 2.22 equivalent resistance Compute the equivalent resistance of the resistor combination shown in Figure 2.43.

Using the series-parallel simplification sequence shown in Figure 2.44, we find the equivalent resistance to be $3k$.



example 2.23 equivalent resistance combinations

What equivalent resistors can be made by combining up to three 1000 -ohm resistors in series and/or in parallel?

Figure 2.45 shows the possible resistor combinations that use up to three resistors. To determine their equivalent resistance, use the parallel combination result from Equation 2.109 and the series combination result from Equation 2.67. This yields equivalent resistances of: (A) 1000 , (B) 500 , (C) 2000 , (D) 333 , (E) 667 , (F) 1500 , and (G) 3000 .

2.3.5 A MORE COMPLEX CIRCUIT

We are now ready to tackle more complex circuits, such as the electrical network shown in Figure 2.1. More specifically, let us suppose that the current i_4 is of particular interest to us. This circuit contains two loops and four nodes, and is amenable to our four-step solution procedure.

As our first step, we choose to assign the branch variables as shown in Figure 2.46. Recall that the assignment of voltage and current variables is still arbitrary (other than the constraint of associated variables), and that the solution is invariant under this choice.

As our second step, we write the element laws for each of the elements. The constituent relations for the resistors in this circuit are of the form $v = iR$, and the relation for the voltage source is $v = V$. In terms of the variables

defined in Figure 2.46, the constituent relations are

$$v_1 = i_1 R_1 \quad (2.110)$$

$$v_2 = i_2 R_2 \quad (2.111)$$

$$v_3 = i_3 R_3 \quad (2.112)$$

$$v_4 = i_4 R_4 \quad (2.113)$$

$$v_5 = V \quad (2.114)$$

Our third step involves writing the KVL and KCL equations for the circuit. For KVL, one possible choice of closed paths is shown in Figure 2.47. If we assign the polarity to a voltage in accordance with the first sign encountered, we see that for Loop 1, v_5 and v_2 are negative, v_1 is positive. The corresponding KVL equations are

$$-v_5 + v_1 - v_2 = 0 \quad (2.115)$$

$$+v_2 + v_3 + v_4 = 0. \quad (2.116)$$

A different choice of paths is shown in Figure 2.48. The KVL equations for this choice are derivable from the set we already have; hence (1) they are equally valid, and (2) they contain no new information. It follows that adding

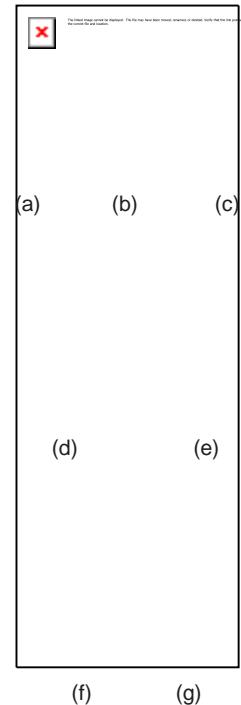


FIGURE 2.45 Various combinations of resistors involving up to three resistors.

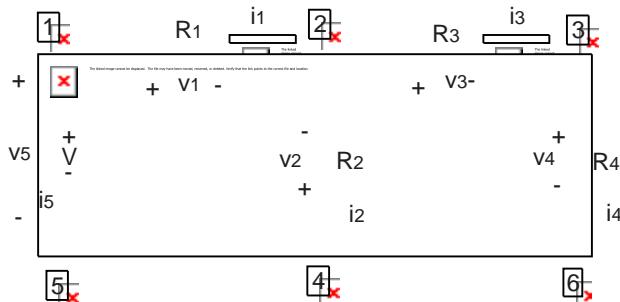


FIGURE 2.46 Assignment of branch variables.

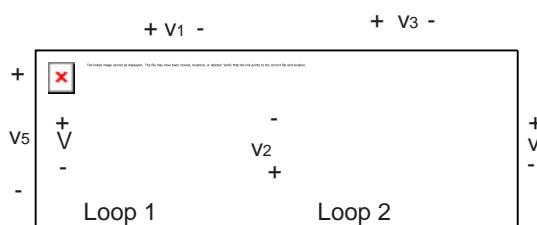
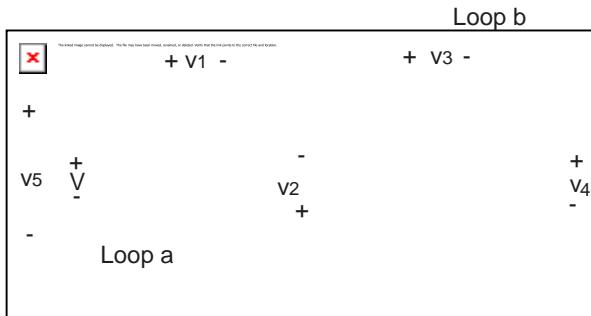


FIGURE 2.47 One choice of closed paths.

FIGURE 2.48 Alternative choice of paths.



a third loop (loop b, Figure 2.48) to Figure 2.47 will not yield a KVL equation independent of Equations 2.115 and 2.116.²

We now write the KCL equations. From Figure 2.46, at Node 1, KCL yields

$$-i_5 - i_1 = 0 \quad (2.117)$$

and at Node 2

$$+i_1 + i_2 - i_3 = 0 \quad (2.118)$$

and at Node 3

$$i_3 - i_4 = 0. \quad (2.119)$$

As in the case of loops, it is possible to write KCL at Node 4, but the equation is not independent of those we already have.

One might be tempted to write node equations for the junctions labeled 5 and 6, but this doesn't make much sense. The branch between 4 and 6 is a perfect conductor, hence it is really just part of the copper lead attached to resistor R4. For this reason we did not bother defining a separate current variable for this branch. A similar argument applies to branch 4-5.

Another way to emphasize that 5 and 6 are not true nodes is to draw the circuit as shown in Figure 2.49. Clearly the circuit topology is unchanged in the sense that the interconnections among resistors and source are the same as before, but the false nodes have disappeared. We conclude that a node should be defined as a junction where two or more circuit elements, other than perfect conductors, join together. Whenever a number of circuit elements connect to one perfect conductor, (for example, 5, 4, 6 in Figure 2.46) only one node is created.

²A detailed treatment of the topological issues underlying the rules is contained in Guillemin (Introductory Circuit Theory, Will, 1953) or Bose and Stevens (Introductory Network Theory, Harper and Row, 1965).

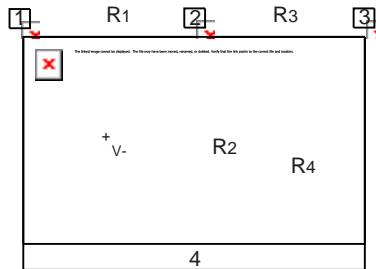


FIGURE 2.49 Circuit in Figure 2.46 redrawn.

We now have ten independent equations (Equations 2.110 through 2.119) and ten unknowns: five voltages and five currents. Thus the equations can be solved for any variable by simple algebra. To find i_4 , for example, we can first substitute the constituent relations, Equations 2.110 through 2.114 into Equations 2.115 and 2.116:

$$-V + i_1 R_1 - i_2 R_2 = 0 \quad (2.120)$$

$$i_2 R_2 + i_3 R_3 + i_4 R_4 = 0. \quad (2.121)$$

Now eliminating i_2 and i_3 using Equations 2.118 and 2.119

$$-V + i_1 R_1 + (i_1 - i_4) R_2 = 0 \quad (2.122)$$

$$(-i_1 + i_4) R_2 + i_4 R_3 + i_4 R_4 = 0. \quad (2.123)$$

Rewriting to collect variables and place in the known voltages on the right-hand side of each equation, we obtain

$$i_1 (R_1 + R_2) - i_4 R_2 = V \quad (2.124)$$

$$-i_1 R_2 + i_4 (R_2 + R_3 + R_4) = 0, \quad (2.125)$$

which can be expressed in matrix form as

$$\begin{pmatrix} (R_1 + R_2) & -R_2 \\ -R_2 & (R_2 + R_3 + R_4) \end{pmatrix} \begin{pmatrix} i_1 \\ i_4 \end{pmatrix} = \begin{pmatrix} V \\ 0 \end{pmatrix}. \quad (2.126)$$

The matrix equation is in the form

$$Ax = b$$

where x is a column vector of the unknowns (i_1 and i_4) and b is the column vector of drive voltages and currents (in this case, just V). This vector of unknowns can be solved by using standard linear algebraic techniques.

For example, i_4 can be found by applying Cramer's Rule³

$$i_4 = \frac{VR_2}{(R_1+R_2)(R_2+R_3+R_4)-R_2} \quad (2.127)$$

$$= \frac{VR_2}{R_1R_2+R_1R_3+R_1R_4+R_2R_3+R_2R_4}. \quad (2.128)$$

With some more effort, we can find the rest of the branch variables as given below

$$-i_5 = i_1 = \frac{R_2+R_3+R_4}{R_1(R_2+R_3+R_4)+R_2(R_3+R_4)V} \quad (2.129)$$

$$i_2 = -\frac{R_3+R_4}{R_1(R_2+R_3+R_4)+R_2(R_3+R_4)V} \quad (2.130)$$

$$i_3 = i_4 = \frac{R_2}{R_1(R_2+R_3+R_4)+R_2(R_3+R_4)V} \quad (2.131)$$

$$v_5 = V \quad (2.132)$$

$$v_1 = \frac{R_1(R_2+R_3+R_4)}{R_1(R_2+R_3+R_4)+R_2(R_3+R_4)V} \quad (2.133)$$

$$v_2 = -\frac{R_2(R_3+R_4)}{R_1(R_2+R_3+R_4)+R_2(R_3+R_4)V} \quad (2.134)$$

$$v_3 = \frac{R_2R_3}{R_1(R_2+R_3+R_4)+R_2(R_3+R_4)V} \quad (2.135)$$

$$v_4 = \frac{R_2R_4}{R_1(R_2+R_3+R_4)+R_2(R_3+R_4)V}. \quad (2.136)$$

This completes our analysis.

Note that in Figure 2.46, resistors R_1 and R_2 alone do not form a simple voltage divider because of the presence of R_3 and R_4 . It is true, however, that R_3 and R_4 form a voltage divider. Further, R_1 and the net resistance of R_2 , R_3 , and R_4 form a second voltage divider.

The analysis of the circuit in Figure 2.46 following the general approach developed in this chapter is both straightforward and tedious, with emphasis on

³Cramer's Rule is a popular method for solving equations of the type $Ax=b$, where x and b are column vectors, and A is a matrix. See Appendix D for more details.

tedious. Fortunately, as we shall see in Chapter 3, there are much less tedious approaches to this analysis. However, in advance of that we can still simplify the analysis by employing results taken solely from earlier sections of this chapter. Specifically, Section 2.4 shows that we can employ the equivalence of parallel and series resistors, and the behavior of current and voltage dividers, to develop an intuitive and simple approach to solving many types of circuits.

2.4 INTUITIVE METHOD OF CIRCUIT ANALYSIS: SERIES AND PARALLEL SIMPLIFICATION

To develop our intuition, let us first illustrate the method with the simple voltage divider in Figure 2.50a. Suppose we were interested in determining the voltage across resistor R_2 . The figure shows a few important variables marked on it. An intuitive way of analyzing the circuit is to replace the two resistors by their series equivalent, as in Figure 2.50b, then find i_1 using Ohm's law. From Equation 2.56, the equivalent series resistance is given by

$$R_s = R_1 + R_2$$

and from Equation 1.4

$$i_1 = V/R_s.$$

Because i_1 must be the same in the two circuits (in Figures 2.50a and 2.50b), we can now find v_2 from Figure 2.50a

$$v_2 = i_1 R_2 \quad (2.137)$$

$$= \frac{R_2}{R_1 + R_2} V. \quad (2.138)$$

We have now determined the value of v_2 in a few simple steps using results from series resistances and Ohm's law. In the future, we will actually write down the result for the voltage divider in a single step by directly applying the voltage divider relation in Equation 2.138.

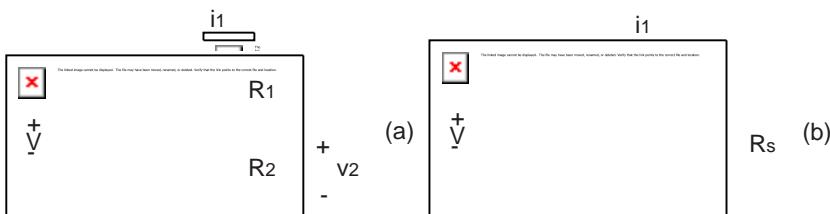


FIGURE 2.50 An intuitive way of analyzing the voltage divider circuit.

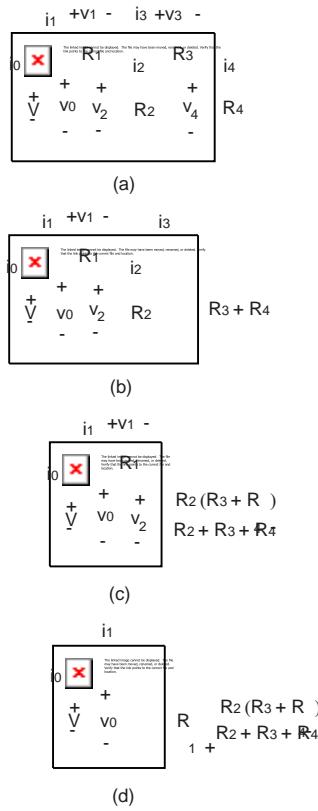


FIGURE 2.51 Collapsing the circuit.

It is worth dwelling on a couple of the “key moves” of our intuitive method. The basic approach is to first collapse, then expand. Notice that our first move was to collapse a set of resistances into a single equivalent resistance. Then, we found the current into the equivalent resistance. Finally, we took an expanded view of the two resistances to determine the specific voltage of interest.

Let us now use our intuition to develop an alternative method of analyzing the circuit in Figure 2.46 (repeated in Figure 2.51a for convenience). It will be obvious that the intuitive method is far less tedious than the rigorous application of the basic method in Section 2.3.

Our alternative analysis of the circuit in Figure 2.51a follows the two basic moves suggested earlier—first collapse, then expand. Accordingly, our analysis begins by collapsing the circuit using the equivalence of parallel and series resistors. This process is illustrated in Figure 2.51. Note that all branch variables that can be preserved during this collapse are shown in Figure 2.51. First, the series resistors R_3 and R_4 are combined to yield the circuit in Figure 2.51b. Next, R_2 is combined in parallel with the series equivalent of R_3 and R_4 to yield the circuit in Figure 2.51c. Finally, the two remaining series resistors are combined in series to yield the circuit in Figure 2.51d.

We now analyze our collapsed circuit in Figure 2.51d. Trivially, we know that

$$V_0 = V$$

and

$$i_0 = -i_1.$$

Now, following the results of Section 2.3.1, or equivalently by applying Ohm’s law directly, we know that

$$i_1 = \frac{V}{R_1 + \frac{R_2(R_3 + R_4)}{R^2 + R^{\frac{3}{2}}R}}$$

Thus, at this point, i_0, V_0 , and i_1 are known.

Our intuitive analysis concludes by expanding the circuit in Figure 2.51d progressively. As we expand, we determine the values of as many of the variables as we can in terms of previously computed variables. Following this process, first, the circuit in Figure 2.51c can be viewed as a voltage divider of V_0 . In other words, i_1 can be multiplied by each of its two resistances to determine V_1 and V_2 . Thus,

$$V_1 = \frac{R_1}{R_1 + \frac{R_2(R_3 + R_4)}{R^2 + R^{\frac{3}{2}}R}}$$

and

$$v_2 = V \cdot \frac{\frac{R_2(R_3+R_4)}{R^2+R^3R^4}}{R_1 + \frac{R_2(R_3+R_4)}{R^2+R^3R^4}}$$

Next, since v_2 is now known, R_2 and the series equivalent of R_3 and R_4 in Figure 2.51b can each be divided into v_2 to determine i_2 and i_3 . In other words,

$$i_2 = v_2 \cdot \frac{R_2}{R_3+R_4}$$

Alternatively, i_2 and i_3 can be determined by viewing R_2 and the series equivalent of R_3 and R_4 as a current divider of i_1 .

Finally, since i_3 is now known, R_3 and R_4 in Figure 2.51a can be reviewed as a voltage divider of v_2 , or they can be multiplied by $i_3 = i_4$ to determine v_3 and v_4 . Doing so yields

$$v_3 = i_3 R_3$$

and

$$v_4 = i_3 R_4.$$

This completes the intuitive analysis of the circuit in Figure 2.51a. The important observation here is that the alternative approach to circuit analysis outlined in Figure 2.51 is considerably simpler than the direct approach.

example 2.24 circuit analysis simplification

As

another example of circuit analysis simplification, consider the network of twelve resistors shown in Figure 2.52. Each resistor in the network has resistance R , and together the network outlines the shape of a cube. Additionally, the network has two terminals marked A and B, which extend from opposite corners of the cube to form a port. We wish to determine the equivalent resistance of the network as viewed through this port.

To determine the network resistance, we turn the network into a complete circuit by connecting a hypothetical current source to its terminals as shown in Figure 2.53. Note that the circuit in Figure 2.53 is now much the same as the circuit in Figure 2.25; the two circuits differ only in the complexity of the resistive network across the current source. Next, we compute the voltage across the port that appears in response to the application of the current source. The ratio of this voltage to the source current is the equivalent resistance of the network as viewed through the port. Note that this procedure does work as desired for the circuit in Figure 2.25 since the division of Equation 2.22 by $I = R$ yields $v_2/I = R$.

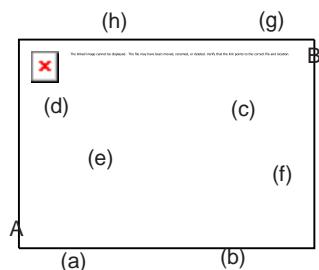


FIGURE 2.52 A cubic resistive network.

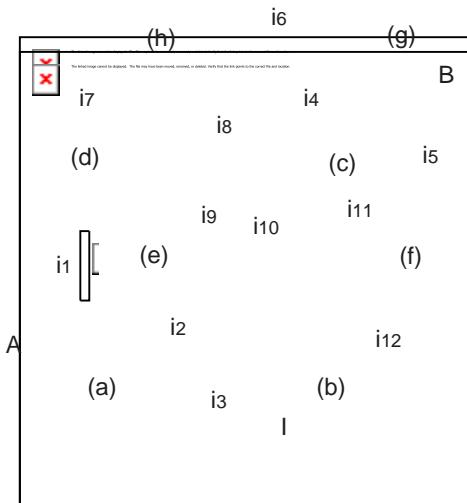


FIGURE 2.53 Introducing a current into the A–B terminal pair of the cubic network.

Turning now to the analysis of the circuit in Figure 2.53, we see that it involves the determination of 26 branch variables, which seems like a painful task. Fortunately, this analysis can be greatly simplified by taking advantage of the symmetry of the circuit, and that is the primary observation to be made here. As a consequence of the symmetry of the circuit, the three branch currents i_1 , i_2 , and i_3 are identical, as are the three branch currents i_4 , i_5 , and i_6 . Further, KCL applied to the two nodes at the port terminals shows that the sum of each group of three branch currents is 1, so all six branch currents equal $1/3$.

Next, again due to the symmetry of the circuit, the six branch currents i_7 through i_{12} are all identical. Further, KCL applied to any interior nodes shows that these six branch currents also equal $1/6$. Now, all branch currents in the circuit are known.

So, through the element laws, the branch voltages across all twelve resistors are known, leaving the branch voltage across the current source as the only remaining unknown. Finally through the application of KVL around any loop that passes through the current source we see that its branch voltage is $5R/12$. Dividing this voltage by $5R/6$ yields $5R/6$ as the equivalent resistance of the cubic network of resistors.

While this solution yields an interesting result, the more important observation is the importance of simplifying a circuit, in this case through symmetry, before attempting its analysis.

example 2.25 resistance of a cubic network

An

alternative method for determining the equivalent resistance of the cubic network in Figure 2.52 that uses series-parallel simplifications is now shown. Also suppose that each of the resistors in the network in Figure 2.52 has a resistance of $1\text{k}\Omega$. Our goal

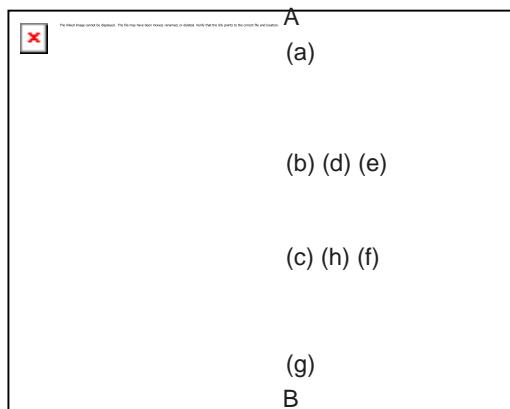


FIGURE 2.54 Simplified network.

is to find the equivalent resistance of this resistive network when looking into the A – B terminal pair.

First, observe the symmetry property of this resistive network. From many of the eight vertices, the network looks identical, and therefore, the resistance between any pair of vertices connected by the solid diagonal (for example, (a)-(g), (b)-(h), (e)-(c), etc.) is the same. Furthermore, looking into A, the set of paths from A to B starting along the edge (a)-(d) are matched by a set of paths starting along the edge (a)-(b), or by a set of paths starting along the edge (a)-(e). Therefore, when we apply a current i_1 as shown in Figure 2.53, it must split evenly into i_1 , i_2 , and i_3 . Likewise, it draws current off the network evenly, that is, i_4 , i_5 , and i_6 are the same. Since the same current and resistance cause the same voltage drop across the resistors, we conclude that nodes (b), (d), and (e) have the same voltage, and nodes (h), (c), and (f) also have the same voltage with respect to any reference node.

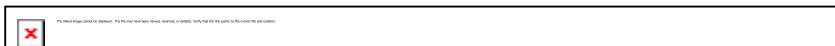
Notice that if we connect nodes with identical voltages by an ideal wire it does not draw any current and does not change the behavior of the circuit. Therefore, for the purpose of computing the resistance, we can connect all nodes with identical voltages, and simplify the network to the one shown in Figure 2.54.

We can now apply your series and parallel rules to determine the equivalent resistance as

$$1k \parallel 1k \parallel 1k \parallel 1k \parallel 1k \parallel 1k \parallel 1k \parallel 1k$$

which equals

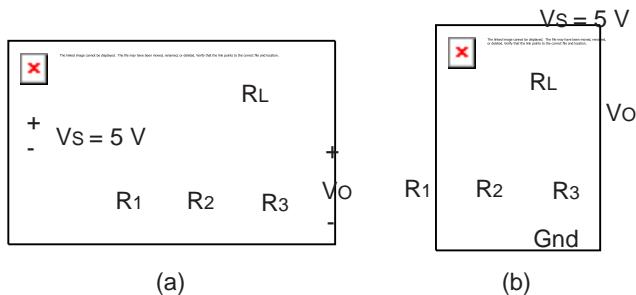
$$\frac{1}{\frac{1}{1k} + \frac{1}{1k} + \frac{1}{1k}} + \frac{1}{\frac{1}{1k} + \frac{1}{1k} + \frac{1}{1k}} + \frac{1}{\frac{1}{1k} + \frac{1}{1k} + \frac{1}{1k}} = \frac{5}{6} k.$$



example 2.26 resistor ratios

Consider the more involved voltage-divider circuit in Figure 2.55a. The voltage source represents a battery that

FIGURE 2.55 Resistor circuit:
(a) more complex voltage-divider circuit; (b) shorthand notation.



is supplying power to the rest of the circuit. Further, assume that the voltage V_o is of interest to us. Notice also that the two voltages V_s and V_o share a common negative reference node. A power supply voltage source and a common voltage reference will be encountered so commonly in our circuit language that it is worth creating an idiomatic representation for them.

Figure 2.55b introduces our shorthand notation. First, batteries that serve as power supplies are often not shown explicitly and use the upwards pointing arrow notation instead. V_s represents the power supply voltage. Often, we are also interested in measuring voltages with respect to a common reference node, termed the ground node. This node is represented with an upside-down "T" symbol as shown in the figure. The polarity symbols corresponding to voltages that are referenced from this node are not shown explicitly. Rather, the negative symbol is associated with the ground node and the plus symbol is associated with the node adjacent to which the voltage variable appears.⁴

Now, referring to Figure 2.55b, suppose $R_1 = R_2 = R_3 = 10\text{ k}$, how do we choose R_L such that $V_o \leq 1\text{ V}$?

The equivalent resistance of the three resistors in parallel is given by Equation 2.98. Thus,

$$R_{eq} = 10\text{ k} \parallel 10\text{ k} \parallel 10\text{ k} = \frac{10}{3}\text{ k.}$$

Using the voltage divider relationship, we require that

$$V_o = \frac{R_{eq}}{R_L + R_{eq}} < 1,$$

which implies that R_L has to be at least four times as large as R_{eq} . In other words

$$R_L > \frac{40}{3}\text{ k.}$$

⁴Chapter 3 will discuss the concepts of ground nodes as well as node voltages in more detail.

2.5 MORE CIRCUIT EXAMPLES

Let us now return to applying the basic method to several other circuits. Consider, for example, the circuit in Figure 2.56, which we will see again in Chapter 3. What is new about this circuit is that it contains two sources. It is not amenable to the intuitive method discussed in Section 2.4. Nonetheless, it can be analyzed by the basic approach presented in Section 2.3.

The element laws for this circuit are

$$v_0 = V \quad (2.139)$$

$$v_1 = R_1 i_1 \quad (2.140)$$

$$v_2 = R_2 i_2 \quad (2.141)$$

$$i_3 = -I \quad (2.142)$$

Next, the application of KCL to the two upper nodes yields

$$i_0 = -i_1 \quad (2.143)$$

$$i_1 = i_2 + i_3 \quad (2.144)$$

and the application of KVL to the two internal loops yields

$$v_0 = v_1 + v_2 \quad (2.145)$$

$$v_2 = V_3. \quad (2.146)$$

Finally, Equations 2.139 through 2.146 can be solved to yield

$$-i_0 = i_1 = -\frac{R_2}{R_1 + R_2} I + \frac{1}{R_1 + R_2} V \quad (2.147)$$

$$i_2 = \frac{R_1}{R_1 + R_2} I + \frac{1}{R_1 + R_2} V \quad (2.148)$$

$$i_3 = -I \quad (2.149)$$

$$v_0 = V \quad (2.150)$$

$$v_1 = -\frac{R_1 R_2}{R_1 + R_2} I + \frac{R_1}{R_1 + R_2} V \quad (2.151)$$

$$v_2 = v_3 = \frac{R_1 R_2}{R_1 + R_2} I + \frac{R_2}{R_1 + R_2} V \quad (2.152)$$

to complete the analysis.

What is most interesting about the results of this analysis is that each branch variable in Equations 2.147 through 2.152 is a linear combination of

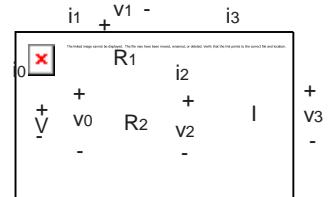


FIGURE 2.56 A circuit with two independent sources.

at term proportional to i_0 and a term proportional to V_0 . This suggests that we could analyze the circuit first with $V_0 = 0$ and second with $i_0 = 0$, and then combine the two analyses to obtain Equations 2.147 through 2.152. This is in fact possible, and it leads to yet further analysis simplifications as we shall see in Chapter 3.

Let us now practice the basic method on several other examples.

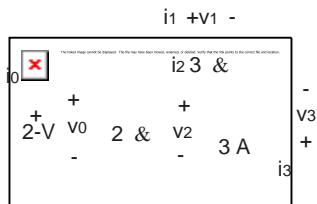


FIGURE 2.57 Another circuit with two independent sources.

example 2.27 circuit with two independent sources

Analyze the circuit in Figure 2.57 using the basic method. Further, show that energy is conserved in the circuit.

The branch variable assignments are shown in the figure. The element laws for this circuit are

$$v_0 = 2V$$

$$v_1 = 3i_1$$

$$v_2 = 2i_2$$

$$i_3 = 3A.$$

Applying KCL to the two upper nodes gives us

$$i_0 + i_1 + i_2 = 0$$

$$i_1 = -i_3.$$

Applying KVL to the two internal loops yields

$$v_0 = v_2$$

$$v_2 = -v_3 + v_1.$$

Solving the preceding eight equations, we get $v_0 = 2V$, $v_1 = -9V$, $v_2 = 2V$, $v_3 = -11V$, $i_0 = 2A$, $i_1 = -3A$, $i_2 = 1A$, and $i_3 = 3A$.

To show that energy is conserved, we need to compare the power dissipated by the resistors and the power generated by the sources. The power into the resistors is given by

$$(-9V) \times (-3A) + (2V) \times (1A) = 29W.$$

The power into the sources is given by

$$(2V) \times (2A) + (-11V) \times (3A) = -29W.$$

It is easy to see that the power dissipated by the resistors equals the power generated by the sources. Thus, energy is conserved.

example 2.28 basic circuit analysis method


The circuit diagram cannot be displayed. The file may have been moved, renamed, or deleted. Verify that the file exists in the correct file and location.

example 2.29 determining the $i - v$ characteristics of a circuit Determine the $i - v$ relationship for the two-terminal devices shown in Figure 2.61a. Make a sketch of the $i - v$ relationship for $R = 4$ and $V = 5V$. As shown in the figure, assume that the internal of the device can be modeled as a voltage source in series with a resistor.

We will find the $i - v$ relationship of the device by applying some form of excitation to the device terminals and obtaining the relationship between the values of i and v . One of the simplest inputs we can apply is a current source providing a current i_{test} , as illustrated in Figure 2.61b. The figure also shows the assignment of branch variables.

We will proceed by solving for the branch variables, v_1, i_1, v_2, i_2, v_3 , and i_3 , and then obtain the $i - v$ relationship by expressing v and i in terms of the expressions for the branch variables. Using the basic method, we first write the element laws

$$v_1 = V$$

$$v_2 = i_2 R$$

$$i_3 = -i_{test}$$

Next, we apply KCL to the two upper nodes

$$i_1 = -i_2$$

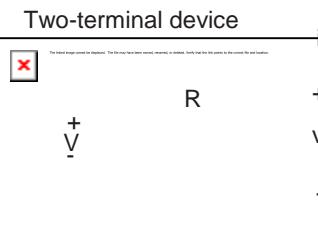
$$i_2 = i_3$$

and KVL to the loop

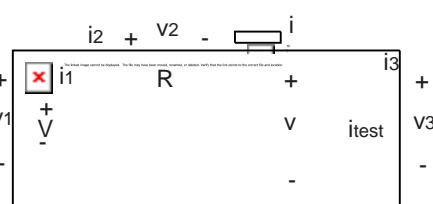
$$v_1 - v_3 - v_2 = 0.$$

These six equations can be solved to yield

$$i_1 = -i_2 = -i_3 = i_{test}$$



(a)



(b)

FIGURE 2.61 Determining the $i - v$ characteristics: (a) a two-terminal device; (b) assignment of branch variables to the circuit constructed to determine the $i - v$ characteristics of the device.

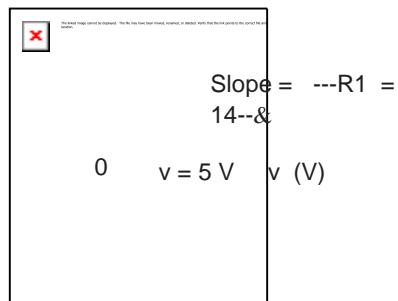


FIGURE 2.62 A plot of the $i-v$ characteristics for the device.

and

$$v_1=V, \quad v_2=-i_{\text{test}}R, \quad \text{and } v_3=V+i_{\text{test}}R.$$

We can now write the expression for v as

$$v=v_3=V+i_{\text{test}}R$$

and substituting $i=i_{\text{test}}$, we obtain the relationship between i and v as

$$v=V+iR.$$

In other words, the $i-v$ relationship is given by

$$i = \frac{v - V}{R}$$

Substituting $V=5$ volts and $R=4$, we get

$$i = \frac{v - 5}{4}$$

This relationship is plotted in Figure 2.62.

2.6 DEPENDENT SOURCES AND THE CONTROL CONCEPT

Section 1.6 introduced the voltage source and the current source as ideal models for energy sources. We call these independent sources because their values are independent of circuit operation. But many sources have values that are dependent on, that is, controlled by some other parameters in the system. For example, the accelerator pedal in an automobile controls the power delivered by the engine; the handle on a sink faucet controls the flow of water; and

room lights can be controlled by either a switch, a binary or two-state device, or a dimmer, a continuous control device. Chapter 6 will introduce another multi-terminal device called the MOSFET in which a control voltage between one pair of terminals of the device determines the MOSFET's behavior between another pair of terminals. Thus, when the multi-terminal dependent source is connected in a circuit, the behavior of the device can be controlled by a voltage or current in some other part of the circuit.

In the examples cited here, only a very small amount of power is needed to control large amounts of power at the output. In the car, for example, a trivial expenditure of energy controls hundredsof horsepower. To idealize, we assume that zero power is required to exercise control; we call this a dependent source or controlled source. The electrical forms of dependent sources are obvious extensions of the sources we have already seen: a dependent voltage source that can be controlled by some voltage or current, and a dependent current source which likewise has a value determined by some voltage or current. Dependent sources are most commonly used to model elements having more than two terminals.

Figure 2.63 shows an idealized voltage-controlled current source (VCCS). The device in the figure has four terminals. A pair of terminals serve as the control port and another pair of terminals are the output port. In many situations, the control port is also called the input port. Figure 2.63 shows a labeling of the branch variables at the output port v_{out} and i_{out} , and the branch variables at the input port v_{in} and i_{in} . The value of the voltage v_{in} across its control input port determines the value of the current i_{out} through its output port. In principle, such a dependent source can provide power, but for simplicity the power terminals inherent to the source are not shown.

The diamond shape of the symbol indicates that the device is a dependent source, and the arrow inside indicates that it is a current source. The direction of the arrow indicates the direction of the source current and the label next to the symbol indicates the value of the source current. In the example in the figure, the source current is some function of the voltage v_{in}

$$i_{out} = f(v_{in}).$$

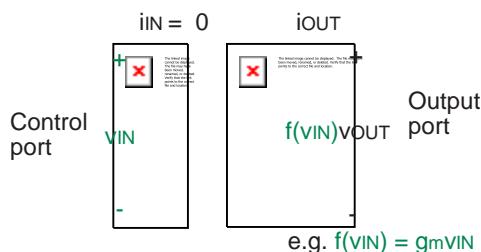


FIGURE 2.63 Voltage-controlled current source.

Whenthedeviceisconnectedinacircuit, v_{IN} mightbeanotherbranch voltageintheircircuit.

Weoftendealwithlineardependentsources.Alinearvoltage-controlled currentsourceischaracterizedbytheequation:

$$i_{OUT}=gV_{IN} \quad (2.173)$$

where g is a constant coefficient. When the dependent source is a voltage-controlledcurrentsource,thecoefficient g iscalledthetransconductancewith unitsofconductance. NoticethatEquation2.173istheelementlawforour dependentsourceexpressedasusualintervinuousofthebranchvariables. Wealsoneedtosummarizethebehavioroftheinputporttocompletelycharacterize thedependentsource. SinceouridealizedVCCSdoesnotrequireanypower tobesuppliedatitsinput, theelementlawfortheinputportissimply

$$i_{IN}=0 \quad (2.174)$$

whichissimplytheelementlawforaninfiniteresistance. Fortheidealdependent sourcesconsideredinthisbook, wewillassumethatthecontrolportsareideal, thatis, theydrawzeropower.

Figure2.64showsacircuitcontainingourdependentsource. Forclarity, thedependentsourcedeviceisshownwithinthedashedbox. Inthefigure, an independentvoltagesource(sourcingavoltage V)isconnectedtothecontrol portandaresistorisconnectedtotheoutputport. Fortheconnectionsshown, because

$$V_{IN}=V$$

theoutputcurrent*i_{OUT}*willbegimestheinputvoltage V . Wewillcomplete thefullanalysisofthecircuitshortly, andshowthatthepresenceofadependent sourcedoesnotalterthemannerinwhichourapproachtocircuitanalysis applied.

Figure2.65showsanothercircuitcontainingourdependentsource. Inthis circuit, thecontrolportisconnectedacrossaresistorwithresistance R_I . Accordingly, the voltage across R_I becomes the guiding voltage for the dependent source.

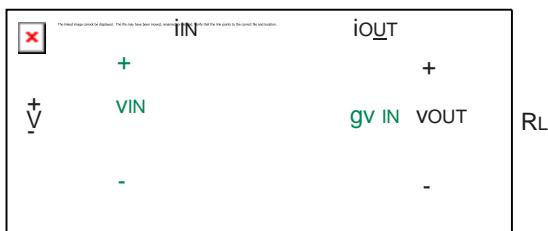


FIGURE 2.64 Acircuitcontainingavoltage-controlled currentsource.

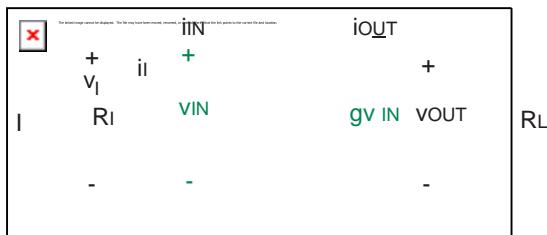


FIGURE 2.65 Another circuit containing a voltage-controlled current source.

Figure 2.66 illustrates the four types of linear dependent sources. Figure 2.66a depicts our now familiar voltage-controlled current source. Figure 2.66b depicts another type of dependent current source whose guiding variable is a branch current. This dependent source is called a current-controlled current source (CCCS).

The element law for the CCCS in Figure 2.66b is

$$i_{OUT} = a_{iIN}. \quad (2.175)$$

The unitless coefficient is referred to as a current transfer ratio. Furthermore, for a CCVS, $a_{iIN} = 0$.

Figures 2.66c and 2.66d depict the symbols for dependent voltage sources. A dependent voltage source supplies a branch voltage that is a function of some other signal within the circuit. Figure 2.66c shows a voltage-controlled voltage source (VCVS) and Figure 2.66d shows a current-controlled voltage source (CCVS). The guiding variable for a VCVS is a branch voltage, and that for a CCVS is a branch current. The diamond shape of their symbols again indicates that they are dependent sources, and the \pm inside indicates that they are voltage sources. The polarity the \pm indicates the polarity of the sourced voltage and the label next to the symbol indicates the value of the sourced voltage.

In the case of the VCVS in Figures 2.66c, the sourced voltage is equal to μV_{IN} , where V_{IN} is a voltage across another branch of the circuit and μ is a unitless coefficient. Thus, the element law for the VCVS in Figure 2.66 is

$$V_{OUT} = \mu V_{IN}. \quad (2.176)$$

The coefficient μ is referred to as a voltage transfer ratio. Furthermore, for a VCVS, $\mu = ca_0$. In the CCVS in Figures 2.66d, the sourced voltage is equal to r_{iIN} , where i_{IN} is the current through another branch of the circuit and r is a coefficient having the units of resistance. Thus, the element law for the CCVS in the figure is

$$V_{OUT} = r_{iIN}. \quad (2.177)$$

The coefficient r is referred to as a transresistance.

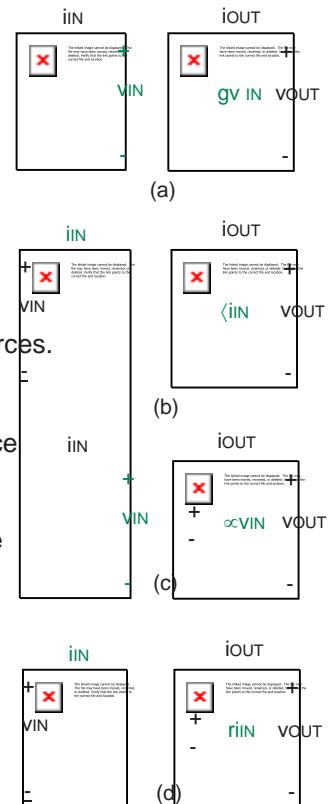


FIGURE 2.66 Four types of dependent sources: (a) VCCS (voltage-controlled current source); (b) CCCS (current-controlled current source); (c) VCVS (voltage-controlled voltage source); (d) CCVS (current-controlled voltage source).

Finally, for both the dependent current source and the dependent voltage source it is once again important to distinguish between the symbols that define them (e.g., g) and the branch variables that are defined (e.g., V_{IN} , i_{IN} , V_{OUT} , and i_{OUT}) in order to express the element laws. In particular, the branch variable definitions may be reversed for convenience, which will lead to a negation of the corresponding element laws.

2.6.1 CIRCUITS WITH DEPENDENT SOURCES

Let us now return to the analysis of our circuit in Figure 2.64, which contains a dependent voltage source. Nonetheless, the circuit can be analyzed by the basic approach presented in this chapter.

Figure 2.67 shows an assignment of the branch variables. The branch variables include v_0 , i_o , V_{IN} , i_{IN} , V_{OUT} , i_{OUT} , V_R , and i_R .

The element laws for this circuit are

$$v_0 = V \quad (2.178)$$

$$i_{IN} = 0 \quad (2.179)$$

$$V_R = R_L i_R \quad (2.180)$$

$$i_{OUT} = g V_{IN}. \quad (2.181)$$

Next, the application of KCL to the two upper nodes yields

$$i_o = -i_{IN} \quad (2.182)$$

$$i_{OUT} = -i_R \quad (2.183)$$

and the application of KVL to the two loops yields

$$v_0 = V_{IN} \quad (2.184)$$

$$V_R = V_{OUT} \quad (2.185)$$

FIGURE 2.67 Assignment of branch variables.



Finally, Equations 2.178 through 2.185 can be solved for the branch variables to yield

$$i_0 = i_{IN} = 0 \quad (2.186)$$

$$v_0 = V_{IN} = V \quad (2.187)$$

$$i_{OUT} = -i_R = -gV \quad (2.188)$$

$$v_R = v_{OUT} = -gV_{RL} \quad (2.189)$$

to complete the analysis.

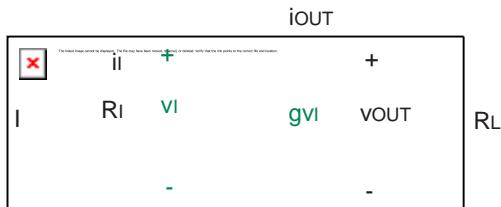
The presence of the dependent source in the circuit in Figure 2.67 does not alter the manner in which our approach to circuit analysis is applied. While this is an important observation, there is arguably a more important observation concerning the analysis of the dependent-source circuit, namely that it can proceed in stages. That is, it is possible to first analyze the operation of the “input side” of the circuit, that is, the independent voltage source and the input of the dependent source, and then separately analyze the operation of the “outside,” that is, the dependent current source and the resistor R_L . We will term this approach the sequential approach to circuit analysis.

To see this, observe that the equations representing the input side of the circuit, namely, Equations 2.178, 2.179, 2.182, and 2.184 can be solved trivially by themselves to yield the values of v_0 , i_0 , V_{IN} , and i_{IN} (see Equations 2.186 and 2.187).

Then, with V_{IN} treated as a known signal, the equations representing the output side of the circuit, namely Equations 2.180, 2.181, 2.183, and 2.185, can be solved by themselves to yield the values of v_{OUT} , i_{OUT} , v_R , and i_R (see Equations 2.188 and 2.189)—a result that is identical to that obtained for the circuit in Figure 2.25.

At this point you are probably wondering why it is that we were able to adopt such a sequential approach to analyzing the circuit in Figure 2.67. The same sequential approach does not work for the circuit in Figure 2.46. The intuition behind this useful property is that our idealized dependent source has decoupled the circuit into two parts—an input part and an output part. Because our dependent source model has an open circuit at its terminals marked by the branch voltage V_{IN} , the behavior of the input part is completely independent of the output part of the circuit. In other words, in determining the behavior of the input part, it is as if the output did not even exist. The output part, however, does depend on one of the input variables, namely, V_{IN} . However, once the value of the control input V_{IN} is determined through an analysis of the input part, it fixes the value of the dependent source. Thus, the dependent source can be treated as an independent source for the purpose of analyzing the output part.

FIGURE 2.68 The input port of an idealized dependent source is not shown explicitly.



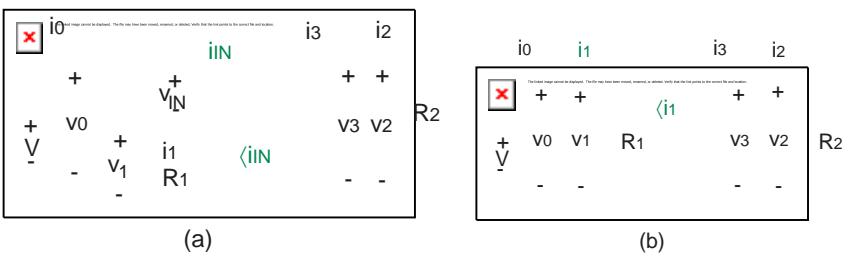
Such a sequential approach to circuit analysis is commonly applied to circuits involving dependent sources, when the circuit does not introduce any external coupling between the control port and the output port of the dependent sources. We will use this approach to advantage in future chapters.

The analysis of circuits with idealized dependent sources admits one other simplification. In an idealized dependent source, the input port (or control port) is an open circuit if the guiding variable is a voltage. Similarly, the input is a short circuit if the guiding variable is a current. Thus, the presence of the input port does not really affect the behavior of the input part of the circuit. The idealized input port is simply present to sample the value of a branch current or voltage without changing the value of the existing branch variable. Therefore, we do not really need to show the input port of the dependent source explicitly, thereby reducing the number of branch variables that we have to deal with.

For example, the input port of the dependent source marked with the branch variables v_{IN} and i_{IN} in Figure 2.65 is an open circuit. Accordingly, $i_{IN} = 0$ and $v_{IN} = v_I$, the voltage across the resistor R_1 . Therefore, we can equivalently use the circuit in Figure 2.68, where the input port of the dependent source is not shown explicitly, and the current sourced by the dependent source is specified directly in terms of v_I , the voltage across the resistor R_1 . We have thus eliminated the branch variables v_{IN} and i_{IN} from our analysis.

As depicted in Figure 2.69, the same simplification can be made for a dependent source in which the guiding branch variable is a current. Figure 2.69a shows a circuit containing a current-controlled current source with the control port marked and all branch variables labeled explicitly. Figure 2.69b shows the

FIGURE 2.69 Simplifying a circuit with a dependent source by not showing the control port explicitly: (a) with control port marked and branch variables labeled explicitly; (b) with simplification.



same circuit after making the simplification, where the source current is now specified in terms of i_1 . Notice that there is a lot less clutter in the latter figure.

example 2.30 current-controlled current source

Consider next the circuit shown in Figure 2.69b. This circuit contains a dependent current source. Notice that we have applied a simplification suggested earlier by not showing the control port of the dependent source explicitly. The current sourced by the dependent source is guided by the current i_1 .

Let us now analyze this circuit. The branch variables are assigned as shown in Figure 2.69b.

The element laws for this circuit are

$$v_0 = V \quad (2.190)$$

$$v_1 = R_1 i_1 \quad (2.191)$$

$$v_2 = R_2 i_2 \quad (2.192)$$

$$i_3 = -\alpha i_1. \quad (2.193)$$

Next, the application of KCL to the two upper nodes yields

$$i_0 + i_1 = 0 \quad (2.194)$$

$$i_2 + i_3 = 0 \quad (2.195)$$

and the application of KVL to the two loops yields

$$v_0 = v_1 \quad (2.196)$$

$$v_2 = v_3. \quad (2.197)$$

Finally, Equations 2.190 through 2.197 can be solved to yield

$$-i_0 = i_1 = \frac{V}{R_1} \quad (2.198)$$

$$-i_3 = i_2 = \frac{\alpha V}{R_1} \quad (2.199)$$

$$v_0 = v_1 = V \quad (2.200)$$

$$v_2 = v_3 = \frac{\alpha R_2 V}{R_1} \quad (2.201)$$

to complete the analysis.

example 2.31 intuitive sequential approach for the cccs Alternatively, we can solve the circuit in Figure 2.69 in a few lines if we use the intuitive sequential approach. Assume that we are interested in finding out the branch variables related to R_2 .

Using the sequential approach, first, let us tackle the input part of the circuit. Since the voltage V appears across R_1 , the current through R_1 is

$$i_1 = \frac{V}{R_1}$$

Now let us tackle the output part of the circuit. The current through the current source is in the same direction as i_2 , and so

$$i_2 = \alpha i_1 = \alpha RV.$$

Applying Ohm's law, we get

$$v_2 = \alpha \frac{VR_2}{R_1}$$

Not surprisingly, this result is the same as that in Equation 2.201.

example 2.32 branch variables Analyze the circuit in Figure 2.70 and determine the values of all the branch variables. Further, show that energy is conserved in the circuit.

We will analyze the circuit intuitively, applying element laws, KVL and KCL, using the sequential approach. Looking at the input side, since the voltage source appears across an open circuit, it is easy to see that both v_o and V_{IN} are two volts. Similarly, both i_o and i_{IN} are zero. Thus, we have determined all the branch variables at the input side.

Next, let us analyze the output part of the circuit. Since we know the value of V_{IN} , the current through the current source is determined as

$$0.001V_{IN} = 0.002A.$$

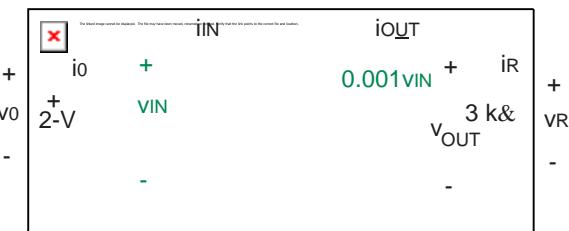


FIGURE 2.70 A circuit containing a voltage-controlled current source.

Since the current source current is in the same direction as i_{OUT} , and in the opposite direction as i_R , we obtain from KCL

$$i_{OUT} = 0.002A$$

and

$$i_R = -0.002A.$$

Finally, applying the element law for a resistor, we obtain

$$v_R = 3 \times 10^3 i_R = -6V$$

and from KVL, we obtain

$$v_{OUT} = v_R = -6V.$$

This completes our analysis, since all output side branch variables are also known.

To verify that energy is conserved in the circuit, we must show that the power dissipated by the elements is equal to the power supplied. Since the input side current is zero, there is no power dissipated or supplied at the input side. At the output side, the power dissipated in the 3-k resistor is given by

$$3kxi^2 = 0.012W.$$

The power into the dependent current source is given by

$$v_{OUT} \times i_{OUT} = -6 \times 0.002 = -0.012W.$$

In other words, the power supplied by the current source is 0.012W. Since the power supplied is equal to the power dissipated, energy is conserved.

More examples containing dependent sources are given in Section 7.2.

example 2.33 voltage-controlled resistor

2.7 A FORMULATION SUITABLE FOR A COMPUTER SOLUTION *

2.8 SUMMARY

KCL is a law stating that the algebraic sum of the currents flowing into any node in a network must be zero.

KVL is a law stating that the algebraic sum of the voltages around any closed path in a network must be zero.

A helpful mnemonic for writing KVL equations is to assign the polarity to a given voltage in accordance with the first sign encountered when traversing that voltage around the loop.

The following is the basic method (or fundamental method) or KVL/KCL method of solving networks:

1. Define voltages and currents for each element.
2. Write KVL.
3. Write KCL.
4. Write constituent relations.
5. Solve.

The series-parallel simplification method is an intuitive method of solving many types of circuits. This approach first collapses a set of resistances into a single equivalent resistance. Then, it successively expands the collapsed circuit and determines the values of all possible branch variables at each step.

The equivalent resistance for two resistors in series is $R_s = R_1 + R_2$.

The equivalent resistance of resistors in parallel is $R_p = \frac{R_1 R_2}{R_1 + R_2}$.

Voltage divider relation means that when two resistors with values R_1 and R_2 are connected in series across a voltage source with voltage V , the voltage across R_2 is given by $\frac{R_2}{R_1 + R_2} V$.

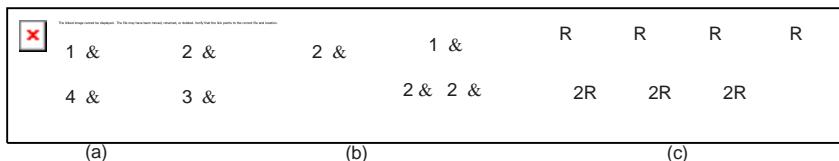
Current divider relation means that when two resistors with values R_1 and R_2 are connected in parallel across a current source with current I , the current through R_2 is given by $\frac{R_1}{R_1 + R_2} I$.

This chapter discussed four types of dependent sources: voltage-controlled current sources (VCCS), current-controlled current sources (CCCS), voltage-controlled voltage sources (VCVS), and current-controlled voltage sources (CCVS).

The sequential method of circuit analysis is an intuitive approach that can often be applied to circuits containing dependent sources when the control port of the dependent source is ideal. This approach first analyzes the circuit on the input side of the dependent source, and then separately analyzes the operation of the output side of the dependent source.

Conservation of energy is a powerful method for obtaining many types of results in circuits. Energy methods are intuitive and can often allow us to obtain powerful results without a lot of mathematical grunge. One energy approach equates the energy supplied by a set of elements in a circuit to the energy absorbed by the remaining set of elements in a circuit. Another energy approach equates the total amount of energy in a system at two different points in time (assuming that there are no dissipative elements in the circuit).

exercise 2.1 Find the equivalent resistance from the indicated terminal pair of the networks in Figure 2.72.



EXERCISES

FIGURE 2.72

exercise 2.2 Determine the voltages v_A and v_B (in terms of v_S) for the network shown in Figure 2.73.

exercise 2.3 Find the equivalent resistance between the indicated terminals (all resistances in ohms) in Figure 2.74.

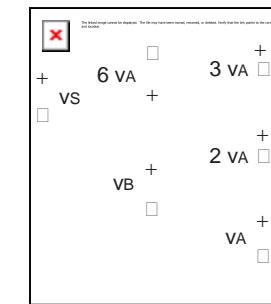
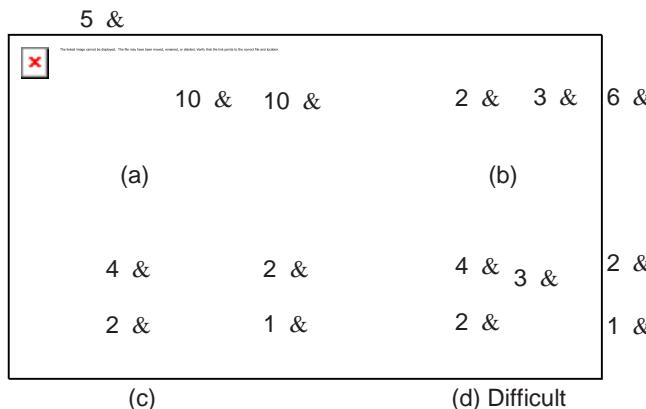


FIGURE 2.73

FIGURE 2.74

exercise 2.4 Determine the indicated branch voltage or branch current in each network in Figure 2.75.

exercise 2.5 Find the equivalent resistance at the indicated terminal pair for each of the networks shown in Figure 2.76.

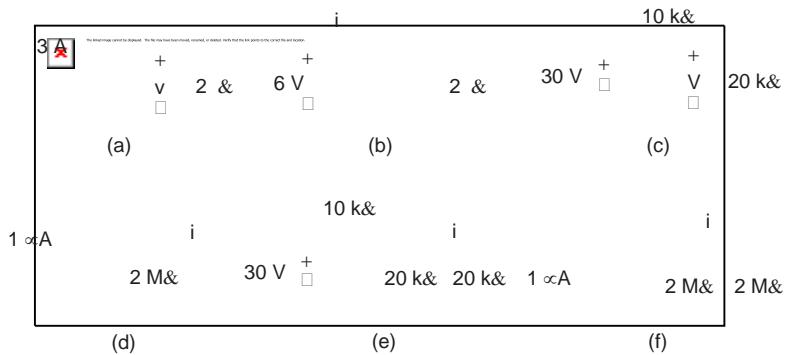


FIGURE 2.75

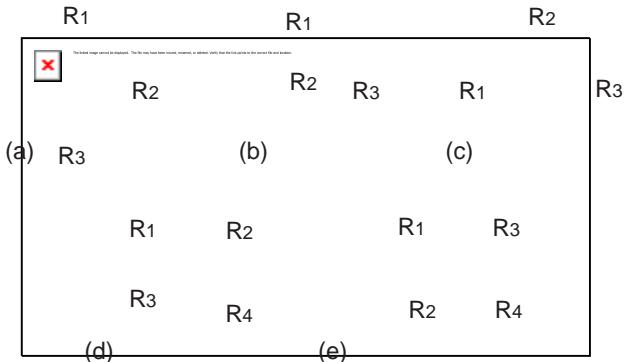


FIGURE 2.76

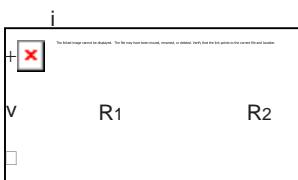


FIGURE 2.77

exercise 2.6 In the circuit in Figure 2.77, v, i , and R_1 are known. Find R_2 .

$$v=5\text{V}$$

$$i=40\mu\text{A}$$

$$R_1=150\text{k}$$

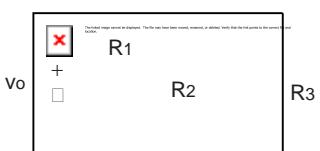


FIGURE 2.78

exercise 2.7 In the circuit in Figure 2.78, $v_o=6\text{V}$, $R_1=100$, $R_2=25$, and $R_3=50$. Which of the resistors if any, are dissipating less than $1/4\text{watt}$?

exercise 2.8 Sketch the $v-i$ characteristics for the networks in Figure 2.79. Label intercepts and slopes.

exercise 2.9

a) Assign branch voltages and branch current variable to each element in the network in Figure 2.80. Use associated referenced directions.

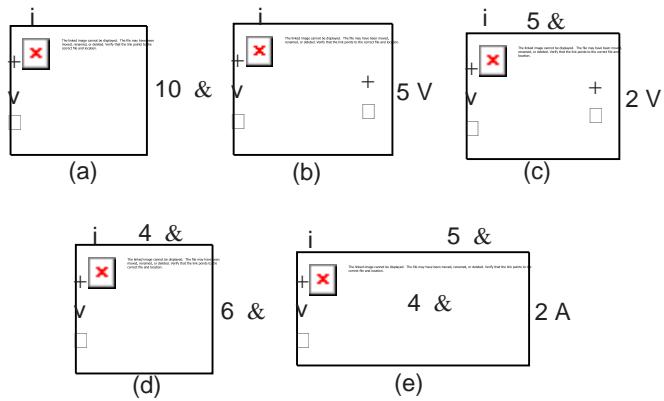


FIGURE 2.79

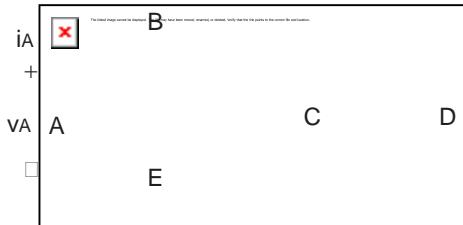


FIGURE 2.80

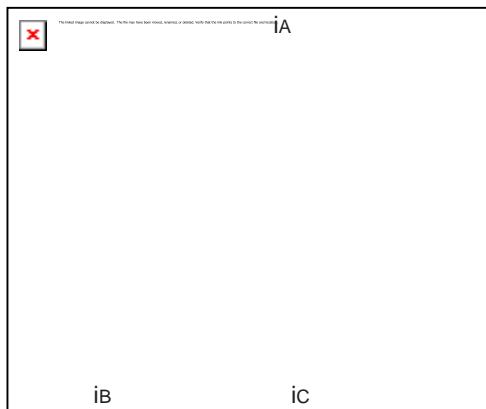
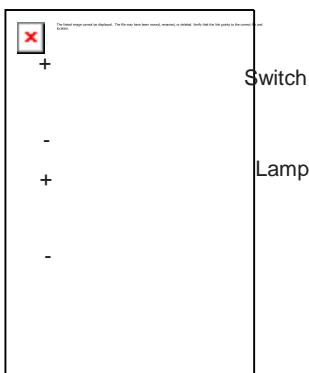
- How many linearly independent KVL equations can be written for this network?
- How many linearly independent KCL equations can be written for this network?
- Formulate a set of KVL and KCL equations for the network.
- Assign non-zero numbers to each branch currents such that your KCL equations are satisfied.
- Assign non-zero numbers to each branch voltages such that your KVL equations are satisfied.
- As a check on your result, you can draw on the fact that power is conserved in a network that obeys KVL and KCL. Therefore calculate the quantity v_{in} . It should be zero.

exercise 2.10 A portion of a larger network is shown in Figure 2.81. Show that the algebraic sum of the currents into this portion of the network must be zero.

problem 2.1 A pictorial diagram for a flashlight is shown in Figure 2.82. The two batteries are identical, and each has an open-circuit voltage of 1.5 V. The lamp

PROBLEMS

FIGURE 2.81



has a resistance of 5 when lit. With the switch closed, 2.5 V is measured across the lamp. What is the internal resistance of each battery?

problem 2.2 Determine the current i in the circuit in Figure 2.83 by working with resistors in series and parallel.

FIGURE 2.82

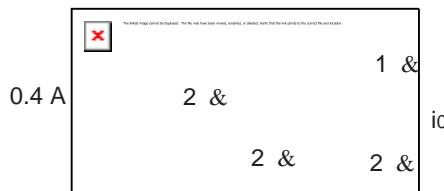
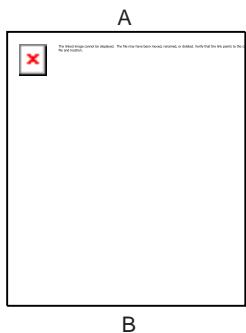


FIGURE 2.83

problem 2.3 Find the resistance between nodes A and B in Figure 2.84. All resistor values equal 1.

problem 2.4 For the circuit in Figure 2.85, find values of R_1 to satisfy each of the following conditions:

- a) $v=3V$
- b) $v=0V$
- c) $i=3A$
- d) The power dissipated in R_1 is $12W$.

FIGURE 2.84

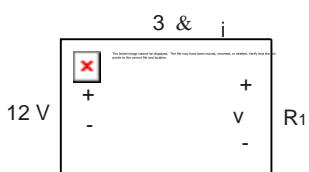
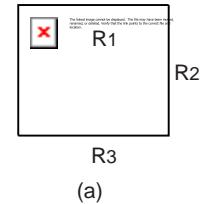
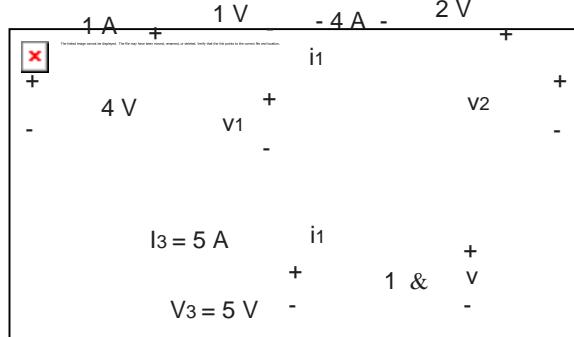


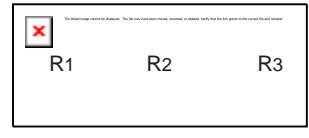
FIGURE 2.85

problem 2.5 Find the equivalent resistance R_T at the indicated terminals for each of the networks in Figure 2.86.

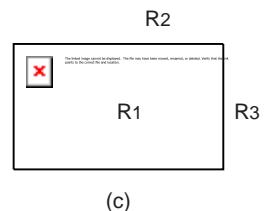
problem 2.6 In each network in Figure 2.87, find the numerical values of the indicated variables (units are amperes, volts, and ohms).



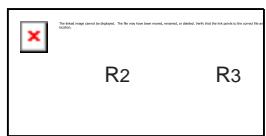
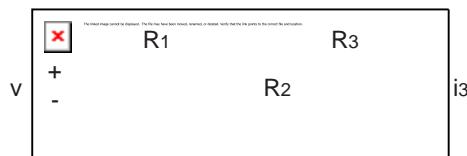
(a)



(b)



(c)

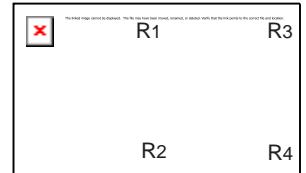
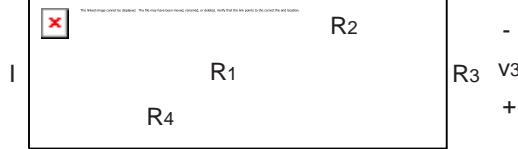


(d)

FIGURE 2.87

problem 2.7 For the circuit in Figure 2.88, determine the current i_3 explicitly in terms of all circuit parameters.

problem 2.8 Determine explicitly the voltage v_3 in the circuit in Figure 2.89.



(e)

FIGURE 2.89

problem 2.9 Calculate the power dissipated in the resistor R in Figure 2.90.

problem 2.10 Design a resistor attenuator to make $v_o = v_i/1000$, using the circuit configuration given in Figure 2.91, and resistor values available in your lab. This problem is underconstrained so it has many answers.

FIGURE 2.86

FIGURE 2.90

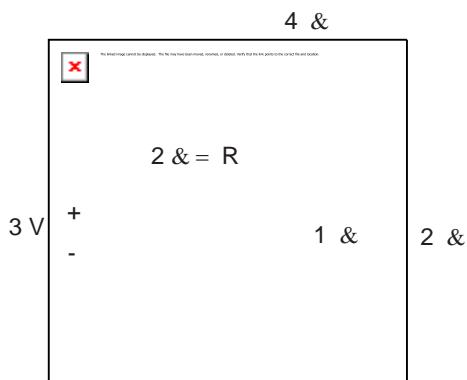


FIGURE 2.91

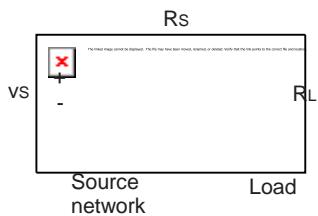
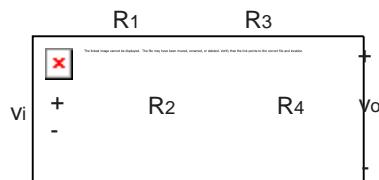
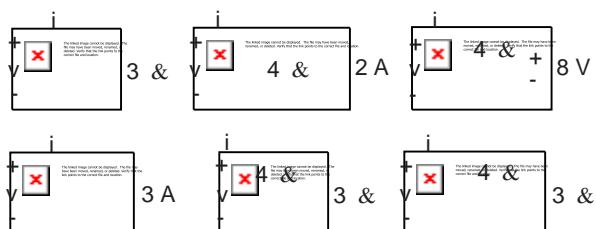


FIGURE 2.92

problem 2.11 Consider the network in Figure 2.92 in which a non-ideal battery drives a load resistor R_L . The battery is modeled as a voltage source V_s in series with a resistor R_s . The following are some proofs about power transfer:

- Prove that for R_s variable and R_L fixed, the power dissipated in R_L is maximum when $R_s=0$.
- Prove that for R_s fixed and R_L variable, the power dissipated in R_L is maximum when $R_s=R_L$ ("matched resistances").
- Prove that for R_s fixed and R_L variable, the condition that maximizes the power delivered to the load R_L requires that an equal amount of power be dissipated in the source resistance R_s .

FIGURE 2.93



problem 2.12 Sketch the characteristics for the networks in Figure 2.93. Label intercepts and slopes.

problem 2.13

- a) Find i_1, i_2 , and i_3 in the network in Figure 2.94. (Note that i_3 does not obey the standard convention for current direction.)
- b) Show that energy is conserved in this network.

problem 2.14 Assume that you have an arbitrary network of passive two-terminal resistive elements in which the $-v$ characteristic of each element does not touch either the v -axis or the i -axis, except that each $-v$ characteristic passes through the origin. Prove that all branch currents and branch voltages in the network are zero.

problem 2.15 Solve for the voltage across resistor R₄ in the circuit in Figure 2.95 by assigning voltage and current variables for each resistor.

problem 2.16 Find the potential difference between each of the lettered nodes (A,B,C, and D) in Figure 2.96 and ground. All resistances are in ohms.

problem 2.17 Find the voltage between node C and the ground node in Figure 2.97. All resistances are in ohms.

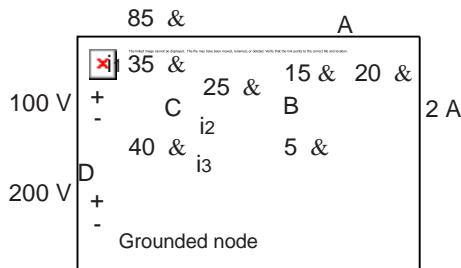


FIGURE 2.97

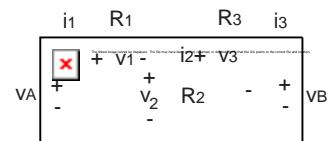


FIGURE 2.94

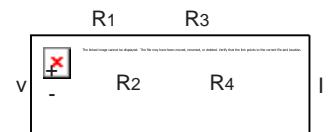


FIGURE 2.95

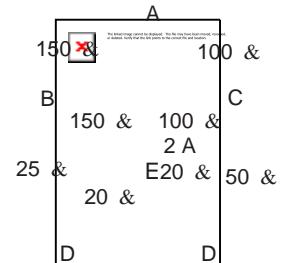
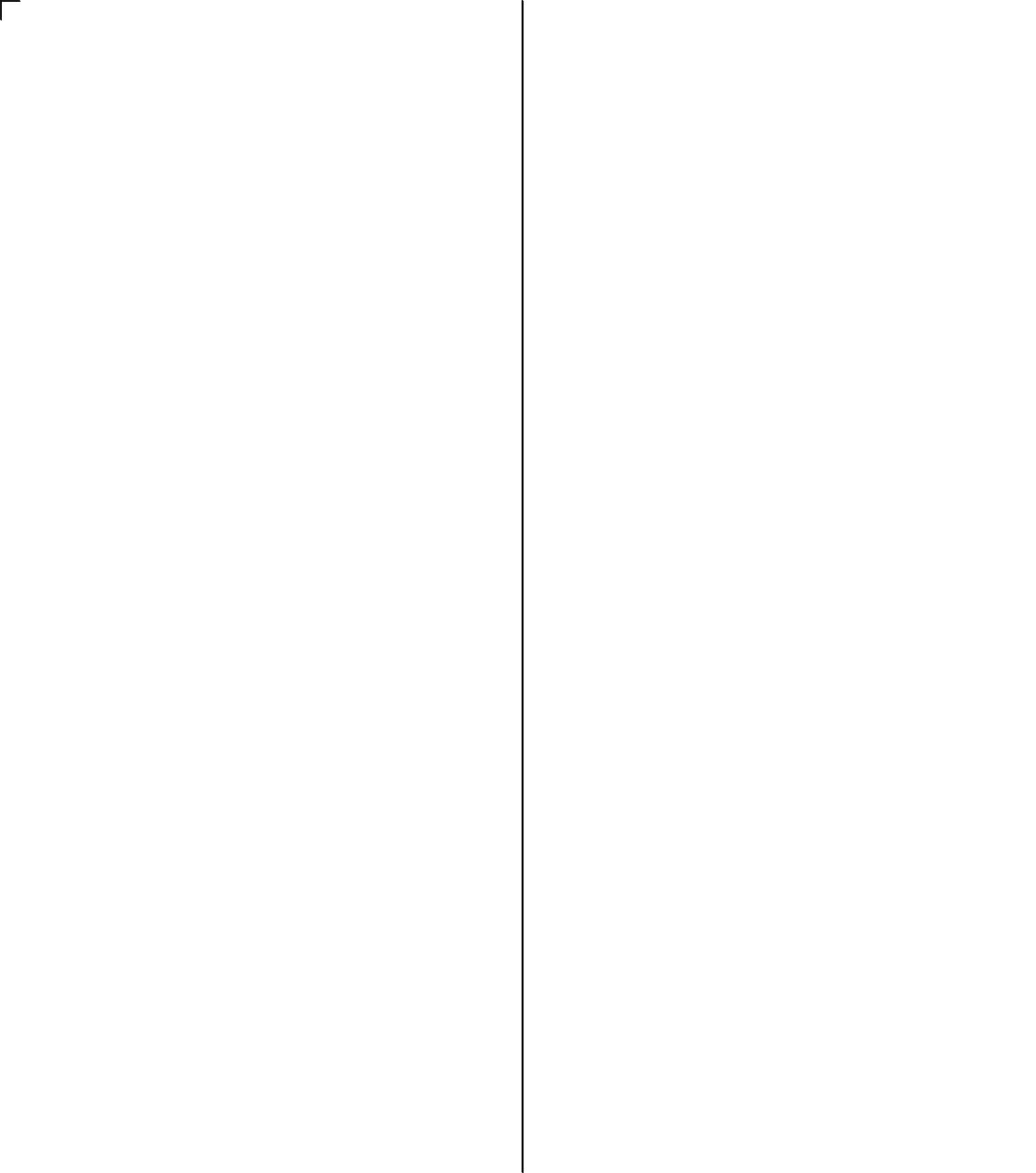
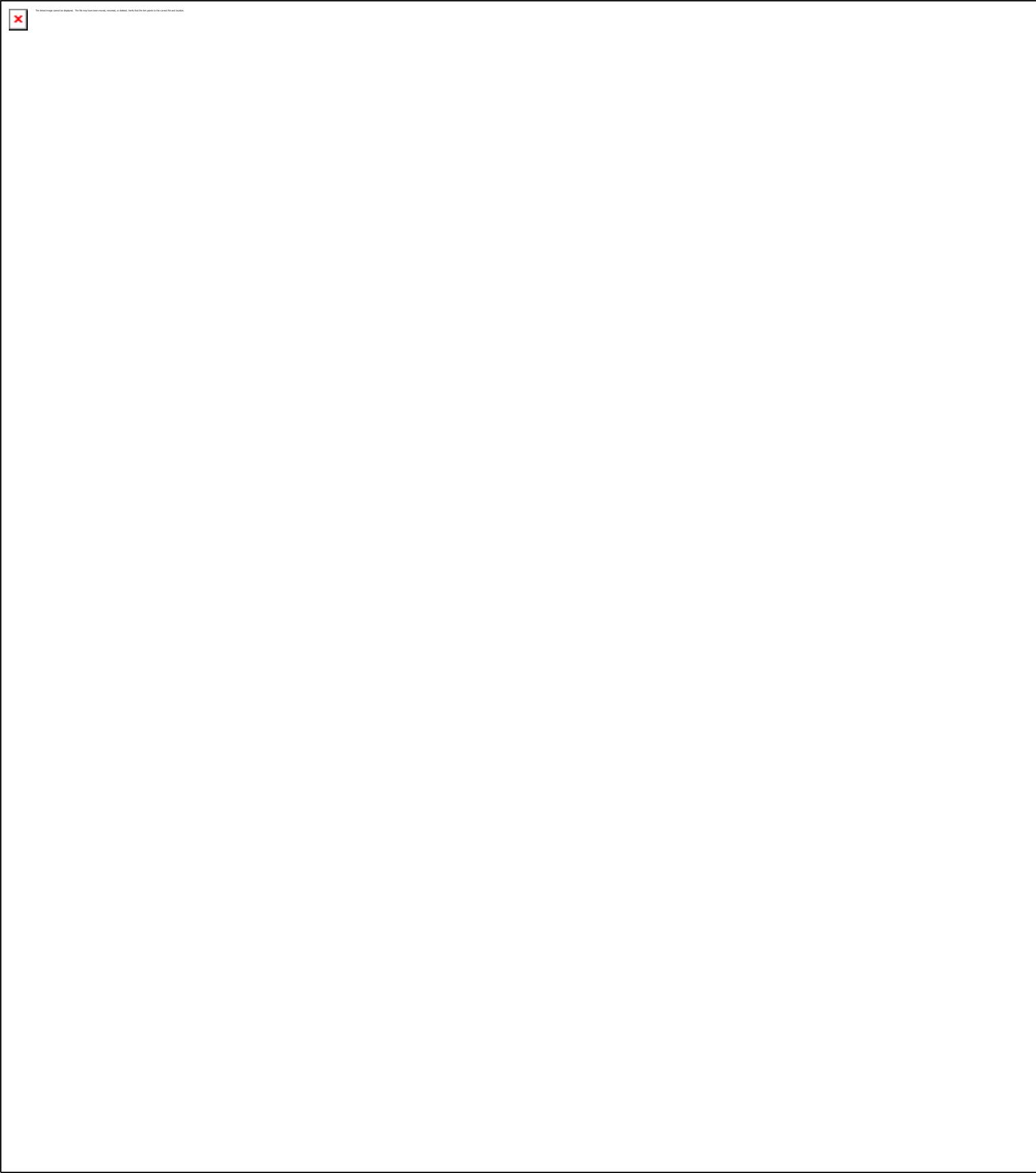


FIGURE 2.96



chapter 3

- 3.1 INTRODUCTION
- 3.2 THE NODE VOLTAGE
- 3.3 THE NODE METHOD
- 3.4 LOOP METHOD *
- 3.5 SUPERPOSITION
- 3.6 THÉVENIN'S THEOREM AND NORTON'S THEOREM
- 3.7 SUMMARY
- EXERCISES
- PROBLEMS



network theorems

3

3.1 INTRODUCTION

The basic network analysis method introduced in Chapter 2 is fundamental but unfortunately often insufficient. The problem is that frequently we deal with complicated circuits in which we are interested in relating only one output variable to one input variable. For example, in analyzing a high-fidelity audio amplifier, we might wish to find only the relationship between the voltage at the output terminals and the voltage at the input terminals. The intermediate voltage and current variables might be of no direct interest to us, yet by the analysis method of Chapter 2, we are forced to define all such variables, and then systematically eliminate them. Even worse, a circuit with N branches, each with its own voltage and current, will in general have $2N$ unknown branch variables. Thus, $2N$ equations must be solved simultaneously in order to complete the analysis. Even for a simple circuit, $2N$ can be an unwieldy number.

Fortunately, there exist better approaches to the organization of circuit analysis, and these approaches are the subject of this chapter. In this chapter, we develop a number of network theorems, all based on the fundamental methods of Chapter 2, which greatly simplify circuit analysis, and provide substantial insight about how circuits behave. These theorems also provide us with additional circuit vocabulary and a little more abstraction.

The first of these powerful techniques, called the node method, is fundamental and can be applied to any circuit, linear or nonlinear. The node method works with a set of variables called node voltages. So, before we present the node method, let us discuss the concept of node voltages, and build up our facility to work with them.

3.2 THE NODE VOLTAGE

In Chapters 1 and 2 we worked with branch voltages. A branch voltage is the potential difference across the element in a branch. In like manner, we can define an node voltage.

A node voltage is the potential difference between the given node and some other node that has been chosen as a reference node. The reference node is called the ground.

Current flows from the node with the higher potential to the node with the lower potential.

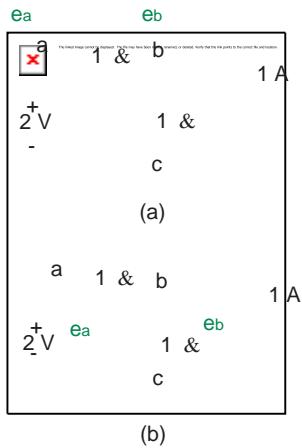


FIGURE 3.1 Ground node and node voltages.

Although the choice of reference node is in fact arbitrary, it is most convenient to choose the node that has the maximum number of circuit elements connected to it. The potential at this node is defined to be zero V, or ground-zero potential. In electrical and electronic circuits, this node will usually correspond to the “common ground” of the system, and is usually connected to the system chassis. Assigning zero potential to the ground node is permissible because elements respond only to their branch voltages and not to their absolute terminal voltages. Thus, an arbitrary constant potential may be uniformly added to all terminal voltages across the circuit thereby permitting any node to be selected as ground. Anode will have a negative voltage if its potential is lower than that of the ground node.

Figure 3.1a shows a circuit that we saw earlier in Chapter 2, and illustrates some new notation. Node c has been chosen as ground. The upside-down “T” symbol is the notation for the ground node. Nodes a and b are other nodes of this circuit. Their node voltages e_a and e_b are marked. Figure 3.1b illustrates that the node voltages are measured with respect to the ground node.

Now, let us practice working with node voltages. Figure 3.2 shows our circuit from Figure 3.1 with a known set of branch voltages and currents. Let us determine the node voltages e_a and e_b . The node voltage e_a is the potential difference between node a and node c . To find the potential difference, let us start at node c and work our way to node a accumulating potential differences along the path $c \rightarrow a$. Thus, starting at node c , we count an increase in potential of 2V as we traverse the voltage source and reach node a . Thus $e_a = 2V$.

Similarly, e_b is the potential difference between nodes b and c . Therefore, starting at node c and heading towards node b across the 1- resistor, we notice a potential increase of 1.5V. So $e_b = 1.5V$.

Notice that from KVL, a given node voltage should be the same irrespective of the path along which voltages are accumulated. Thus, let us confirm that the value of e_b that is obtained by taking the path $c \rightarrow a \rightarrow b$ is the same as that obtained by taking the direct path $c \rightarrow b$. Starting at c , we first accumulate the voltage of 2V as we cross the voltage source and reach node a . Then proceeding towards node b , we notice a 0.5V drop across the 1-resistor, resulting in a 1.5V value for e_b , as seen earlier.

As we will see shortly, the node method will determine all the node voltages in a circuit. Once node voltages are known, we can readily determine all the

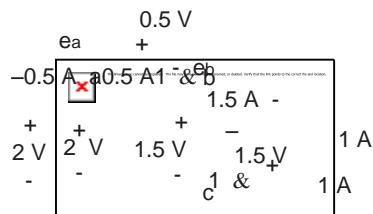


FIGURE 3.2 Determining the node voltages from the branch variables.

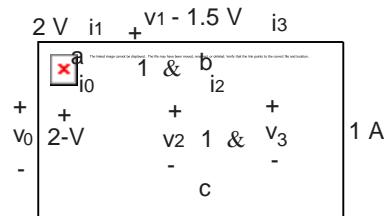


FIGURE 3.3 Determining the branch variable values from node voltages.

branch variables. As an example, Figure 3.3 shows our circuit from Figure 3.1 with a known set of node voltages. Let us determine the values of the branch variables.

Let us first determine the value of v_1 . The branch voltage v_1 is the potential difference between the nodes a and b . In other words,

$$v_1 = e_a - e_b = 2V - 1.5V = 0.5V.$$

We need to be careful with voltage polarities as we obtain branch voltages by taking the difference of a pair of node voltages. As depicted in Figure 3.4, the relationship between the branch voltage v_{ab} and node voltages v_a and v_b is given by

$$v_{ab} = v_a - v_b. \quad (3.1)$$

Intuitively, if $v_a > v_b$, then v_{ab} is positive when its positive polarity coincides with the node with voltage v_a .

Similarly, noting that the potential of the ground node is taken as 0V,

$$v_0 = e_a - e_c = 2V - 0V = 2V$$

and

$$v_2 = v_3 = e_b - e_c = 1.5V - 0V = 1.5V.$$

The branch currents are easily determined from the branch voltages and element laws as:

$$i_1 = \frac{v_1}{1} = 0.5A$$

$$i_2 = \frac{v_2}{1} = 1.5A$$

$$i_0 = -i_1 = -0.5A$$



FIGURE 3.4 Branch and node voltages for the element are related as $v_{ab} = v_a - v_b$.

and

$$i_3 = -1A.$$

example 3.1 node voltages Determine the node voltages corresponding to nodes c and b for the circuit in Figure 3.5. Assume that g is taken as the ground node.

Let v_c and v_b denote the voltages at nodes c and b, respectively. To find v_c , let us follow the path $g \rightarrow f \rightarrow c$. Accordingly, there is a $+1V$ increase in potential from g to f, and a further $-2V$ "increase" from f to c resulting in an accumulated potential of $-1V$ at c.

Thus $v_c = -1V$.

Similarly, because the potential at node b is $4V$ higher than that at node c, we get

$$v_b = 4V + v_c = 4V - 1V = 3V.$$



example 3.2 branch voltages Determine all the branch voltages for the circuit in Figure 3.6 when the node voltages are measured with respect to node e.

We find each of the branch voltages by taking the difference of the appropriate node voltages. Let us denote the voltage of node i as v_i :

$$v_1 = v_a - v_b = -1V$$

$$v_2 = v_b - v_e = 2V$$

$$v_3 = v_b - v_c = -1V$$

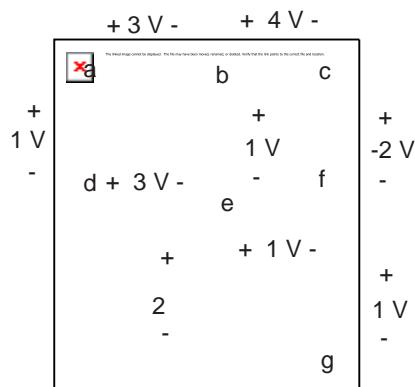


FIGURE 3.5 Circuit for determining node voltages.

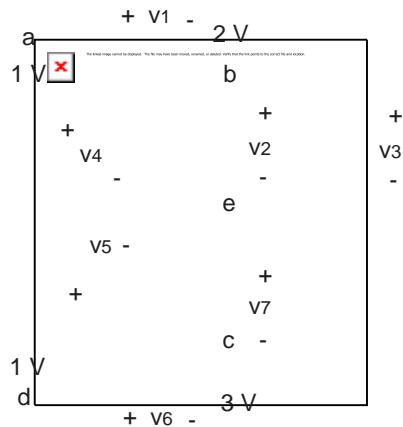


FIGURE 3.6 Circuit for determining branch voltages.

$$v_4 = v_a - v_e = 1V$$

$$v_5 = v_d - v_e = 1V$$

$$v_6 = v_d - v_c = -2V$$

$$v_7 = v_e - v_c = -3V.$$

Once all the branch voltages are known, the branch currents can readily be found from the branch voltages and the individual element laws. For example, if the element with the branch voltage v_1 is a resistor with resistance $1k$, then its branch current i_1 defined according to associated variables is given by

$$i_1 = \frac{v_1}{1k} = -1mA.$$

Thus far, in this section, we have shown that once the node voltages for a circuit are known, we can readily determine all the branch voltages by applying KVL, and then the branch currents from the branch voltages and element laws. Since we can determine branch currents from node voltages and element laws, we can also write KCL for each of the nodes in a network in terms of node voltages and the element parameters. Although our doing so appears unmotivated at this point, we will make use of this fact in node analysis in Section 3.3.

For example, consider the subcircuit shown in Figure 3.7. Let us write KCL for Node 0 directly in terms of the node voltages e_0 , e_1 , e_2 , e_3 , and e_4 , (defined with respect to some ground).

Let us start by determining the current through the resistance R_1 into Node 0. The branch voltage across the resistance R_1 is given by applying

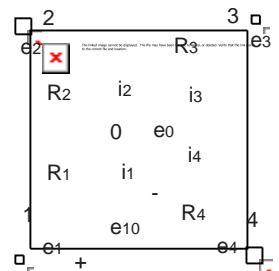


FIGURE 3.7 Circuit for writing KCL.

KVLs

$$e_{10} = e_1 - e_0$$

where the negative polarity of e_{10} is defined to be at Node 0. Thus, the current i_1 through the resistance R_1 into Node 0 is given by using the element law for resistors as

$$i_1 = \frac{e}{R_1}$$

In terms of the node voltages,

$$i_1 = \frac{e_1 - e_0}{R_1}$$

We can determine the currents into Node 0 through the other resistors in a similar manner:

$$i_2 = \frac{e_2 - e_0}{R_2}$$

$$i_3 = \frac{e_3 - e_0}{R_3}$$

$$i_4 = \frac{e_4 - e_0}{R_4}$$

We can now write KCL for Node 0 in terms of node voltages and element values as

$$\frac{e_1 - e_0}{R_1} + \frac{e_2 - e_0}{R_2} + \frac{e_3 - e_0}{R_3} + \frac{e_4 - e_0}{R_4} = 0. \quad (3.2)$$

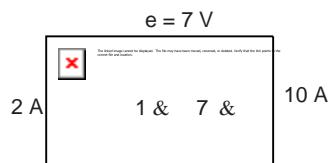


FIGURE 3.8 Satisfying KCL.

example 3.3 kcl Show that the node with voltage $e_0 = 7\text{ V}$ in Figure 3.8 satisfies KCL.

For KCL to be satisfied at the node with node voltage e_0 , the currents leaving the node must be zero. In other words

$$2A + \frac{(7-0)\text{V}}{1} + \frac{(7-0)\text{V}}{7} - 10A = 0$$

must be 0. It is easy to see that this expression equals 0, and so KCL is satisfied.

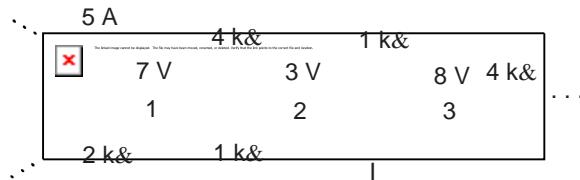


FIGURE 3.9 Portion of a circuit containing three nodes.

example 3.4 more kcl Figure 3.9 shows a portion of a circuit containing three nodes: 1, 2, and 3. The node voltages with respect to some ground are shown.

1. Write KCL for Node 2 in Figure 3.9 in terms of the node voltages and element values.
2. Determine the current through the current source.

KCL for Node 2 in terms of node voltages and element values is given by:

$$\frac{3V - 7V + 3V - 7V + 3V - 8V}{4k} + I = 0$$

Simplifying, we obtain $I = 10 \text{ mA}$.

In summary, a voltage is always defined as the potential difference between a pair of points—the two branch terminals for a branch voltage, and two nodes for a node voltage. Accordingly, voltage measurement instruments have two leads—one to connect to the node in question and one to the reference node or ground. Thus, when we refer to a node voltage, we are also making an implicit reference to a common ground node.

Interestingly, the significance of potential differences between pairs of nodes is easily illustrated with the example of a person hanging from a high voltage line. Although we do not recommend that you try this, a person hanging from a high voltage line is safe as long as no part of their body touches the ground. However, a deadly current would flow if the person were to touch the ground or another wire at a different potential.

Node voltages will be used in the next section as the variables in the node method. The node method will solve for the node voltages, which as we saw in this section, are sufficient to determine all the branch voltages and currents.

3.3 THE NODE METHOD

Perhaps the most powerful approach of circuit analysis is referred to as node analysis. Node analysis is based on the combination of element laws, KCL, and

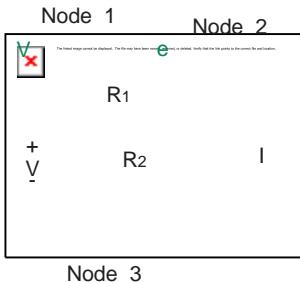


FIGURE 3.10 A resistive circuit.

KVL, just as was the basic approach presented in Chapter 2. Thus, it introduces no new physics, and it processes exactly the same information. However, node analysis organizes the analysis of a circuit in a manner that yields a relatively manageable problem, and this is what makes it particularly powerful.¹

Let us illustrate the method with an example. Suppose we wish to find the voltage across and the current through resistor R_1 in the circuit shown in Figure 3.10. Notice that the circuit in the figure is identical to the one we analyzed in Figure 2.56 using the basic method, and therefore node analysis of it must yield the results in Equations 2.151 and 2.147 for the branch voltage and current corresponding to R_1 . For node analysis, instead of defining voltage and current variables for each element in the network, we will choose node voltages as our variables.

As discussed in the previous section, since node voltages are defined with respect to a common reference, we first need to choose our reference ground node. While any node may be selected as the ground node, some nodes are more useful as ground nodes than others. Such useful nodes include those with the maximum number of circuit elements connected to it. Another useful ground node is one that connects to the maximum number of voltage sources. Sometimes the operation of a circuit may be more intuitively understood with a particular selection of the ground node. Alternatively, voltage measurements are often more easily or safely made with respect to a certain node and so that node might naturally be selected as the ground node.

One choice of ground node and a corresponding set of node voltages is defined in the figure. Node 3 is a good choice because it has three branches and it connects directly to the voltage source. Since the independent voltage source has a known voltage V , we can directly label the voltage of Node 1 as V using the element law for an independent voltage source. Thus, we have one unknown node voltage e . Because node voltages identically satisfy KVL, it is not necessary to write KVL. To demonstrate this point, let us write KVL around the loops. Doing so, we find

$$-V + (V - e) + e = 0 \quad (3.3)$$

$$-e + e = 0. \quad (3.4)$$

Both of these equations are identically zero for all values of the node voltage variables: As promised, this choice of voltage variables automatically satisfies KVL. So to solve the circuit it is not necessary to write KVL. Instead, we

1. While node analysis is generally quite simple, it is complicated by the presence of floating independent voltage sources and by the presence of dependent sources. Note that a floating independent voltage source is a source that has neither terminal connected to ground, neither directly nor through one or more other independent voltage sources. Consequently, we first introduce node analysis without these complications, and then treat these complications in succession.

will directly proceed with writing KCL equations. Furthermore, to save time the KCL equations can be written directly in terms of the node voltages and the resistors' values. Since we have only one unknown, e , we need only one equation. Hence, at Node 2,

$$\frac{e-V_2}{R_1} - \frac{e}{R_2} = I = 0. \quad (3.5)$$

Notice that the preceding step is actually two substeps bundled into one: (1) writing KCL in terms of currents and (2) substituting immediately node voltages and element parameters for the currents by using KVL and element laws. By doing these two substeps together, we have eliminated the need to define branch currents.

Note that in one step we have one unknown and one equation, whereas by the KVL and KCL method of Chapter 2 we would have written eight equations in eight unknowns. Further, note that both the device law for every resistor and all independent statements of KVL for the circuit have been used in writing Equation 3.5.

The voltage e can now be determined easily as

$$e = \frac{1}{R_1} + \frac{1}{R_2} = I + R_1 \frac{V}{e}. \quad (3.6)$$

It is wise to check dimensions at this point: Each term in this example should have the dimensions of current. Our equation can be somewhat simplified by rewriting in terms of conductance rather than resistance:

$$e(G_1 + G_2) = I + VG_1 \quad (3.7)$$

where $G_1 = 1/R_1$ and $G_2 = 1/R_2$. Simplifying further,

$$e = \frac{1}{G_1 + G_2} I + \frac{G_1}{G_1 + G_2} V. \quad (3.8)$$

In terms of resistances,

$$e = \frac{R_1 R_2}{R_1 + R_2} I + \frac{R_2}{R_1 + R_2} V. \quad (3.9)$$

Once we have determined the values of the node voltages, we can easily obtain the branch currents and voltages from the node voltages by using KVL and the constituent relations. For example, suppose we are interested only

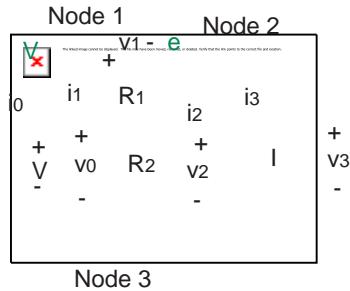


FIGURE 3.11 A resistive circuit.

$v_1 = V - e$, the voltage across R_1 , and i_1 , the current through R_1 , as illustrated in Figure 3.11. Then

$$v_1 = V - e = -\frac{1}{G_1 + G_2} 2i + \frac{G_2}{G_1 + G_2} V \quad (3.10)$$

and

$$i_1 = (V - e) G_1 = -\frac{G_1}{G_1 + G_2} 2i + \frac{G_1 G_2}{G_1 + G_2} V. \quad (3.11)$$

In terms of resistances, v_1 and i_1 are given by

$$v_1 = -\frac{R_1 R_2}{R_1 + R_2} 2i + \frac{R_1}{R_1 + R_2} V$$

and

$$i_1 = -\frac{R_2}{R_1 + R_2} 2i + \frac{1}{R_1 + R_2} V.$$

For completeness, let us go ahead and determine the other branch voltages and currents as well:

$$v_0 = V \quad (3.12)$$

$$v_2 = v_3 = e = -\frac{1}{G_1 + G_2} 2i + \frac{G_1}{G_1 + G_2} V \quad (3.13)$$

$$i_0 = -i_1 = \frac{G_1}{G_1 + G_2} i - \frac{\frac{G_1^2}{G_1 + G_2}}{V} \quad (3.14)$$

$$i_2 = e G_2 = \frac{G_2}{G_1 + G_2} 2i + \frac{G_1 G_2}{G_1 + G_2} V \quad (3.15)$$

$$i_3 = -I. \quad (3.16)$$

This completes the node analysis.

A comparison of the equations for the branch voltages and currents (Equations 3.10 through 3.16) with the corresponding Equations 2.147 through 2.152 in Chapter 2 shows that the node analysis has resulted in the same expressions for the branch variables as did the direct analysis presented. However, the node analysis is obtained from the results in a much simpler manner. The direct analysis of Chapter 2 involved the solution of eight simultaneous equations, namely Equations 2.139 through 2.146, while the node analysis involved the solution of only one equation, namely Equation 3.5, and the explicit back substitution of its solution.

In summary, the specific steps of the node method can be written as:

1. Select a reference node, called ground, from which all other voltages will be measured. Define its potential to be 0V.
2. Label the potentials of the remaining nodes with respect to the ground node. Any node connected to the ground node through either an independent or dependent voltage source should be labeled with the voltage of that source. The voltages of the remaining nodes are the primary unknowns and should be labeled accordingly. In this chapter we will denote the unknown node voltages by the symbol V . Since there are generally far fewer nodes than branches in a circuit, there will be far fewer primary unknowns to determine in a node analysis.
3. Write KCL for each of the nodes that has an unknown node voltage (in other words, the ground node and nodes with voltages sources connected to ground are excluded), using KVL and element laws to obtain the currents directly in terms of the node voltages and differences in element parameters. Thus, one equation is written for each unknown node voltage.
4. Solve the equations resulting from Step 3 for the unknown node voltages. This is the most difficult step in the analysis.
5. Back-solve for the branch voltages and currents. More specifically, use node voltages and KVL to determine branch voltages as desired. Then, use the branch voltages, the element laws, and KCL to determine the branch currents, again as desired.

At this point, it is instructive to make some general comments about the equations produced by the node method. Although the actual collection of conductance terms in Equation 3.8 is not particularly educational in this somewhat contrived example, the general form of the equation is useful. The right-hand side has two terms, one for each source, and these source terms enter the

equation assumes, and not products. Equations will always be of this form if the circuit is made up of linear elements. In fact, we use this property to define a linear network: A network is linear if the response to an input $ax_1 + bx_2$ is the same as a sum of the responses to x_1 alone plus b times the response to x_2 alone. That is, if $f(x)$ is the response to some excitation x , then the system is linear if and only if

$$f(ax_1 + bx_2) = af(x_1) + bf(x_2). \quad (3.17)$$

3.3.1 NODE METHOD: A SECOND EXAMPLE

As a second, and slightly more complex, example of node analysis, consider the circuit shown in Figure 3.12, which is the same as that shown in Figure 2.46 except for the addition of an independent current source. Specifically, suppose we wish to find the voltage across and the current through resistor R_3 .

The first two steps in its node analysis, namely the selection of a ground node and the labeling of its node voltages, are already complete. As shown in Figure 3.12, Node 4 is selected as the ground node, Node 3 is labeled with the known voltage V of the independent source, and Nodes 1 and 2 are relabeled with the unknown node voltages e_1 and e_2 , respectively. Node 4 is a good choice for the ground node because it joins the largest number of branches and connects directly to the voltage source.

Next, following Step 3, we write KCL for Nodes 1 and 2 in terms of the unknown node voltages. This yields

$$\frac{(V-e_1)+(e_2-e_1)}{R_3} - \frac{e_1}{R_2} = 0 \quad (3.18)$$

for Node 1, and

$$\frac{(e_1-e_2)}{R_3} - \frac{e_2}{R_4} + I = 0 \quad (3.19)$$

for Node 2.

Note that in one step we have generated two equations and two unknowns, whereas by the KV and KCL method of Chapter 2 we would have written twelve equations in twelve unknowns. The voltages e_1 and e_2 can now be

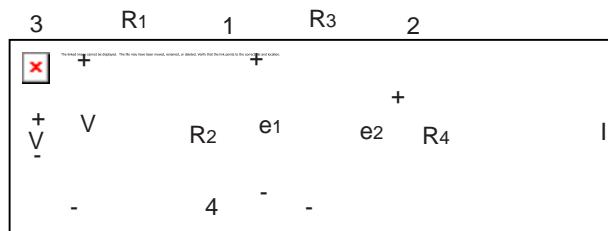


FIGURE 3.12 A resistive circuit.

determined by standard algebraic methods. First, rewrite the equations with the source terms on the left-hand side of the equations, and the dependent variables on the right:

$$\frac{V}{R_1} = e_1 - \frac{1}{R_1 + R_2} + R_3 \frac{1}{3} - \frac{e_2}{R_3} \quad (3.20)$$

$$I = -R_3 \frac{e_1}{3} + e_2 - \frac{1}{R_3 + R_4}. \quad (3.21)$$

Rewriting in terms of conductance to simplify our calculations:

$$G_1 V = e_1 (G_1 + G_2 + G_3) - e_2 G_3 \quad (3.22)$$

$$I = -e_1 G_3 + e_2 (G_3 + G_4). \quad (3.23)$$

Application of Cramer's rule (see Appendix D), yields

$$e_1 = \frac{VG_1(G_3+G_4)+IG_3}{(G_1+G_2+G_3)(G_3+G_4)-G_{32}} \quad (3.24)$$

$$= \frac{V(G_1G_3+G_1G_4)+IG_3}{G_1G_3+G_2G_4+G_2G_3+G_3G_4}. \quad (3.25)$$

Similarly, we can obtain e_2 as

$$e_2 = \frac{G_1G_3V+(G_1+G_2+G_3)I}{(G_1+G_2+G_3)(G_3+G_4)-G_{32}} \quad (3.26)$$

All node voltages are now known, and from these node voltages all branch variables in the circuit can be explicitly determined by using KVL and the constituent relations. For example, suppose the voltage across R_3 is v_3 , and the current through R_3 is i_3 , as illustrated in Figure 3.13. Then

$$v_3 = e_1 - e_2$$

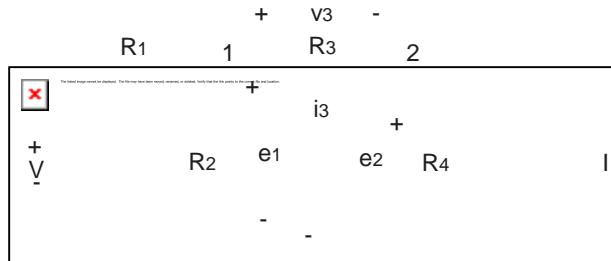


FIGURE 3.13 The resistive circuit.

and

$$i_3 = \frac{e_1 - e_2}{R_3}$$

Since the circuit in Figure 3.12, with $I = 0$, is the same as the circuit in Figure 2.46, the analysis of the two circuits (with $I = 0$) using the basic and the node methods should yield the same results. Accordingly, the reader might want to compare the values for v_3 and i_3 obtained here, with those obtained in Equations 2.135 and 2.131.

This example illustrates an important circuit property: The structure of a node equation is closely related to the topology of the circuit. We will briefly introduce this relationship here, and spend some more time on this topic in Section 3.3.4. First, let us write our two node equations 3.22 and 3.23 in matrix form:

$$\begin{matrix} G_1 + G_2 + G_3 & -G_3 & e_1 \\ -G_3 & G_3 + G_4 & = e_2 \end{matrix} \quad \begin{matrix} G_1 & 0 & V \\ 0 & 1 & I \end{matrix} . \quad (3.27)$$

The matrix equation is in the form

$$G^- e^- = S^- s^- \quad (3.28)$$

where e^- is a column vector of unknown voltages and s^- is the column vector of known source amplitudes. G^- is called the conductance matrix and S^- is called the source matrix for reasons that will be apparent shortly. In Equation 3.22, written at the e_1 node, we note from Figure 3.12 that the coefficient of the e_1 term (the first term in the first row of the G matrix) is the sum of the conductances connected to the e_1 node. Similarly in Equation 3.23, the coefficient of the e_2 term (the second term in the second row of the G matrix) is the sum of the conductances connected to the e_2 node. (These terms are often called the "self" conductances.) The off-diagonal coefficients represent conductances connected between the corresponding nodes, the "mutual" conductances. In Equation 3.22, for example, the coefficient of the e_2 term (the second term in the first row of the G matrix) is the mutual conductance between the e_1 node (because this is the e_1 equation) and e_2 . For linear resistive circuits, the off-diagonal terms are negative, assuming that the equations have been structured to make the main-diagonal terms positive.

It is self-evident that with circuits made up of linear resistors, the mutual conductance e_1 to e_2 must be the same as the mutual conductance from e_2 to e_1 . Hence the two off-diagonal coefficients in the node equations are identical. More generally, we expect node equation coefficientsto exhibit mirror symmetry about the main diagonal for linear resistive circuits, as is evident from the G -matrix. These helpful topological constraints are destroyed if we do not apply

KCL at the nodes defined by the node voltages. Such a procedure is mathematically correct (the new equations are derivable by algebraic manipulation of the original equations, Equations 3.22 and 3.23) but the symmetries are gone.

Interestingly, the SPICE software package uses the node method to solve circuits. The program takes as input a file containing a description of the circuit topology and by systematically following the node method produces a matrix equation such as that in Equation 3.27. It then solves for the vector of unknowns e^- using standard linear algebraic techniques.

example 3.5 node method Determine the current i through the 5-resistor in the circuit in Figure 3.14.

Let us use the node method to solve the circuit. As Step 1 of node analysis, we will choose Node 1 as our ground node as depicted in Figure 3.14.

Step 2 labels the potentials of the remaining with respect to the ground node. Figure 3.14 shows such a labeling. Since Node 2 is connected to the ground node through an independent voltage source, it is labeled with the voltage of the source, namely 1V. Node 3 is labeled with a node voltage e_1 and Node 4 is labeled with a node voltage e_2 .

Next, following Step 3, we write KCL for Nodes 3 and 4. KCL for Node 3 is

$$\frac{e_1 - 1 + e_4}{3} - \frac{e_1 - e_2}{2} + 2 = 0$$

and that for Node 4 is

$$-2 + \frac{e_2 - e_1}{2} - 5_2 - 1 = 0.$$

Following Step 4 we solve these equations to determine the unknown node voltages. This yields

$$e_1 = 0.65V$$

and

$$e_2 = 4.75V.$$

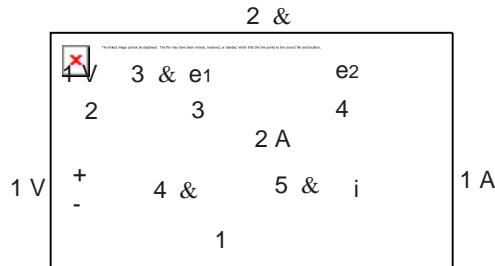


FIGURE 3.14 Determining the unknown current i .

We can now determine i :

$$i = \frac{4.75}{5} = 0.95A.$$

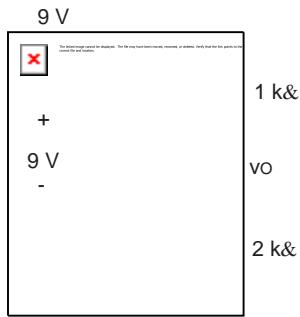


FIGURE 3.15 The voltage-divider circuit.

example 3.6 node method solution of the voltage-divider circuit Let's you think the node method is applicable only to complex circuits with many nodes, let us apply the node method to the simple voltage-divider circuit in Figure 3.15 to obtain the voltage v_o .

The ground node is selected as shown in Figure 3.15. The circuit in Figure 3.15 has one unknown node voltage, v_o , also as marked in the figure. So, Steps 1 and 2 are complete.

Following Step 3, we write KCL for the node with the unknown node voltage:

$$\frac{v_o - 9}{1k} + \frac{v_o}{2k} = 0.$$

Multiplying throughout by $2k$ we obtain

$$2v_o - 18 + v_o = 0$$

which yields

$$v_o = 6V.$$

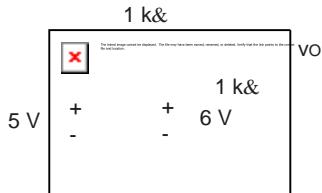


FIGURE 3.16 A summing circuit.

example 3.7 find node voltage using the node method Determine the node voltage v_o in the circuit shown in Figure 3.16 using the node method.

The circuit in Figure 3.16 has only one unknown node voltage, v_o , as marked in the figure. Figure 3.16 also shows a ground node, and so Steps 1 and 2 are complete.

Following Step 3, we write KCL for the node with the unknown node voltage:

$$\frac{v_o - 5}{1k} + \frac{v_o - 6}{1k} = 0$$

Multiplying throughout by $1k$ we obtain

$$v_o - 5 + v_o - 6 = 0$$

which simplifies to

$$v_o = \frac{5V + 6V}{2}$$

or

$$v_o = 5.5V.$$

The circuit in Figure 3.16 is called an adder circuit since v_o is proportional to the sum of the input voltages.



example 3.8 more on the node method Determine the node voltage in the circuit in Figure 3.17 using the node method.

The ground node and unknown node variables are marked as shown in Figure 3.17. Next, following Step 3, we write KCL for the node with the unknown voltage.

Then, we write KCL for the node with the unknown node voltage::

$$\frac{v - 2}{3} = 3V.$$

Thus,

$$v = 11V.$$

Compare the node analysis shown here with the basic method applied to the same circuit on page 190.



example 3.9 even more on the node method

3.3.2 FLOATING INDEPENDENT VOLTAGE SOURCES

Node analysis as described here does not work for circuits that contain floating independent voltage sources such as the one shown in Figure 3.20. A floating independent voltage source is a voltage source that has neither terminal connected to ground, nor directly or through one or more other independent voltage sources. Thereason node analysis does not work is that the element law for an independent voltage source does not relate its branch current to its branch voltage. Therefore, it is not possible to complete Step 3 of node analysis if the circuit contains a floating independent voltage source. In this case, it is necessary to modify the node analysis slightly.

To apply node analysis to a circuit containing a floating voltage source we must realize that the node voltages at the terminals of the source are directly

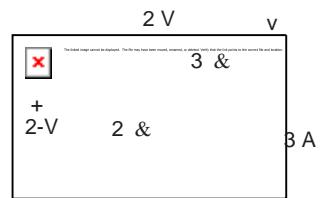
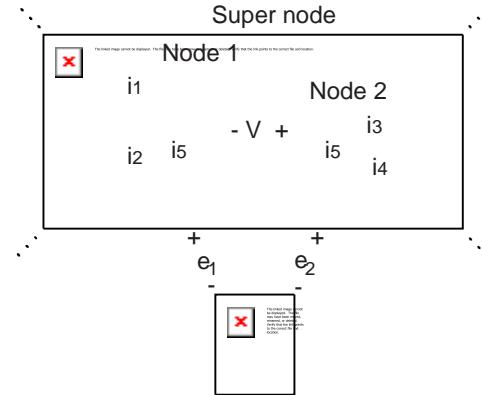


FIGURE 3.17 A circuit with two independent sources.

FIGURE 3.20 A floating independent voltage source and its treatment as a supernode.



related by the element law for that source. For example, the application of KVL to the circuit in Figure 3.20 shows that

$$e_2 = V + e_1. \quad (3.32)$$

Because of this, the number of unknown node voltages in the circuit can be immediately reduced by one since e_1 and e_2 can be determined directly from each other using Equation 3.32. Consequently, the number of independent statements of KCL needed to determine the unknown node voltages can similarly be reduced by one. Thus, Nodes 1 and 2 in Figure 3.20 must together contribute one statement of KCL to the first part of Step 3 of the node analysis (namely, writing KCL for each of the nodes that has an unknown node voltage). Further, this single statement of KCL should not involve e_5 since e_5 cannot be determined from the element law of the voltage source in the second part of Step 3 (namely, using KVL and element laws to obtain the currents directly in terms of the node voltage differences and element parameters).

To derive the desired statement of KCL for Nodes 1 and 2, we draw a surface around both nodes, enclosing what is referred to as a supernode in the process. Then, we write KCL for the supernode. In the case of Figure 3.20, KCL applied to the supernode yields

$$i_1 + i_2 + i_3 + i_4 = 0 \quad (3.33)$$

for the first part of Step 3. Note that this statement of KCL is nothing more than the sum of

$$i_1 + i_2 + i_5 = 0 \quad (3.34)$$

$$i_3 + i_4 - i_5 = 0, \quad (3.35)$$

which are the individual statements of KCL for Nodes 1 and 2. Following this, in the second part of Step 3, the currents are eliminated by substituting node voltages and element parameters in their place. In our example, i_1 and i_2 are determined using e_1 and the parameters of the elements through which i_1 and i_2 flow. Similarly i_3 and i_4 are determined using $e_1 + V$ and the parameters of the elements through which i_3 and i_4 flow, with e serving as the one unknown node voltage.

Alternatively, i_1 and i_2 can be determined using $e_2 - V$, and i_3 and i_4 can be determined using e , with e serving as the one unknown node voltage. Finally, it should be recognized that a floating string of independent voltage sources is handled in exactly the same manner as a floating isolated independent voltage source.

Let us illustrate node analysis applied to a circuit with a floating independent voltage source, and hence a supernode, using the circuit shown in Figure 3.21. The circuit is the same as that shown in Figure 3.10 except that Node 2 is now selected as the ground node, and the node voltages for Nodes 1 and 3 are defined differently. The supernode containing the floating voltage source is also marked in the figure.

The primary unknown in the circuit, e , is now the voltage at Node 3. Note also that the voltage at Node 1, the other node in the supernode, is labeled in terms of e . By defining the ground node and labeling the node voltages, we have completed Steps 1 and 2 in the node analysis.

Next we perform Step 3 for the supernode. This yields

$$\frac{e+V+R}{R_1} \frac{e}{2} + I = 0. \quad (3.36)$$

In Equation 3.36, $(e+V)/R_1$ is the current (written in terms of node voltages and element parameters) out of the supernode through the branch containing

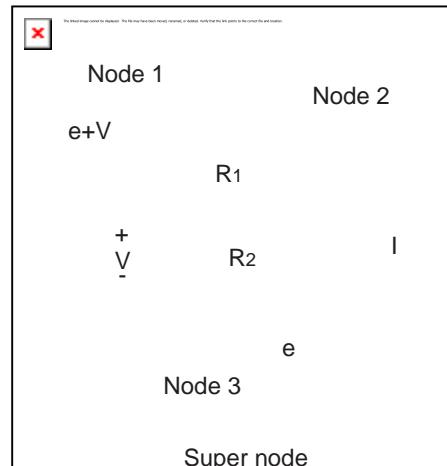


FIGURE 3.21 A circuit with a floating independent voltage source.

R₁. Similarly, e/R₂ is the current out of the supernode through R₂, and this is the current through the third branch from the supernode.

Following Step 4, the solution of Equation 3.36 is

$$e = -R \frac{R_1 R_2}{R_1 + R_2} I - \frac{R_2}{R_1 + R_2 V}. \quad (3.37)$$

Finally, to complete the node analysis, the solution for e could be used in Step 5 of node analysis to determine the branch voltages and then the branch currents in the circuit. While we will not do this here, it is worth while to see that it will yield the same results as in Equations 3.10 through 3.16, providing that the branch currents and voltages are defined in the same manner. To see that this will be the case, observe that in Equation 3.37 is the same as in Equation 3.9 except for a minus sign, owing to the change in the sign of e as defined in Figures 3.10 and 3.21.

example 3.10 floating independent voltage source As another example of node analysis is applied to a circuit with a floating independent voltage source, consider the circuit shown in Figure 3.22. In this circuit, the voltage source having value V₃ is the only floating independent voltage source. Because the source having value V₁ is connected to ground at Node 5 it is not a floating source, hence Node 1 is labeled with the node voltage V₁. Similarly, the source having value V₂ is not a floating source because it is connected to ground through the known voltage V₁, hence Node 2 is labeled with the known node voltage V₁+V₂. Thus, only the voltages at Nodes 3 and 4 in the supernode are unknown. In Figure 3.22, Node 3 is labeled with the unknown node voltage e, and so Node 4 is labeled with the node voltage e+V₃.

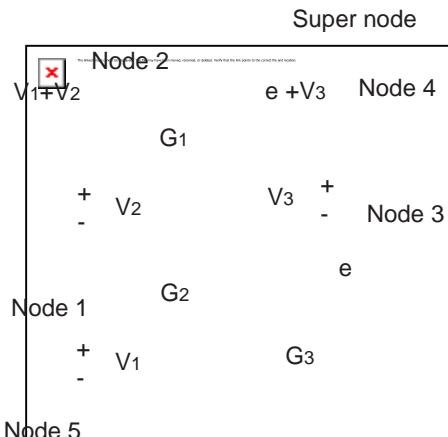


FIGURE 3.22 Another circuit with a floating independent voltage source.

To continue the node analysis of the circuit in Figure 3.22, we perform Step 3 for the supernode. This yields

$$G_1[(e+V_3)-(V_1+V_2)] + G_2(e-V_1) + G_3e = 0. \quad (3.38)$$

Here, conductances have been used for convenience. Following Step 4, the solution of Equation 3.38 is

$$e = \frac{(G_1+G_2)V_1+G_1V_2-G_1V}{G_1+G_2+G}. \quad (3.39)$$

Finally, to complete the node analysis, the solution for e could be used in Step 5 to determine the branch voltages and then the branch currents in the circuit. We will not do this here.

3.3.3 DEPENDENT SOURCES AND THE NODE METHOD

A dependent source will also complicate the node analysis previously described when its element law does not easily relate its branch current to its branch voltage. In this case, it will again not be possible to complete Step 3, and so it is again necessary to modify the node analysis slightly. Since there are four types of dependent sources, and the branch currents and voltages that control them can appear through or across many different types of elements, it is impractical to treat each case separately in its most efficient manner. As a compromise, we present the easing method that treats all cases of dependent sources, and illustrate how this method can be made more efficient in a few illustrative cases. We will illustrate the method using the circuit in Figure 3.23, which contains a dependent current source, whose current is some function of a branch variable i as shown in the figure.

Our method of applying node analysis to a circuit containing dependent sources begins by assuming that we know the value of each dependent source. This assumption allows us to treat each dependent source as an independent source, and carry out a node analysis of the circuit as described in the previous subsections. For example, in the case of a dependent current source (see Figure 3.23), we replace the dependent source with an independent current source with some assumed current, say I (see Figure 3.24), and carry out our usual five-step node analysis. As part of this analysis we solve for the branch variables that control the dependent sources in terms of the assumed source values.

Of immediate interest are the expressions for the branch variables that control dependent sources. In our example, this branch variable is i . Next, we substitute these expressions for the controlling variables into the element laws for the dependent sources, and self-consistently solve for the actual values of the dependent sources. Continuing with our dependent current source example of

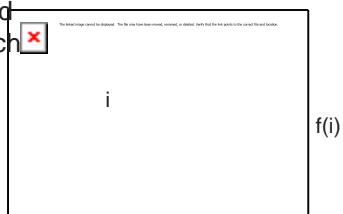


FIGURE 3.23 A circuit containing a dependent current source.

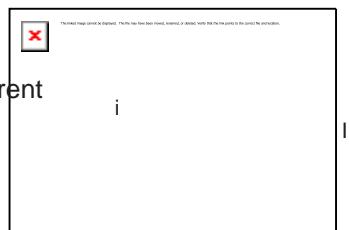


FIGURE 3.24 Replacing the dependent current source with an independent current source I .

Figure 3.23, suppose that the expression for i is some function of the assumed current I and is of the form

$$i = g(I). \quad (3.40)$$

We substitute this expression for the branch variable into the element law for the dependent current source as

$$I = f(i) = f(g(I)) \quad (3.41)$$

and solve for I . The solution for I will not contain the variable i . Note that if the expression for i is shown in Equation 3.40 does not contain I , then no additional work needs to be done to solve for I , since $f(g(I))$ is itself a solution for I .

Finally, we back-substitute the actual values of the dependent sources—in other words, the solution for I —into the original node analysis, thereby completing the analysis in total.

As a concrete example, suppose the dependence source function

$$f(i) = 10i.$$

Further, suppose we obtain the following expression for i as a function of the assumed current I :

$$i = g(I) = 2I \pm 2A.$$

Then, according to Equation 3.41,

$$I = f(g(I)) = 10I \pm 2A.$$

Solving, we get

$$I = -5A.$$

As expected, the solution for I does not contain the variable i .

This modification to the original node analysis is not always the most efficient method of analysis, but it always works. However, when the element laws for the dependent sources can be easily expressed in terms of the node voltages, it is possible to take a more intuitive approach and apply the simple node analysis described in Section 3.3 without modification. In our example of Figure 3.23, suppose that the circuit on the left has the node voltages shown

in Figure 3.25. In this case, it is easy to see that the element law for the current source can be easily written in terms of the node voltages as

$$f(i) = f \frac{e_a - e_b}{R}$$

and our simple node analysis can be applied without modification. We will do examples using both the modified and unmodified versions of the node method.

To illustrate our modified method of node analysis for a circuit containing a dependent source, consider the analysis of the circuit shown in Figure 3.26. This circuit has one dependent source, namely a CCCS. To analyze this circuit using the node method, we first replace its CCCS with an independent current source carrying a known current, say i , and analyze the resulting circuit. The resulting circuit, however, is exactly that shown in Figure 3.10, which we have already analyzed using the node method in Section 3.3. Note that the value in Figure 3.10 replaces the value i_1 in Figure 3.26. Thus, we are partially done with the analysis of the circuit in Figure 3.26.

The results of our analysis of the circuit in Figure 3.10 appear in Equations 3.10 through 3.16. Let us copy them here for convenience after replacing conductances with resistances.

$$v_0 = V \quad (3.42)$$

$$i_0 = \frac{R_2}{R_1 + R} 2i - \frac{1}{R_1 + R_2 V} \quad (3.43)$$

$$v_1 = -\frac{R_2}{R_1 + R} 2i + \frac{R_1}{R_1 + R_2 V} \quad (3.44)$$

$$i_1 = -\frac{R_2}{R_1 + R} 2i + \frac{1}{R_1 + R_2 V} \quad (3.45)$$

$$v_2 = v_3 = \frac{R_1 R_2}{R_1 + R} 2i + \frac{R_2}{R_1 + R_2 V} \quad (3.46)$$

$$i_2 = \frac{R_1}{R_1 + R} 2i + \frac{1}{R_1 + R_2 V} \quad (3.47)$$

$$i_3 = -i. \quad (3.48)$$

Of particular interest from that analysis is the value of i_1 because i_1 controls the CCCS in Figure 3.26. Using the result for i_1 from Equation 3.45 we next write

$$I = \alpha i_1 = \alpha - \frac{R_2}{R_1 + R} 2i + \frac{1}{R_1 + R_2} V. \quad (3.49)$$

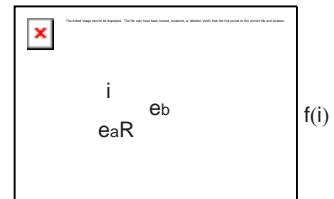


FIGURE 3.25 Node voltages.

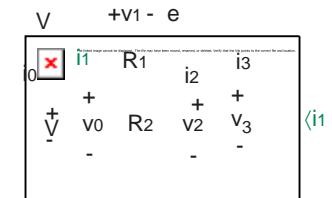


FIGURE 3.26 A circuit with a dependent source.

The first equality in Equation 3.49 expresses the equality of the CCCS in Figure 3.26 and its surrogate independent current source in Figure 3.10. The second equality follows from the substitution for i_1 using Equation 3.45 from the node analysis of the circuit in Figure 3.10. Since i_1 is determined in terms of I during that analysis, Equation 3.49 becomes an implicit equation that must be solved for I . This solution yields

$$I = \frac{\alpha}{R_1 + (1+\alpha)R_2 V} \quad (3.50)$$

The actual value of the CCCS is now known.

Finally, we back-substitute Equation 3.50, namely the actual value of I , into Equations 3.42 through 3.48 to obtain

$$v_0 = V \quad (3.51)$$

$$i_0 = -\frac{1}{R_1 + (1+\alpha)R_2 V} \quad (3.52)$$

$$v_1 = \frac{R_1}{R_1 + (1+\alpha)R_2 V} \quad (3.53)$$

$$i_1 = \frac{1}{R_1 + (1+\alpha)R_2 V} \quad (3.54)$$

$$v_2 = v_3 = \frac{(1+\alpha)R_2}{R_1 + (1+\alpha)R_2 V} \quad (3.55)$$

$$i_2 = \frac{R_1 + 1(1+\alpha)R_2}{R_1 + (1+\alpha)R_2 V} \quad (3.56)$$

$$i_3 = \frac{-\alpha}{R_1 + (1+\alpha)R_2 V} \quad (3.57)$$

This completes the analysis of the circuit in Figure 3.26.

While the preceding analysis is not terribly difficult, it cannot nevertheless be carried out more efficiently in many cases. As mentioned previously, commonly, it is possible to apply the simple node analysis described in Section 3.3 without modification because the element law for the CCCS can be easily expressed in terms of the node voltage e . To see this, we begin by performing Step 3 of node analysis to write

$$\frac{e - V + R_2}{R_1} - \alpha V - \frac{e}{R_1} = 0 \quad (3.58)$$

for the node at which e is defined. Note that in the third term in Equation 3.58, $(V - e)/R_1$ has been substituted for i_1 .

Next, following Step 4, we solve Equation 3.58 for e to obtain

$$e = \frac{(1+\alpha)R_2}{R_1 + (1+\alpha)R_2 V} \quad (3.59)$$

This result is the same as expressed in Equation 3.55. The remainder of the node analysis, namely Step 5, then proceeds to yield Equations 3.51 through 3.57 directly. It is important to note, however, that the node analysis of circuits containing dependent sources cannot always be easily simplified in this manner.

example 3.11 dependent current source Now, let us analyze a slightly different circuit containing a dependent source as shown in Figure 3.27. The node voltages v_o and v_i are marked. The dependent current source supplies a current

$$i_o = f(x)$$

where we will consider two cases:

1. In the first case, x is the voltage v_i , and the current

$$i_o = -G_m v_i.$$

2. In the second case, x is the current i_i , and

$$i_o = -\beta i_i.$$

Let us suppose that we are specifically interested in determining v_o as a function of v_i in both cases.

Let us consider the first case in which

$$i_o = -G_m v_i.$$

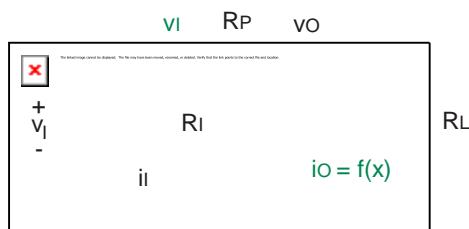


FIGURE 3.27 Another dependent current source circuit.

Notice that ratio is directly expressed in terms of a node voltage, and so we can apply your simple node analysis technique without any modification, remembering, however, to substitute the element law for the dependent source current when writing KCL for the nodes with unknown voltages.

Since the ground and node voltages have been defined as shown in Figure 3.27, Steps 1 and 2 of node analysis are complete.

For Step 3, we write KCL at the node with the unknown voltage v_o by summing the currents into the node as follows:

$$\frac{v_i - v_o}{R_p} + (-G_m v_i) = \frac{v_o}{R_L} \quad (3.60)$$

Notice that we have used the element law for the dependent current source, namely,

$$i_o = -G_m v_i$$

to substitute for the current into the node from the dependent current source.

By simplifying Equation 3.60, we obtain:

$$v_o = \frac{(1 - G_m R_p) R_L}{R_p + R_L} v_i. \quad (3.61)$$

We have thus expressed v_o as a function of v_i when $i_o = -G_m v_i$.

Let us now consider the second case in which

$$i_o = -\beta i_i.$$

Although not directly expressed in terms of a node voltage, it is easy to see that i_o can be expressed in terms of a node voltage by substituting $i_i = v_i / R_i$ as follows:

$$i_o = -\beta v_i \frac{1}{R_i}$$

Thus, as in the first case, we can apply your simple node analysis technique without any modification. Going to Step 3 of node analysis, we write KCL at the node with the unknown voltage v_o by summing the currents into the node as follows:

$$\frac{v_i - v_o}{R_p} + (-\beta R_i \frac{v_i}{R_i}) = \frac{v_o}{R_L} \quad (3.62)$$

Notice that we have used the element law for the dependent current source, namely,

$$i_o = -\beta v_i - \frac{v_i}{R_i}$$

to substitute for the current into the node from the dependent current source.

By simplifying Equation 3.62, we obtain:

$$V_o = \frac{1 - \beta R_p}{R_p + R_L} V_i. \quad (3.63)$$

We have thus expressed V_o as a function of V_i when $\alpha = -\beta i$.



example 3.12 a more complex dependent-current source problem

3.3.4 THE CONDUCTANCE AND SOURCE MATRICES *

3.4 LOOP METHOD *

example 3.13 loop method

3.5 SUPERPOSITION

Suppose we make the circuit in Figure 3.12 one step more complicated by adding a third source, as shown in Figure 3.33. Straightforward node analysis following the procedure outlined by the node method yields

$$(V_1 - e_1)G_1 + (V_2 - e_1)G_2 + (e_2 - e_1)G_3 = 0 \quad (3.97)$$

$$(e_1 - e_2)G_3 - e_2 G_4 + I = 0. \quad (3.98)$$

Collecting the source terms on the left side:

$$V_1 G_1 + V_2 G_2 = e_1 (G_1 + G_2 + G_3) - e_2 G_3 \quad (3.99)$$

$$I = -e_1 G_3 + e_2 (G_3 + G_4). \quad (3.100)$$

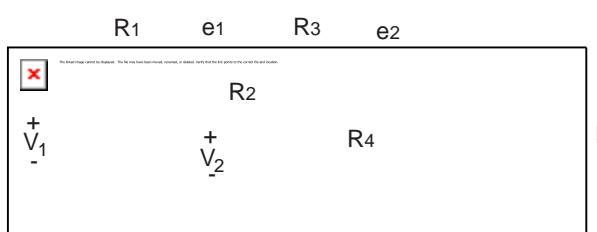


FIGURE 3.33 A network with three sources.

Let us again find e_1 :

$$e_1 = \frac{(V_1 G_1 + V_2 G_2)(G_3 + G_4) + I G_3}{(G_1 + G_2 + G_3)(G_1 + G_2 + G_3 + G_4)} \quad (3.101)$$

$$= \frac{V_1 G_1 (G_3 + G_4) + V_2 G_2 (G_3 + G_4) + I G_3}{G_1^2 G_3^2 G_4^2} \quad (3.102)$$

Again note the structure of this expression:

All denominator terms are of the same sign. Thus the denominator cannot be made zero for any non-zero values of conductances. (If the denominator could be made zero, we could get infinite e_1 for finite sources values, a violation of conservation of energy.)

Each term on the right consists of one source term multiplied by a resistive (or conductive) factor. There are no products of source terms.

We now wish to translate these mathematical constraints to circuit constraints, to find simpler methods for analyzing multi-source networks. Specifically, we wish to find the terms in Equation 3.102, by inspection, from Figure 3.33. The mathematics says that, because of linearity, the first term remains unchanged if the other two sources are set to zero. We must now interpret this statement in circuit terms. Mathematically, we wish to set variable V_2 to zero, so in circuit terms we must set voltage source V_2 to zero. By definition, source V_2 must now be zero regardless of what current flows through it, that is, it must be a short circuit. So in general, setting a voltage source to zero is equivalent in circuit terms to replacing that source by a short circuit. Similarly, setting I to zero means that no current can flow through that branch of the circuit regardless of the terminal voltage. Hence setting a current source to zero is equivalent in circuit terms to replacing that source by an open circuit. These are two additional important circuit primitives. Applying these two concepts to Figure 3.33, we can find the first term in Equation 3.102, that is, the part of e_1 arising from source V_1 , by forming a subcircuit from Figure 3.33 with V_2 and I set to zero as shown in Figure 3.34a. Thus, in Figure 3.34a, e_{1A} is the voltage component of e_1 due to source V_1 acting alone. Now e_{1A} can be found by inspection using the voltage-divider primitive:

$$e_{1A} = V_1 \frac{R_2(R_3 + R_4)}{R_1 + R_2 + R_3 + R_4} \quad (3.103)$$

where the two vertical lines are shorthand notation for “in parallel with.” The numerator, for example, is R_2 in parallel with the sum of R_3 and R_4 . The calculation is somewhat simplified if we use conductance instead of resistance.

Using the conductance form of the voltage-divider relation (Equation 2.50), we find

$$e_{1A} = V_1 \frac{G_1}{G_1 + G_2 + G_3 + G_4 / (G_3 + G_4)} \quad (3.104)$$

where the two conductances in series, G_3 and G_4 are calculated using Equation 2.58. Both of these expressions are the same as the first term in Equation 3.102, after some manipulation. Note that the form of Equation 3.104 is much simpler and more insightful than the forms in Equations 3.101 and 3.102, because the derivation in terms of the voltage-divider primitive reveals the basic structure of the circuit. But the main point of this development is to show that the effect of source V_1 on the node voltage e_1 can be found very easily by forming a subcircuit in which V_2 and I are set to zero.

By the same argument, the effect of V_2 and I on e_1 can be calculated using the subcircuits shown in Figure 3.34b and 3.34c, respectively. For V_2 , sources V_1 and I are set to zero, as shown in Figure 3.34b. Clearly circuits 3.34a and 3.34b are identical in topology, so the effect of V_2 on e_1 can be written from Equation 3.103 by interchanging R_1 and R_2 , or G_1 and G_2 in Equation 3.104. This will give us e_{1B} , the component of e_1 due to voltage source V_2 .

To find the effect of I , it is necessary to set both V_1 and V_2 to zero, that is, replace each by a short circuit, as shown in Figure 3.34c. Now e_{1C} can be

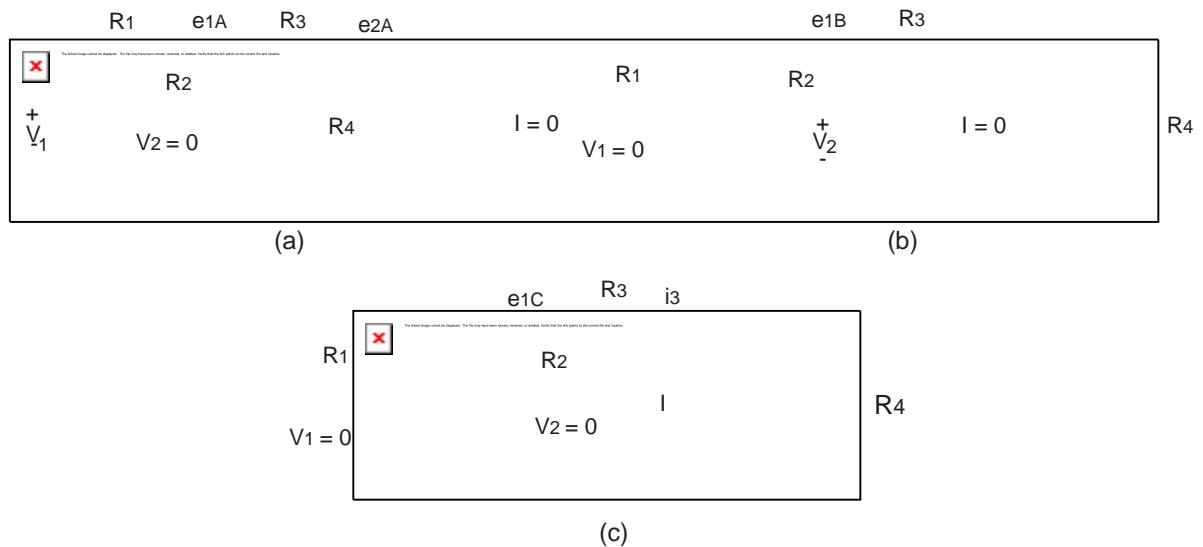


FIGURE 3.34 Subcircuits.

found by noting that the total conductance of the path to the left of the source is, from Equations 2.94 and 2.58,

$$G = \frac{(G_1 + G_2)G_3}{G_1 + G_2 + G_3} \quad (3.105)$$

Hence, from the current divider relation, the current through R_3 is

$$i_{R_3} = \frac{GI}{\frac{G}{G+G_4} \cdot \frac{G}{G+G_2}} \quad (3.106)$$

Now e_{1C} can be found from the relation

$$e_{1C} = \frac{i_{R_3}}{G_1 + G_2} \quad (3.107)$$

$$= \frac{GI}{(G+G_4)(G_1+G_2)} \quad (3.108)$$

which, on substitution of Equation 3.105 and simplification, reduces to

$$e_{1C} = \frac{IG_3}{(G_1+G_2)G_3 + G_4(G_1+G_2) + G_3G_4} \quad (3.109)$$

This is equivalent to the third term in Equation 3.102.

This example illustrates both the use of superposition to solve a network with several sources, and also shows how primitives (elementary procedures) can be used to solve circuits by inspection. Generalizing, we note that any messy linear network — the one in Figure 3.15, for example — will yield straightforward network analysis and lead to a set of equations of the form

$$V_1G_{1a} + V_2G_{1b} + \dots + I_1 + \dots = e_1G_{11} + e_2G_{12} + \dots \quad (3.110)$$

$$V_1G_{2a} + \dots \quad \dots \quad \dots = e_1G_{21} + e_2G_{22} + \dots$$

$$V_1G_{3a} + \dots \quad \dots \quad \dots = e_1G_{31} + \dots$$

These have been written in the standard form, with source terms on the left in each equation. All of the unknown variables appear on the right side, each multiplied by conductances: the sum of the appropriate "self" conductances for terms along the main diagonal, and the sum of the appropriate "mutual" conductances elsewhere.

Further, the solution of such a set of linear simultaneous equations will always result in an expression of the general form of Equation 3.102, in which the voltage or current we are trying to evaluate will be equal to a sum of terms each involving only one source.

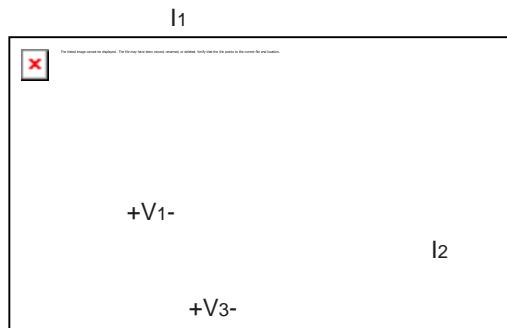


FIGURE 3.35 Aresistive network.

The superposition theorem thus states that in a linear network with a number of independent sources, the response can be found by summing the responses to each independent source acting alone, with all other independent sources set to zero. These individual responses can be found very readily by forming subcircuits in which all independent sources except one are reset to zero.

Accordingly, the superposition method for linear networks can best be stated as follows:

The Superposition Method

- For each independent source, form a subcircuit with all other independent sources set to zero. Setting a voltage source to zero implies replacing the voltage source with a short circuit, and setting a current source to zero implies replacing the current source with an open circuit.
- From each subcircuit corresponding to a given independent source, find the response to that independent source acting alone. This step results in a set of individual responses.
- Obtain the total response by summing together each of the individual responses.

example 3.14 superposition analysis of averaging circuit

Show that the node voltage v_0 in the circuit shown in Figure 3.36 is the average of the two input voltages using the method of superposition.

By the method of superposition, the voltage v_0 can be determined by summing the responses of each of the sources acting alone. We will first obtain v_{05} , the response of the 5-V source acting alone. The subcircuit corresponding to the 5-V source acting alone is shown in Figure 3.37. Notice we have shorted the 6-V source.

By the voltage divider action, we can write

$$v_{05} = \frac{1k}{1k+1k} 5V = \frac{5}{2} V.$$

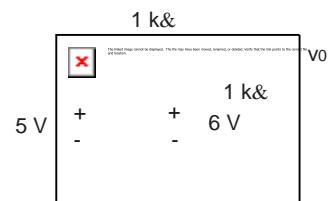


FIGURE 3.36 Circuit for performing superposition analysis.

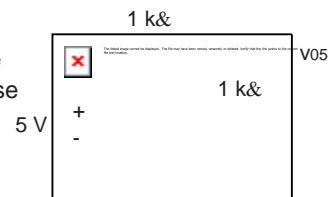


FIGURE 3.37 Circuit with 5-V source acting alone.

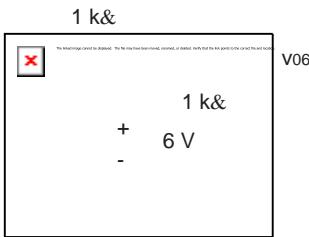


FIGURE 3.38 Circuit with 6-V source acting alone.

Next, we obtain v_{06} , the response of the 6-V source acting alone. The subcircuit corresponding to the 6-V source acting alone is shown in Figure 3.38. In this case, we have shorted the 5-V source.

Again, by the voltage divider action, we can write

$$v_{06} = \frac{1k}{1k+1k} 6V = \frac{6}{2} V.$$

We now sum the two partial responses to obtain

$$v_0 = v_{05} + v_{06} = \frac{5+6}{2} = 5.5V.$$

It is easy to see that v_0 is the average of the two input voltages.

example 3.15 applying the method of superposition Figure 3.39 shows a circuit containing a independent voltage source and an independent current source. Determine the current.

We will use the method of superposition to solve this circuit in two different ways. First, we will obtain the node voltage using superposition, and then, using the value of e , obtain the current I . Our second approach will directly determine I using the method of superposition.

First Method

Let us first determine the value of e using superposition. By the method of superposition, the voltage e can be determined by summing the responses of each of the sources acting alone. We will first obtain v_e , the response of the voltage source acting alone. The subcircuit corresponding to the voltage source acting alone is shown in Figure 3.40. Notice we have turned the current source off by open-circuiting it.

By the voltage divider action, we can write

$$e_v = 1 \cdot \frac{2}{2+2} = \frac{1}{2} V.$$

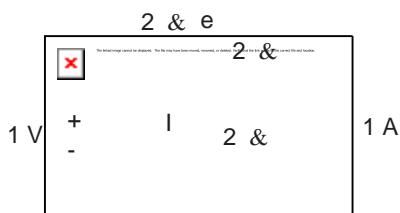


FIGURE 3.39 Circuit with two independent sources.

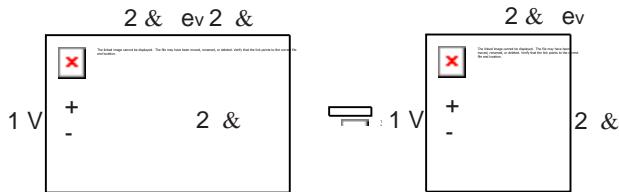


FIGURE 3.40 Subcircuit corresponding to the voltage source acting alone.

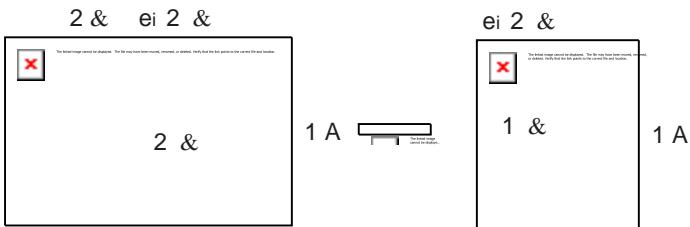


FIGURE 3.41 Subcircuit corresponding to the current source acting alone.

Next, we obtain e_i , the response of the current source acting alone. The subcircuit corresponding to the current source acting alone is shown in Figure 3.41. In this case, we have shorted the voltage source.

We first simplify the subcircuit by replacing the pair of 2-ohm resistors in parallel with an equivalent 1-ohm resistor as depicted in Figure 3.41. Then, since the 1-A current flows through each of the resistors, the voltage across the 1-ohm resistor is equal to e_i . In other words,

$$e_i = 1A \times 1 = 1V.$$

We now sum the two partial responses to obtain the total response. That is,

$$e = e_v + e_i = \frac{1}{2}1V = 1.5V.$$

We can now determine i as

$$i = \frac{e}{2} = \frac{1.5}{2}A = 0.75A.$$

Second Method

Next, we will directly determine i using superposition. Superposition says that i can be determined by summing the currents generated by each of the sources acting alone. We will first obtain i_v , the current due to the voltage source acting alone. The subcircuit corresponding to the voltage source acting alone is shown in Figure 3.42.

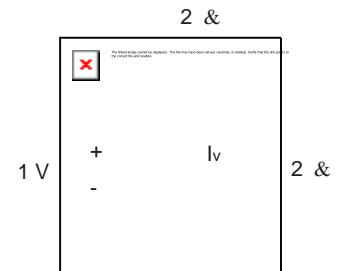


FIGURE 3.42 Subcircuit corresponding to the voltage source acting alone.

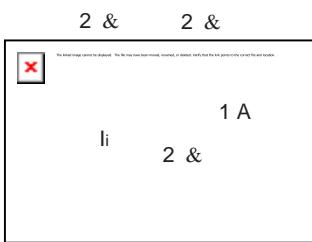


FIGURE 3.43 Subcircuit corresponding to the current source acting alone.

The current in the subcircuit is given by the voltage divided by the sum of the resistors. In other words,

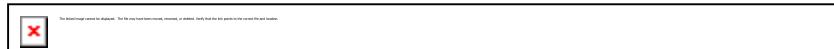
$$I_v = \frac{1 \text{ V}}{2+2} = 0.25 \text{ A.}$$

Next, we obtain I_i , the response of the current source acting alone. The subcircuit corresponding to the current source acting alone is shown in Figure 3.43.

By the current divider relation, it is easy to see that $I_i = 0.5\text{A}$, since the 1-A current supplied by the current source divides equally into the two branches of the subcircuit in Figure 3.43.

We now sum the two partial responses to obtain the total response. That is,

$$I = I_v + I_i = 0.25\text{A} + 0.5\text{A} = 0.75\text{A.}$$



example 3.16 resistive adder circuit An elementary resistive adding circuit is shown in Figure 3.44a. This circuit might be used to add together a number of microphone signals before sending them to one amplifier. (Notice that this circuit is a generalization of the circuit in Figure 3.36.) We shall discover better ways of building such a circuit in later chapters, but the present form serves as a good illustration of the principle of superposition.

From the preceding discussion, the effect on the output voltage V_o of the source V_1 acting alone can be found by forming a subcircuit in which all other independent sources are set to zero, which in this case means replacing V_2, V_3 , and V_4 by short circuits, as shown in Figure 3.44b. Now V_{oa} , the response to V_1 alone, can be found by inspection

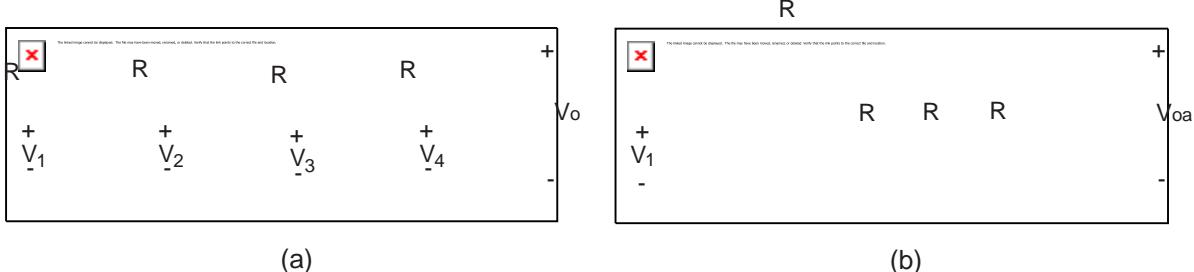


FIGURE 3.44 Resistive adding circuit.

using the voltage-divider relation

$$V_{oa} = \frac{R/3}{R+R/3} V_1. \quad (3.111)$$

The complete response is the sum of four such terms, which in this special case all have the same coefficient

$$V_o = \frac{1}{4} (V_1 + V_2 + V_3 + V_4). \quad (3.112)$$

Note that there is no restriction on the nature of the sources (other than frequency limits, etc., as discussed in Chapter 1). The sources could be DC, sine waves or square waves, speech, or a mixture of these. Equation 3.112 states that the output will be the sum of these individual signals, each multiplied by a constant, a “scaling factor.” If the inputs were four sine waves, each at a different frequency, then the output voltage would be the sum of these four sinusoids, appropriately scaled. No other frequencies would be present in the output signal. Thus a further consequence of linearity is that, whatever frequencies are present at the input or in the inputs of a linear system, these and only these frequencies will appear at the output.



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example 3.17 superposition applied to a beehive network

3.5.1 SUPERPOSITION RULES FOR DEPENDENT SOURCES

When the dependencies are linear, dependent sources are amenable to the set of analyses discussed earlier in Chapters 2 and 3. Care must be taken, however, in applying the superposition principle. Recall that the principle of superposition allows linear multi-source networks to be solved for one source at a time by setting all other independent sources to zero. Setting a voltage source to zero means replacing it with a short circuit; a current source set to zero is an open circuit. The complete response is the sum of the responses to each individual source.

What do we do about dependent sources? A practical way is to leave all the dependent sources in the circuit. The network can then be solved for one independent source at a time by setting all other independent sources to zero, and summing the individual responses.

Alternatively, the dependent sources could be treated as independent sources, and in a final step of the analysis, their dependencies must be back-substituted in terms of the other network parameters. However, this method tends to be impractical.

example 3.18 a single dependent source and superposition

Consider the circuit in Figure 3.49. It contains two independent sources and one dependent source. Using the superposition method, let us derive the output voltage v_o .

We will solve the circuit by leaving the dependent current source in the circuit and summing the responses of each of the independent sources acting alone.

1-V Source Acting Alone

Figure 3.50 shows the circuit corresponding to the 1-V source acting alone, where v_{o1} is the corresponding response. Notice that the dependent current source has been left in the circuit, and the 2-V source has been shorted out.

By the voltage divider relation, we know that

$$v_1 = 0.5V.$$

Thus,

$$v_{o1} = \frac{1}{100} v_1 \times 1k = 5V.$$

2-V Source Acting Alone

Figure 3.51 shows the circuit corresponding to the 2-V source acting alone, where v_{o2} is the corresponding response. By the voltage-divider relation, we know that

$$v_2 = 1V.$$

Thus,

$$v_{o2} = \frac{1}{100} v_2 \times 1k = 10V.$$

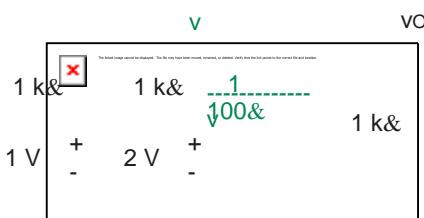


FIGURE 3.49 Circuit containing two independent sources and one dependent source.

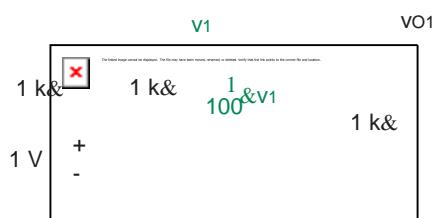


FIGURE 3.50 Subcircuit corresponding to the 1-V source acting alone.

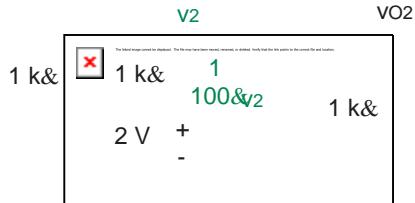


FIGURE 3.51 Subcircuit correspondingtothe2-Vsource actingalone.

Summing the two responses, we get the total response as

$$VO = VO_1 + VO_2 = 15V.$$



example 3.19 multiple dependent sources and superposition

As a more complicated example, consider the circuit in Figure 3.52. Using the superposition method, let us derive the output voltage v_o as a function of v_i .

This circuit has two dependent current sources and two independent voltage sources (v_1 and v_2). We will solve this problem by leaving both the dependent current sources in the circuit and summing the responses of each of the independent sources acting alone. We also define two intermediate variables, the node voltages v_a and v_b .

v_1 Acting Alone

We will first obtain the response with v_1 acting alone. Figure 3.53 shows the circuit corresponding to v_1 acting alone. v_{o1} is the corresponding response. Notice that the

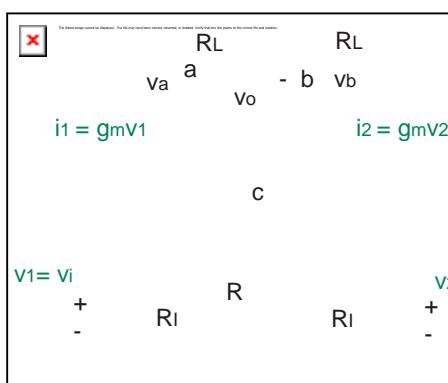


FIGURE 3.52 Circuitwithmultipledependent sources.

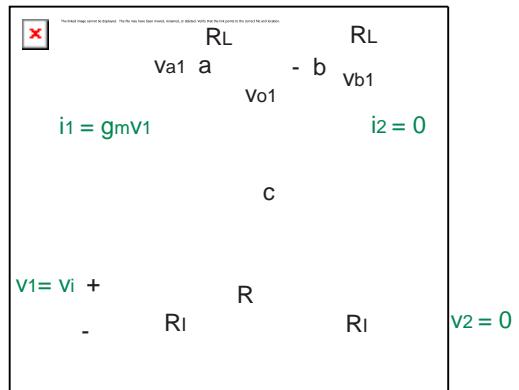


FIGURE 3.53 Subcircuitcorrespondingtov1acting alone.

dependent current sources have been left in the circuit, and v_2 has been shorted out. Since $v_2=0$, we find that $i_2=0$ (in other words, the dependent current source behaves like an open circuit).

We will first determine v_{a1} and v_{b1} , the node voltages at the nodes a and b due to v_1 acting alone. We will then determine v_{o1} as their difference.

Since $i_2=0$, there is no voltage drop across the resistor R_L connected to node b . So, node b will be at ground potential. In other words,

$$v_{b1}=0.$$

We can obtain v_{a1} by using KVL as

$$v_{a1}=0-i_1R_L=-g_m v_1 R_L=-g_m v_i R_L.$$

Therefore

$$v_{o1}=v_{a1}-v_{b1}=-g_m v_i R_L.$$

v_2 Acting Alone

Figure 3.54 shows the circuit corresponding to v_2 acting alone. v_{o2} is the corresponding response. In this circuit, since $v_1=0$, we find that $i_1=0$.

Since $i_1=0$, there is no voltage drop across the resistor R_L connected to node a , and so, this time around, node a will be at ground potential. In other words,

$$v_{a2}=0.$$

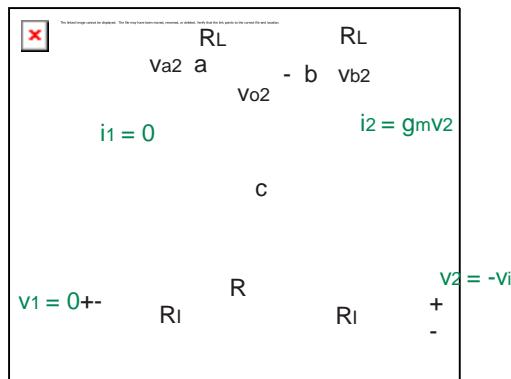


FIGURE 3.54 Subcircuit corresponding to v_2 acting alone.

We can obtain v_b by using KVL as

$$v_b = 0 - i_2 R_L = -g_m v_2 R_L = -g_m (-v_i) R_L = g_m v_i R_L.$$

Therefore

$$v_o = v_a - v_b = -g_m v_i R_L.$$

We can now obtain the total response by summing the responses to each of the independent sources acting alone. In other words,

$$v_o = v_{o1} + v_{o2} = -2g_m v_i R_L.$$

3.6 THÉVENIN'S THEOREM AND NORTON'S THEOREM

3.6.1 THE THÉVENIN EQUIVALENT NETWORK

A simple extension of the concept of superposition yields two additional network theorems of great power, which allow us to suppress a lot of detail in circuit analysis and focus attention only on that part of a network we are really interested in. Consider, for example, a battery, or a high-fidelity power amplifier, or a wall outlet for 110-VAC power, or a power supply for a computer.

What is the simplest way to describe the electrical properties of each of these systems at its output terminals? Is one parameter needed, or ten, or fifty? Clearly the voltage measured with a high-quality meter that draws negligible current is one important parameter (the open-circuit voltage mentioned in Section 1.7). Likewise we would want to know the frequency: zero frequency for the battery, 60 hertz (or 50 or even 25 in some countries) for the power line, etc. But we have already observed another effect that is important. When current is drawn from many of these systems, the voltage at the terminals drops. Depending on the quality of the wiring in a dormitory, the lights may dim noticeably when a toaster is plugged into the same circuit. Or the voltage of the flashlight battery will drop when a bulb is connected and current flows, as noted in Section 1.7. How can this effect be characterized? For the battery, is it necessary to make measurements at 100 current levels, and plot a curve of the characteristic?

If the system is linear, then the answer to this question is very simple. We will show that any collection of voltage sources, current sources, and resistors can be represented at any pair of terminals by one voltage source and one resistor, or by one current source and one resistor. The graphical construction of Figure 1.43 already hinted at this fact, but we present here a more formal proof. We start with a general linear network containing sources and resistors, shown as a amorphous box in Figure 3.55a. We presume that the only two

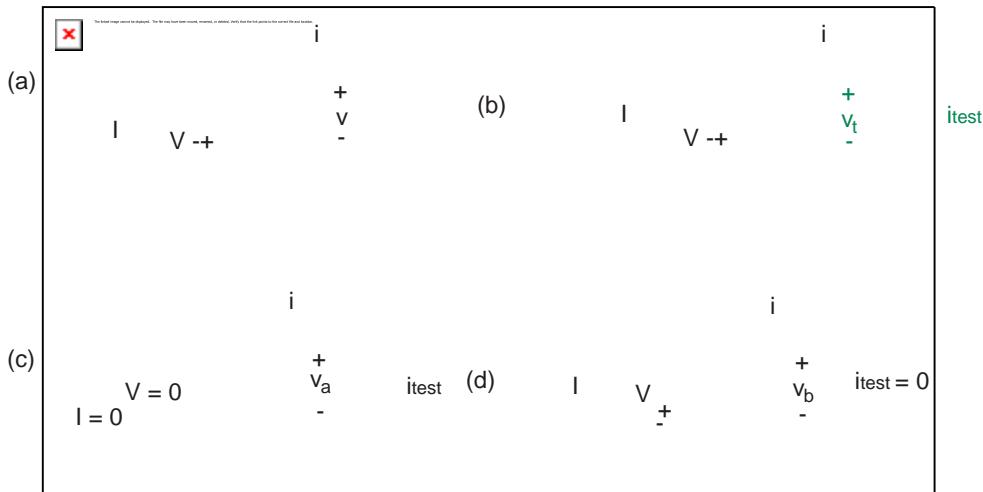


FIGURE 3.55 Derivation of the

Thévenin network.

terminals we are interested in are shown emerging on the right. We wish to find the relationship between v and i at these terminals.

To find v in terms of i , we need to apply some form of excitation, and measure the response. The derivation is simplest if we use either a voltage source or a current source, rather than a complicated excitation network. In Figure 3.55b, we have chosen to apply a test current source to the terminals. To calculate the response v by superposition, first set all the internal independent sources to zero, as in Figure 3.55c, and calculate the voltage v_a . As discussed in Section 3.5.1, dependent sources are left as is. Then set i_{test} to zero, as in Figure 3.55d, and calculate v_b . The desired value of v is the sum $v_a + v_b$. From Figure 3.55c,

$$v_a = i_{test} R_t \quad (3.113)$$

where R_t is the net resistance measured between the two terminals when all internal independent sources are set to zero. Resistance R_t is called the Thévenin Equivalent Resistance. From Figure 3.55d, v is obviously just the voltage appearing at the terminals of the original network when no current is flowing; we call this the open-circuit voltage. That is,

$$v_b = V_{oc} \quad (3.114)$$

Now by superposition,

$$v_t = v_a + v_b = V_{oc} + i_{test} R_t. \quad (3.115)$$

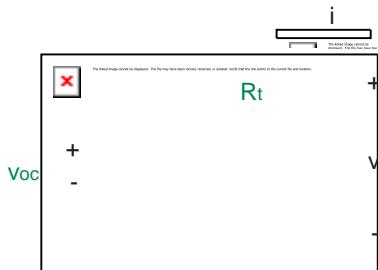


FIGURE 3.56 Thévenin equivalent.

This simple relation between voltage and current at a pair of terminals applies regardless of the complexity of the network, provided only that the network is linear. Thus, returning to the questions posed earlier, if we specify the open-circuit voltage and the Thévenin equivalent resistance of the battery, or the computer power supply, or the wall outlet, then to the extent that such systems can be considered to be linear, we have completely characterized the system as it appears at its terminals.

Equation 3.115 should be familiar from Section 1.7. It is the same as Equation 1.23, the volt–ampere relation for a voltage source in series with a resistor. In graphical terms it is the equation of a straight line in the v – i plane with slope $1/R_t$ and voltage axis intercept V_{oc} . So the preceding calculation can be interpreted in terms of a circuit called the Thévenin equivalent circuit shown in Figure 3.56. If V_{oc} and R_t are calculated using the subcircuits in Figure 3.55c and 3.55d, then this circuit and the one in Figure 3.55a are equivalent, in the sense that any measurement at the indicated terminals are equivalent. In other words, any measurement at the indicated terminals of the two circuits will yield identical results.

Two independent measurements on a circuit are required to determine the parameters for the Thévenin model. One appropriate pair of measurements is as follows. The source parameter V_{oc} is the voltage measured or calculated at the desired terminal pair when no current is flowing at these terminals:

$$V_{oc} = V_{\text{test}} \quad (3.116)$$

R_t is the resistance measured or calculated at the desired terminal pair when all internal independent sources are set to zero:

$$R_t = \frac{V_{\text{test}}}{I_{\text{test}}} \quad (3.117)$$

Summarizing, the Thévenin method allows us to abstract the behavior of a linear network at a given pair of terminals as a voltage source in series with a resistor. The voltage source in series with a resistor is called the Thévenin

A Method for Determining the Thévenin Equivalent Circuit

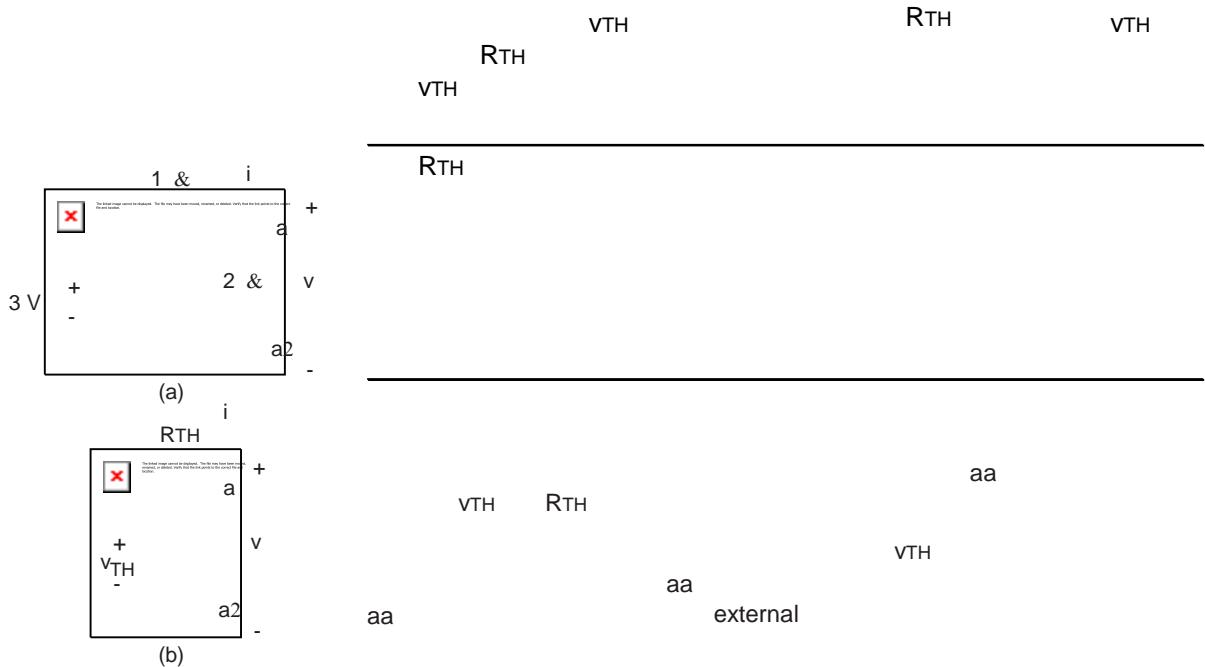
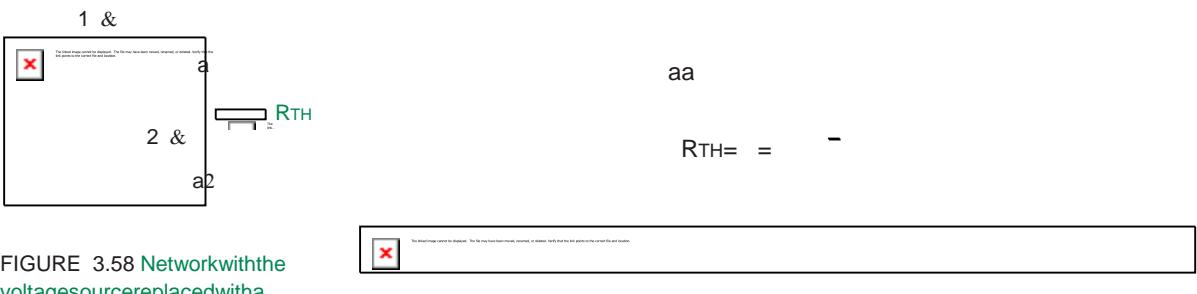


FIGURE 3.57 Example circuit to illustrate the Thévenin method:
 (a) a network; (b) its Thévenin equivalent network.

$$V_{TH} = \frac{+}{+} = R_{TH}$$



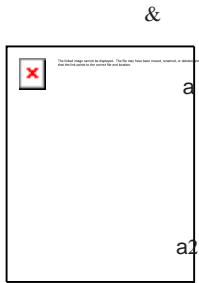


FIGURE 3.59 The resulting Thévenin equivalent circuit.

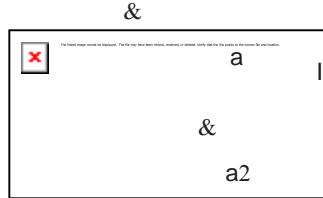
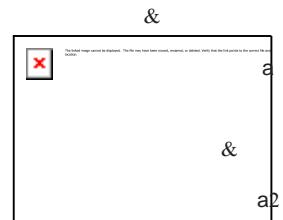


FIGURE 3.60 Circuit to illustrate the power of the Thévenin method.



method. First, suppose we are asked to determine the current I_1 through the voltage source in the circuit in Figure 3.60.

Let us use the Thévenin method to obtain the desired current. To apply the Thévenin method, we will replace the network to the left of the voltage source (that is, to the left of the aa terminal pair, and depicted in Figure 3.61a) with its Thévenin equivalent network (depicted in Figure 3.61b). Once this replacement is made, as illustrated in Figure 3.62, then, the current I_1 can be written by inspection as

$$I_1 = \frac{V_{TH} - 1V}{R_{TH}} \quad (3.118)$$

V_{TH} and R_{TH} are the Thévenin equivalent parameters. The first step of the Thévenin method is to measure V_{TH} . As shown in Figure 3.63, V_{TH} is the open-circuit voltage measured at the aa port.

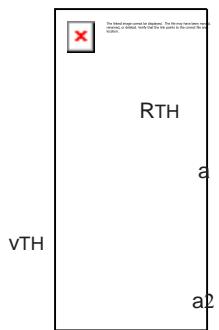


FIGURE 3.61 Thévenin equivalent network.

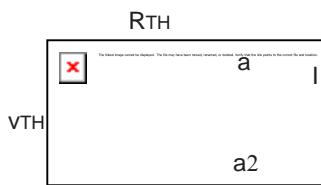


FIGURE 3.62 Circuit with network to the left of the aa terminal pair replaced with its Thévenin equivalent.

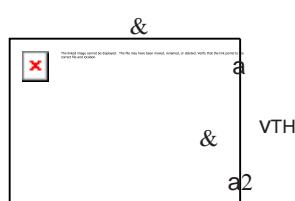


FIGURE 3.63 Open-circuit voltage.

Since the 2-A current flows through both the 2-resistors in Figure 3.63, v_{TH} can be written by inspection as

$$v_{TH} = 2A \times 2 = 4V.$$

By the second step of the Thévenin method, the resistance R_{TH} is found by measuring the resistance of the open-circuit network seen from the a -port with the independent current sources set to zero; that is, with the current source replaced with an open circuit as illustrated in Figure 3.64. It is easy to see that

$$R_{TH} = 2.$$

Having determined the Thévenin equivalent parameters v_{TH} and R_{TH} , we can now obtain I_1 from Equation 3.118 as

$$I_1 = \frac{4V - 1V}{2} = \frac{3}{2} A.$$

Notice that in this example the Thévenin method has allowed us to tackle a given problem (the circuit in Figure 3.60) by splitting it into three trivial subproblems, namely, the circuits in Figures 3.63, 3.64, and 3.62.

To further illustrate the power of the Thévenin method, suppose that the 1-V source in Figure 3.60 is replaced by a 10-resistor as illustrated in Figure 3.65, and we are asked to find the current I_2 through the 10-resistor.

We first notice that the network to the left of the terminal pair aa' in Figure 3.65 is unchanged from that in Figure 3.60. Thus, from the viewpoint of determining a parameter relating to the network on the right side of the aa' terminal pair, we can replace that network on the left with its Thévenine equivalent determined previously as illustrated in Figure 3.66.

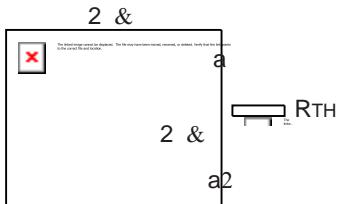


FIGURE 3.64 Measuring

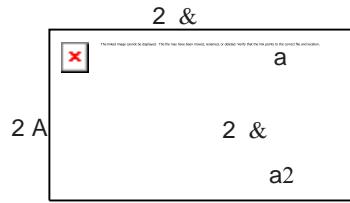


FIGURE 3.65 Circuit to further illustrate the power of the Thévenin method.

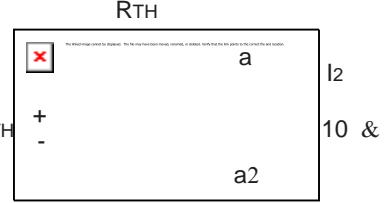


FIGURE 3.66 Circuit with network to the left of the terminal pair replaced with its Thévenine equivalent.

The current I_2 can be quickly determined from the network in Figure 3.66a as

$$I_2 = \frac{V_{TH}}{R_{TH} + 10}$$

We know that $V_{TH} = 4\text{V}$ and $R_{TH} = 2\Omega$, and so $I_2 = 1/3\text{A}$.



example 3.22 bridge circuit Determine the current I in the branch b in the circuit in Figure 3.67.

There are many approaches that we can take to obtain the current I . For example, we could apply the node method and determine the node voltages at nodes a and b and thereby determine the current I . However, since we are interested only in the current I , a full blown node analysis is not necessary; rather we will find the Thévenin equivalent network for the subcircuit to the left of the a - a terminal pair (Network A) and for the subcircuit to the right of the b - b terminal pair (Network B), and then using these subcircuits solve for the current I .

Let us first find the Thévenin equivalent for Network A. This network is shown in Figure 3.68a. Let v_{THA} and R_{THA} be the Thévenin parameters for this network.

We can find v_{THA} by measuring the open-circuit voltage at the a - a port in the network in Figure 3.68b. We find by inspection that

$$v_{THA} = 1\text{V}$$

Notice that the 1-A current flows through each of the 1- Ω resistors in the loop containing the current source, and so v_1 is 1V. Since there is no current in the resistor connected to the a terminal, the voltage v_2 across that resistor is 0. Thus $v_{THA} = v_1 + v_2 = 1\text{V}$.

We find R_{THA} by measuring the resistance looking into the a - a port in the network in Figure 3.68c. The current source has been turned into an open circuit for the purpose

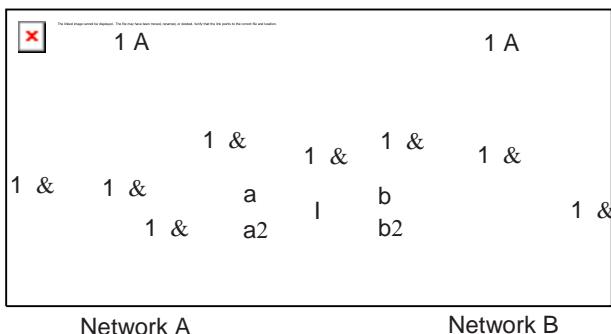


FIGURE 3.67 Determining the current in the branch b .

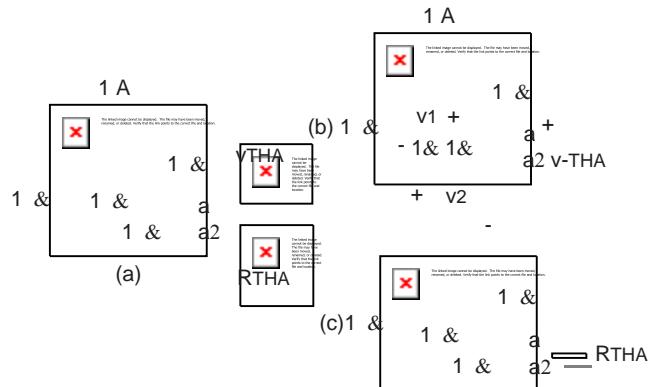


FIGURE 3.68 Finding the Thévenin equivalent for Network A.

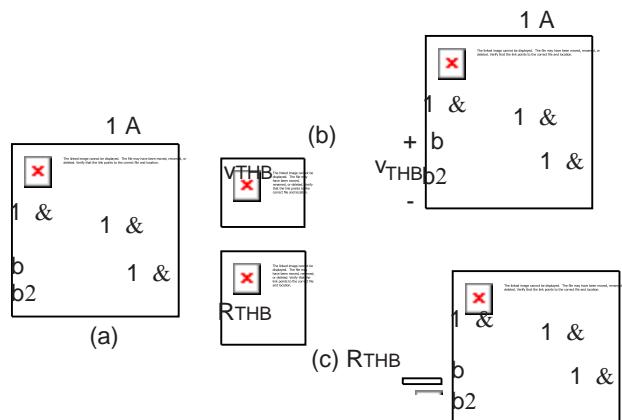


FIGURE 3.69 Finding the Thévenin equivalent for Network B.

of measuring R_{THA} . By inspection, we find that

$$R_{THA}=2.$$

Let us now find the Thévenin equivalent for Network B shown in Figure 3.69a. Let v_{THB} and R_{THB} be the Thévenin parameters for this network.

v_{THB} is the open-circuit voltage at the b_2 port in the network in Figure 3.69b. Using reasoning similar to that for v_{THA} we find

$$v_{THB}=-1V.$$

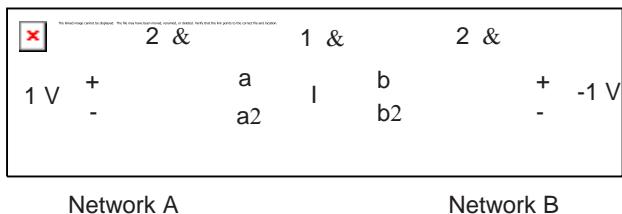


FIGURE 3.70 Networks A and B replaced by their Thévenin equivalents.

R_{THB} is the resistance looking into the bb port in the network in Figure 3.69c. By inspection,

$$R_{THB}=2.$$

Replacing Network A and Network B with their Thévenin equivalents, we obtain the equivalent circuit in Figure 3.70.

The current I is easily determined as

$$I = \frac{21V + -1(-1+V)2}{5} = \frac{2}{5} A.$$

Notice in this example we were able to solve a relatively complicated problem by combining the results of five subproblems (namely, the circuits in Figures 3.68b, 3.68c, 3.69b, 3.69c, and 3.70), each of which was solvable by inspection.

example 3.23 thévenin analysis of a circuit with a dependent source Find the Thévenin equivalent circuit for the network to the left of the aa terminal pair in Figure 3.71. Notice that this circuit contains a dependent source.

The network whose Thévenin equivalent is desired is shown in Figure 3.72. Let V_{TH} and R_{TH} be the Thévenin parameters for this network.

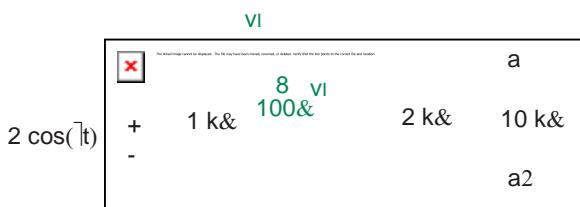
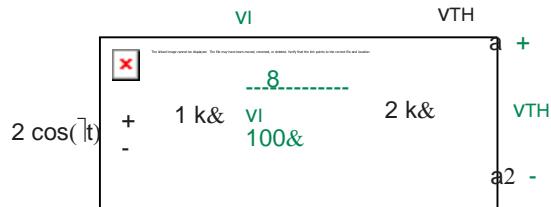


FIGURE 3.71 Thévenin analysis of a circuit with a dependent source.

FIGURE 3.72 Network to be replaced by its Thévenine equivalent.



Determining V_{TH}

We first find V_{TH} by computing the open-circuit voltage at the a port of the circuit in Figure 3.72. We will find this voltage by applying the node method. Since the current of the dependent source is expressible directly in terms of anode voltage, we can apply the node method without modification.

Figure 3.72 shows the ground node, and the two other nodes labeled with the node voltages v_I and V_{TH} . Notice that v_I is already known to be

$$v_I = 2 \cos(\omega t).$$

This completes Steps 1 and 2 of the node method.

Following Step 3 of the node method, we write KCL for Node a.

$$\frac{V_{TH}}{2k+100S} - \frac{8}{v_I} = 0.$$

Next, applying Step 4, we simplify the preceding equation to get

$$V_{TH} = -160v_I = -320\cos(\omega t).$$

Since we were interested only in the node voltage V_{TH} , we do not have to complete Step 5 of node analysis.

Determining R_{TH}

We now find R_{TH} by computing the resistance looking into the a port in the network in Figure 3.73. The independent voltage source has been turned into a short circuit for

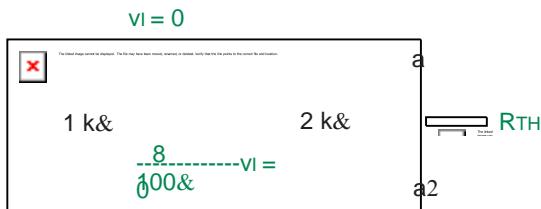


FIGURE 3.73 Determining R_{TH} .

the purpose of computing R_{TH} . The dependent source, however, is left in the circuit. Since $v_i = 0$, the current through the dependent current source is 0, and therefore, the dependent source behaves like an open circuit. Thus,

$$R_{TH} = 2k\Omega.$$

The resulting Thévenin circuit is shown in Figure 3.74.

3.6.2 THE NORTON EQUIVALENT NETWORK

An analogous derivation to that in Section 3.6.1 gives rise to the Norton equivalent network. Recall that our goal is to find the $v - i$ relation for the network in Figure 3.75a so that we can replace the network with a simple equivalent circuit that yields the same $v - i$ relation as the original network. To find the $v - i$ relationship, this time we apply a test voltage v_{test} to the circuit, as in Figure 3.75b, and find the resultant current i_t . Using superposition, the two subcircuits needed to find i_t are shown in Figure 3.75c and 3.75d. In 3.75c, v_{test} is set to zero and we measure i_a . In 3.75d, all independent sources are reset to zero and we measure i_b . Then,

$$i_t = i_a + i_b.$$

From Figure 3.75c,

$$i_a = -i_{sc} \quad (3.119)$$

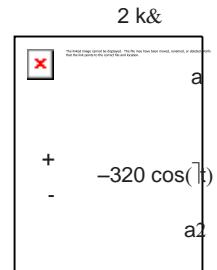
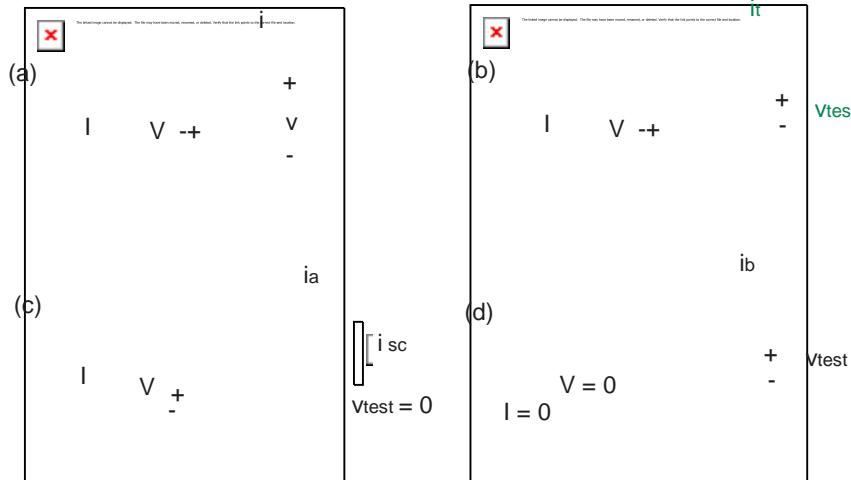


FIGURE 3.74 Resulting Thévenin circuit.

FIGURE 3.75 Derivation of Norton network.

where i_{sc} is the current that flows in the short circuit across the network terminals in response to the internal sources, and thus is the short circuit current. From Figure 3.75d,

$$i_b = \frac{V_{test}}{R_t} \quad (3.120)$$

where R_t is the net resistance measured between the terminals when all internal independent sources are set to zero. Because this calculation and the one in Figure 3.55 are identical (except for a change in excitation) the parameter R_t is obviously the same in both calculations.

To complete the derivation, we find by superposition

$$i_t = i_a + i_b = -i_{sc} + \frac{V_{test}}{R_t} \quad (3.121)$$



FIGURE 3.76 The Norton equivalent network.

As in the Thévenin derivation, this equation can be interpreted in terms of a circuit. It states that the terminal current is the sum of two components: a current source i_{sc} and a resistor current $\frac{V_{test}}{R_t}$. Hence the Norton equivalent network, Figure 3.76, has a current source in parallel with a resistor. Examination of either the two equations, Equations 3.121 and 3.115, or the two figures, Figures 3.56 and 3.76 show that there is a simple relation between V_{oc} and i_{sc} . Working from the figures, we can calculate the open-circuit voltage of each circuit to find

$$V_{oc} = i_{sc} R_t. \quad (3.122)$$

Thus it is a simple matter to change from one of these equivalent networks to the other.

To determine the Norton parameters for some circuit, against two independent measurements are required. The source parameter i_{sc} could be found by applying a short to the circuit terminals and measuring the resultant current. The resistance parameter is measured as before in Equation 3.117. Note that the source parameters i_{sc}, V_{oc} are related by Equation 3.122, so measuring or calculating any two of V_{oc}, i_{sc} and R_t is sufficient to characterize both the Norton and the Thévenin model. In particular, it is often convenient to find R_t from two simple terminal measurements on the circuit

$$R_t = \frac{V}{i_{sc}} \quad (3.123)$$

In summary, the Norton method allows us to abstract the behavior of a linear network at a given pair of terminals as a current source in parallel with a resistor. The current source in parallel with the resistor is called the Norton equivalent circuit of the network. Like the Thévenin equivalent, the Norton

equivalent circuit can also be used to model the effect of the given network on other circuits external to the network.

A Method for Determining the Norton Equivalent Circuit The Norton equivalent circuit for any linear network at a given pair of terminals consists of a current source i_{N} in parallel with a resistor R_N . The current i_{N} and resistance R_N can be obtained as follows:

1. i_{N} can be found by applying a short at the designated terminal pair on the original network and calculating or measuring the current through the short circuit.
2. R_N can be found in the same manner as R_{TH} , that is, by calculating or measuring the resistance of the open-circuit network seen from the designated terminal pair with all independent sources internal to the network set to zero; that is, with voltage sources replaced with short circuits, and current sources replaced with open circuits.

example 3.24 norton equivalent Figure 3.77a shows a network and Figure 3.77b shows its Norton equivalent network viewed from the network's a port. Determine the values of i_{N} and R_N .

By the first step of the Norton method, the current i_{N} is given by applying a short at the aa terminal pair and calculating the current through the short circuit. Figure 3.78 shows the network with a short at the aa terminal pair.

The current through the short at the aa terminal pair in Figure 3.78 is given by

$$i_{\text{N}} = \frac{3V}{12} = 3A.$$

By the second step of the Norton method, the resistance R_N is found by measuring the resistance of the open-circuit network seen from the aa port with the independent voltage sources set to zero. The network with the voltage source replaced with a short is shown in Figure 3.79.

The resistance viewed from the aa port is given by

$$R_N = \frac{12}{2} = 6\Omega.$$

The resulting Norton equivalent circuit is drawn in Figure 3.80.

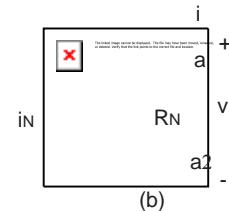
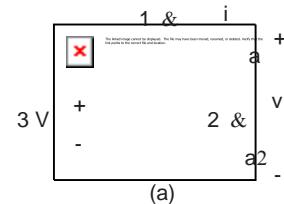


FIGURE 3.77 Norton equivalent network: (a) a network; (b) its Norton equivalent network.

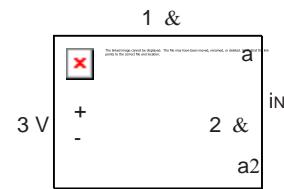


FIGURE 3.78 Determining i_{N} .

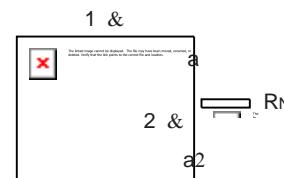


FIGURE 3.79 Determining R_N .

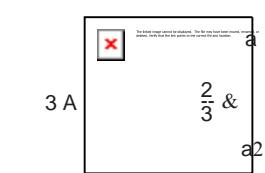


FIGURE 3.80 Resulting Norton equivalent circuit.

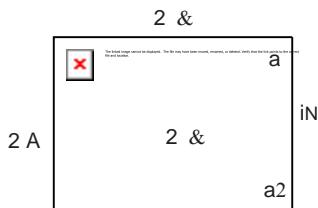
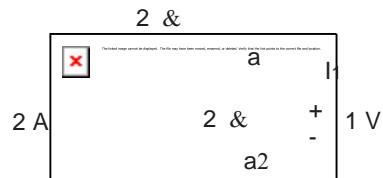
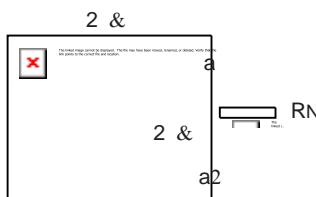
FIGURE 3.82 Determining i_N .

FIGURE 3.81 Circuit for applying the Norton method.

FIGURE 3.83 Determining R_N .

parallel with a resistance of value R_N . The first step of the Norton method is to measure i_N , which is the short-circuit current measured at the short circuit applied at the port as shown in Figure 3.82. Since all of the 2-A current flows through the short,

$$i_N = 2 \text{ A}.$$

By the second step of the Norton method, the resistance R_N is found by measuring the resistance of the open-circuit network seen from the $a-a'$ port with the current source replaced with an open circuit as illustrated in Figure 3.83. It is easy to see that

$$R_N = 2 \Omega.$$

The resulting Norton equivalent circuit is depicted in Figure 3.84.

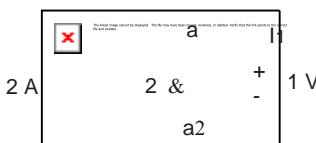
Having determined the Norton equivalent circuit, we can now obtain I_1 by connecting this equivalent circuit to the source on the right-hand side of the $a-a'$ terminal pair as shown in Figure 3.85.

Since the voltage across the 2-resistor is 1 V, the current through the 2-resistor is 0.5 A. By applying KCL at Node a, we get

$$-2A + 0.5A + I_1 = 0.$$

Or, $I_1 = 1.5A$.

FIGURE 3.84 Resulting Norton equivalent circuit.

FIGURE 3.85 Connecting back the Norton equivalent circuit to determine I_1 .

example 3.26 norton equivalent network Let us revisit the example in Figure 3.71 and this time around determine the Norton equivalent circuit for the network to the left of the $a-a'$ terminal pair. Let I_N and R_N be the Norton parameters for this network.

Determining I_N

We first find I_N by computing the short-circuit current through the short placed at the $a-a'$ terminal pair as depicted in Figure 3.86. I_N can be determined by inspection as

$$I_N = -\frac{8}{100} VI = -\frac{4}{100} \cos(\omega t).$$

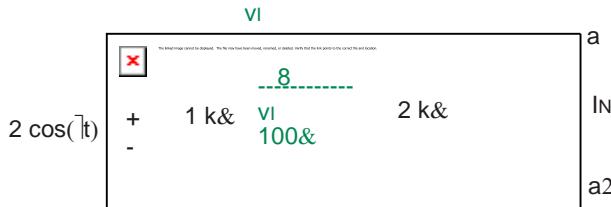


FIGURE 3.86 DeterminingIN.

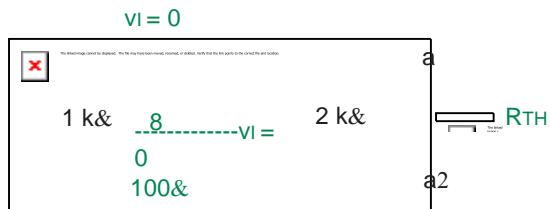


FIGURE 3.87 DeterminingRN.

DeterminingRN

We now find RN by computing the resistance looking into the a port in the network in Figure 3.87. As computed in the Thévenin inversion of this example,

$$R_N = 2k\Omega.$$

The resulting Norton circuit is shown in Figure 3.88.

3.6.3 MORE EXAMPLES

Norton and Thévenin equivalents are particularly useful because often the two parameters are easy to find, as a consequence of the strong circuit constraints imposed as shown in Figures 3.55 and 3.75. This is best illustrated by an example. Suppose we are given the network in Figure 3.89a, and are asked to find the voltage across R3 for a number of different values of R3. We could just solve the whole network for each value of R3, but a simpler approach is to find the Thévenin equivalent of the network driving R3, that is, the network to the left of the points x-x. For clarity in this first example, we abstract this portion of the network in Figure 3.89b.

As we have noted, there are several ways to make the calculations, so it pays to examine the possibilities and choose the easiest route. The open-circuit voltage appears directly in the abstracted circuit, Figure 3.89b. The short-circuit current can be found from Figure 3.89c, and R_t from 3.89d. By inspection from Figure 3.89d,

$$R_t = R_1 R_2. \quad (3.124)$$

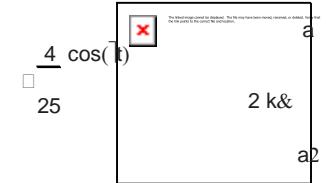


FIGURE 3.88 ResultingNorton equivalentcircuit.

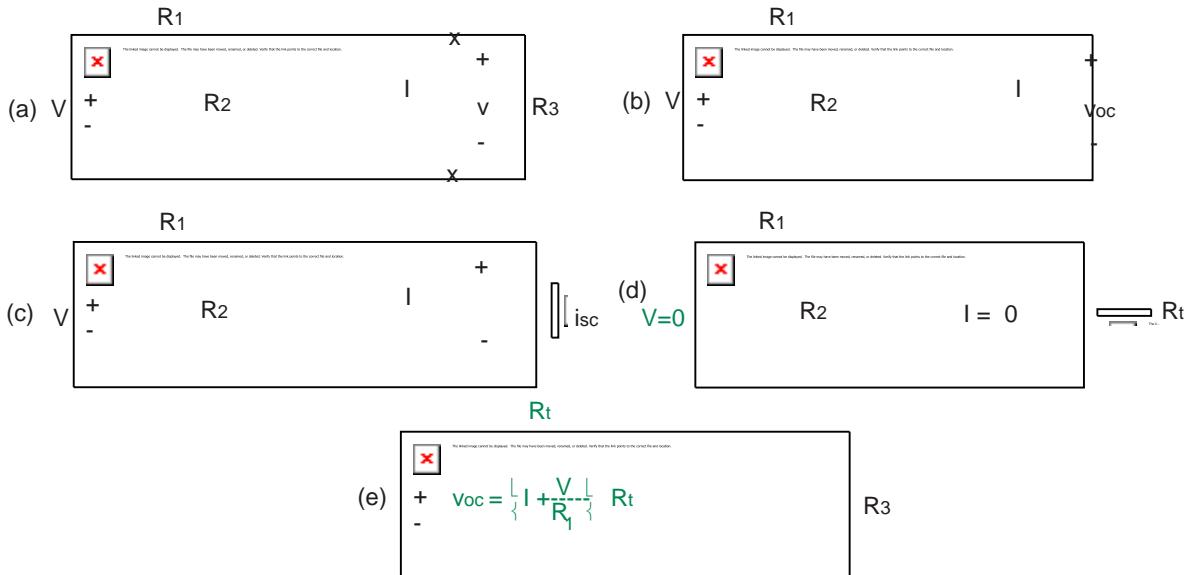


FIGURE 3.89 Example in which we are to find voltage across R_3 for several different values of R_3 .

In Figure 3.89c, the short-circuit constraint makes the calculation of I_{sc} for this particular topology easy. Because of the short circuit, R_2 can have no voltage across it, hence has no current flowing through it. Now by superposition,

$$I_{sc} = I + V/R_1. \quad (3.125)$$

The calculation of V_{oc} from Figure 3.89b is straightforward, but a step more complicated than the preceding ones, so normally it would not be attempted. But for completeness, superposition of the two sources gives

$$V_{oc} = V \frac{R_2}{R_1 + R_2} + \frac{I(R_1 R_2)}{R_1 + R_2}. \quad (3.126)$$

It is clearly easier to find V_{oc} from Equations 3.122, 3.124, and 3.125:

$$V_{oc} = (I + V/R_1)R_t. \quad (3.127)$$

Hence the complete circuit with the left half replaced by its Thévenin equivalent is as shown in Figure 3.89e. Now the voltage across R_3 for the various values of R_3 can be found by inspection. It should be noted that the Norton equivalent would have been just as effective in this problem. Also note that the circuit constraints imposed by the definitions of R , I_{sc} , and V_{oc} often make the calculations of these parameters very easy, even in complicated networks.

example 3.27 bridge circuit Another example is shown in Figure 3.90a. This is a bridge circuit, often used in the laboratory to measure values of unknown resistors by comparing against known standard resistors. We want to find the voltage across R_5 , and then find the condition on the other resistor values that will make this voltage zero. Direct application of nodal analysis is quite messy, so we will seek an alternative method.

To solve, find the Thévenine equivalent of the circuit facing R_5 , that is, the circuit shown in Figure 3.90b. The circuit now consists of two independent voltage dividers connected across a common voltage source V . The layout of the dividers is not quite as straightforward as in Figure 2.36 but, topologically, they are the same. Hence we can calculate the two voltage-dividers' voltages v_a and v_b by inspection; then subtract to find v_{oc} .

$$v_{oc} = v_a - v_b = V \cdot \frac{R_3}{R_1 + R_3} - \frac{R_4}{R_2 + R_4} . \quad (3.128)$$

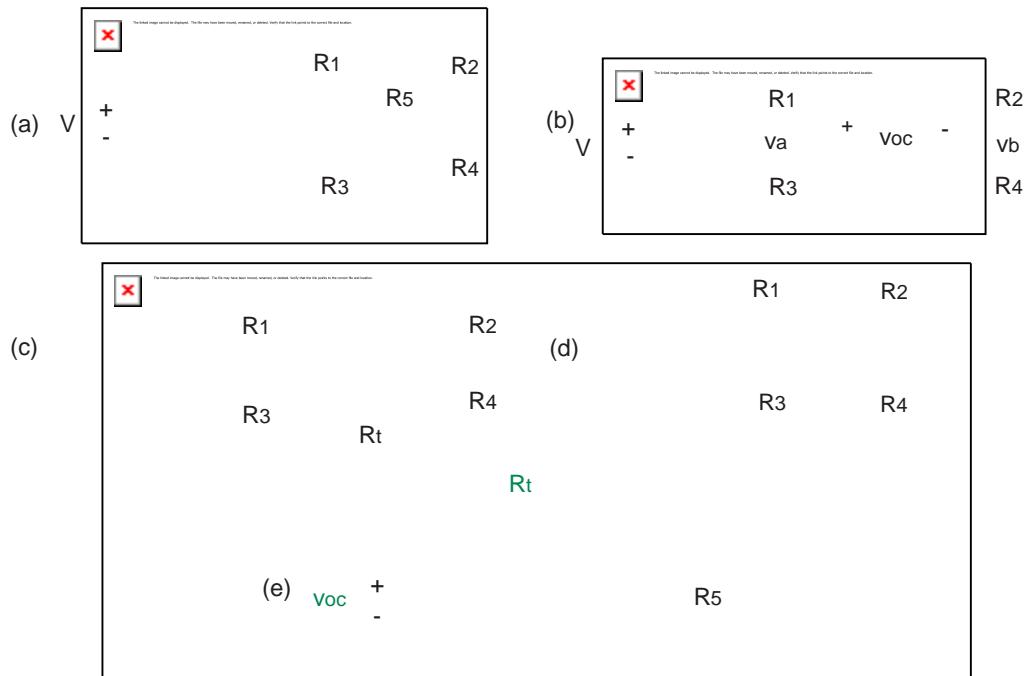


FIGURE 3.90 Example: A bridge circuit.

Now find the Thévenine equivalent resistance with V_s set to zero, that is, for the circuit shown in Figure 3.90c. This is identical to the circuit in 3.90d,

$$R_t = (R_1 R_3) + (R_2 R_4). \quad (3.129)$$

The complete circuit can now be drawn as in Figure 3.90e. It is clear that the voltage across R_5 will be zero if V_{oc} is zero, that is, if

$$\frac{R_3}{R_1 + R_3} = \frac{R_4}{R_2 + R_4} \quad (3.130)$$

or equivalently

$$\frac{R_3}{R_1} = \frac{R_4}{\frac{R_2}{2}}. \quad (3.131)$$

Thus if R_5 is replaced by a voltmeter, the circuit can be used to find an unknown resistor, say R_3 , in terms of three known resistors. Make one of the resistors, say R_1 , a decade box with known resistance values and adjust until the voltmeter reads zero. The value of R_3 is then given by Equation 3.131.

Two closing comments: First, note that the identity of all voltages and currents inside the network that is replaced by the Thévenin or Norton circuit in general lose their identity; only the terminal voltage and current are preserved. Thus, for example, the current through R_3 in Figure 3.90a does not appear as any identifiable current flowing in the Thévenin circuit in Figure 3.90e. Second, if one wishes to measure the Thévenin or Norton parameters of a system in the laboratory, two independent measurements are required in order to specify the two parameters in the model. In addition, certain practical issues must be faced. For example, it is unwise, in fact dangerous, to apply a short circuit to a large battery such as an automobile storage battery in an attempt to measure the short-circuit current suggested in Figure 3.75b. A better procedure is to first measure the open-circuit voltage, then measure the terminal voltage when some known resistor is connected to the battery. These two measurements can then be used to find R_t .

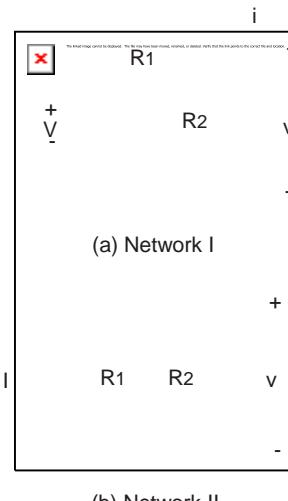


FIGURE 3.91 Two simple networks: (a) Network I; (b) Network II.

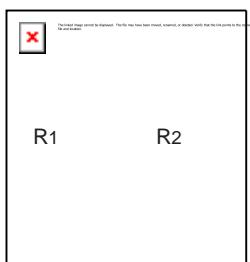


FIGURE 3.92 Equivalent resistance of the network.

example 3.28 norton and thévenin equivalents

As another simple example, let us find the Norton and Thévenine equivalent networks and their i -characteristics for the two circuits shown in Figure 3.91.

Let us start with Network A. First, let us find the Thévenine equivalent circuit. Shorting the voltage source results in the circuit shown in Figure 3.92. Therefore, $R_{TH} = R_N = R_1 R_2 / (R_1 + R_2)$, where R_{TH} and R_N are the Thévenin and Norton equivalent resistors, respectively. From the voltage-divider relationship, open circuit voltage V_{oc} is $V_R2 / (R_1 + R_2)$. This yields the Thévenine equivalent circuit on the left-hand side of Figure 3.93.

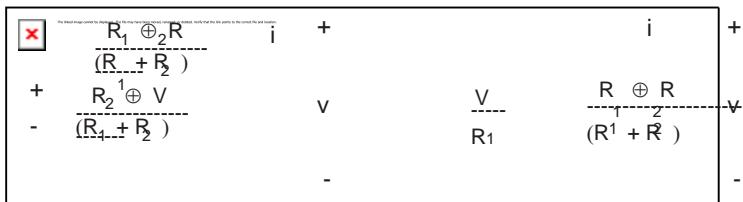


FIGURE 3.93 Equivalent networks.

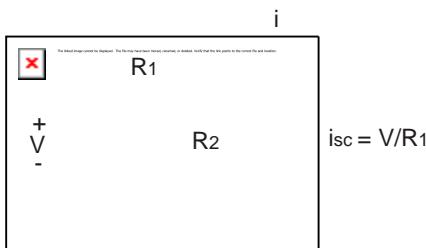


FIGURE 3.94 Shortcircuitcurrent.

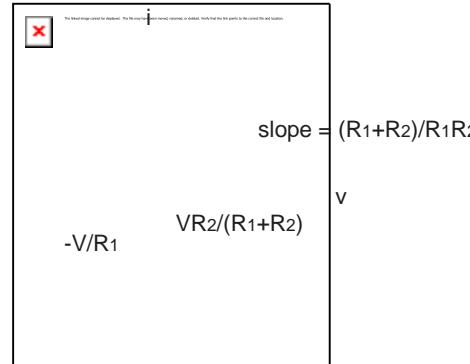


FIGURE 3.95 Thei–vcharacteristicsofthenetwork.

Now, let us find the Norton equivalent circuit for Network A. Referring to Figure 3.94, the short-circuit current i_{sc} is V/R_1 . Therefore, the Norton equivalent network is as shown on the right-hand side of Figure 3.93.

The v_i curve of the circuit must pass through points $(v_{oc}, 0)$ and $(0, -i_{sc})$, as shown in Figure 3.95.

Let us now analyze Network B. Turning off the current source results in the circuit shown in Figure 3.92, which yields $R_1R_2/(R_1+R_2)$ as the equivalent resistance for both the Thévenin and Norton equivalent networks. The open-circuit voltage is IR .

Thus, $v_{oc} = R_1I/(R_1+R_2)$. As illustrated in Figure 3.96, all of the current will flow through the branch with zero resistance, that is, $i_{sc} = I$.

The equivalent networks are shown in Figure 3.97, and the v_i characteristics are shown in Figure 3.98.

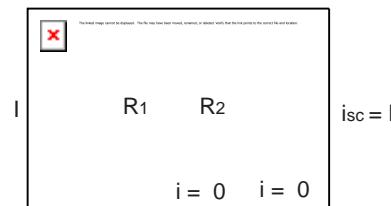


FIGURE 3.96 Short-circuitcurrent.

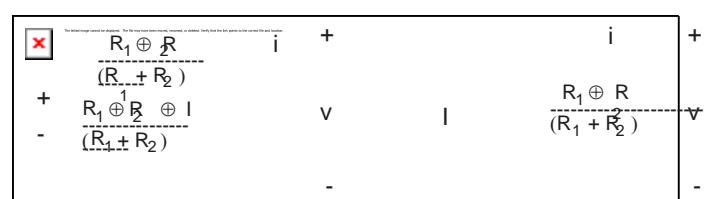


FIGURE 3.97 Equivalentnetworks.

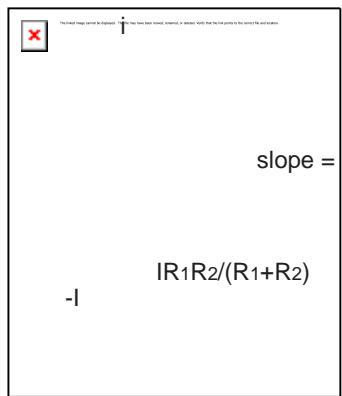


FIGURE 3.98 Thev–i characteristics of the network.

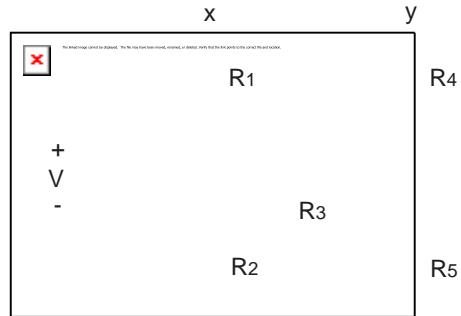


FIGURE 3.99 Resistive circuit.

example 3.29 a different approach using the thévenin method ThenetworkshowninFigure3.99wassolvedearlier usingtheThéveninmethod(seeFigure3.90).Inthisexample,wewillsolvethesame circuitusingtheThéveninmethod, butwithaslightlydifferentapproach.

Making the observation that the voltages at points x and y are the same, we can transform the circuit into the equivalent circuit shown in Figure 3.100. We can then transform the circuits in Figures 3.100a and 3.100b into their Théveninequivalent networks. Figure 3.100a will have a source voltage of $VR_2/(R_1+R_2)$ and an equivalent resistance of $R_1 R_2$. Figure 3.100b will have a source voltage of $VR_5/(R_4+R_5)$ and an equivalent resistance of $R_4 R_5$.

The new circuit is shown in Figure 3.101. Notice that the new circuit is much easier to analyze. We leave the rest of the analysis as an exercise for you.

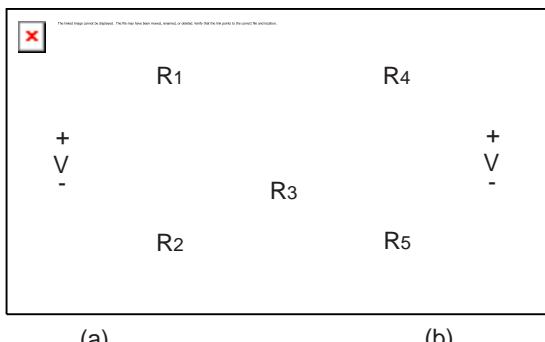


FIGURE 3.100 Equivalent circuit with two voltage sources.

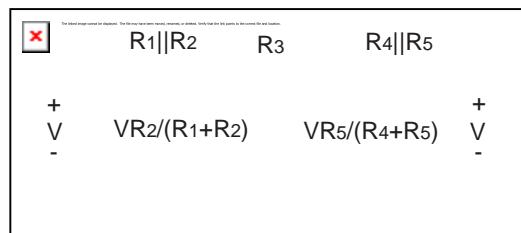


FIGURE 3.101 Equivalent Thévenin circuit.

3.7 SUMMARY

In the node method one node is designated as a reference or ground node, and all other node voltages are measured with respect to that node. Only the KCL equations and the constituent relations need be written.

In the loop method currents are defined to flow in loops. Loop currents are defined until all branches are traversed by at least one current. Only KVL equations need be written.

Superposition means that if the circuit is linear, multi-source networks can be solved for one source at a time by setting all other independent sources to zero. Setting a voltage source to zero means replacing it with a short circuit; a current source set to zero is an open circuit. The complete response is the sum of the responses to each individual source.

For circuits with dependent sources, a practical solution is to leave all the dependent sources in the circuit. The network can then be solved for one independent source at a time by setting all other independent sources to zero, and summing the individual responses.

The Thévenin equivalent circuit for any linear network at a given pair of terminals consists of a voltage source in series with a resistor. The element value for the Thévenin equivalent voltage source can be found by calculating or measuring at the designated terminal pair on the original network the open-circuit voltage. The equivalent resistance can be calculated or measured as the resistance of the network seen from the designated terminal pair with all independent sources internal to the network set to zero.

The Nortonequivalent circuit contains a current source in parallel with a resistor. The element value for the Nortonequivalent current source can be found by calculating or measuring at the designated terminal pair on the original network the short-circuit current. As with the Thévenin equivalent resistance, the Nortonequivalent resistance can be calculated or measured as the resistance of the network seen from the designated terminal pair with all independent sources internal to the network set to zero. Note that the value of the equivalent resistance is the same for the Thévenin and Norton equivalent circuits, that is, $R_{TH} = R_N$.

Since the Thévenin equivalent voltage v_{TH} , the Nortonequivalent current i_N , and the equivalent resistance $R_{TH} = R_N$ are related as

$$v_{TH} = i_N R_{TH},$$

the element values for these equivalents can be found by calculating or measuring any two of the open-circuit voltage, the short-circuit current, or the resistance.

Circuit analysis is often simplified by applying superposition or finding Thévenin or Norton equivalents, because complicated circuits are reduced to simpler circuits, for which the solution may already be known.

EXERCISES

exercise 3.1 Write node equations for the network in Figure 3.102. Solve for the node voltages, and use these voltages to find the branch current i . To minimize errors and facilitate answer-checking, it is helpful to obtain literal expressions before substituting numerical values for the parameters:

$$V=2V \quad R_3=3 \quad R_1=2 \quad R_4=2 \quad R_2=4 \quad R_5=1$$

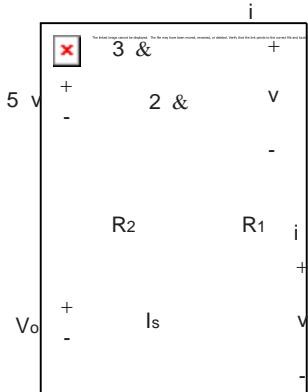


FIGURE 3.103

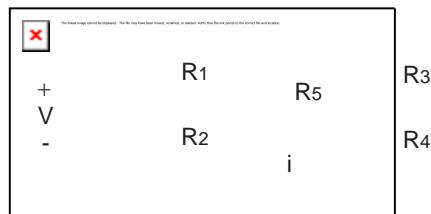


FIGURE 3.102

exercise 3.2 Find the Norton equivalent at the indicated terminals for each network in Figure 3.103.

exercise 3.3 Find the Thévenine equivalent for each network in Figure 3.104.

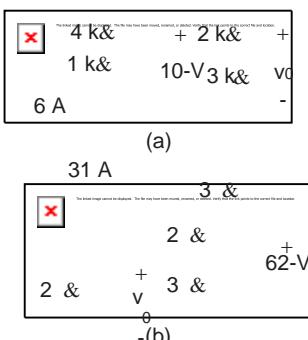


FIGURE 3.105

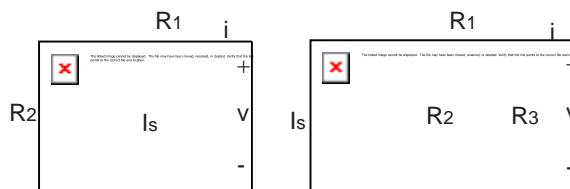
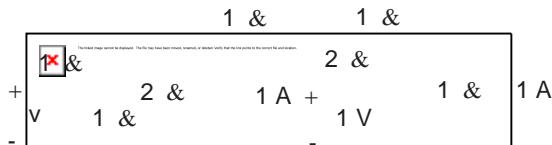


FIGURE 3.104

exercise 3.4 Find v in Figures 3.105a and 3.105b by superposition.

exercise 3.5 Use superposition to find the voltage v in the network in Figure 3.106.



exercise 3.6 Determine (and label carefully) the Thévenine equivalent for the network in Figure 3.107:

$$R_1 = 2\text{k} \quad R_2 = 1\text{k} \quad i_o = 3\text{mA} \cos(\omega t)$$

exercise 3.7 Determine and label carefully the Norton equivalent for the network in Figure 3.108.

exercise 3.8 Find the Thévenine equivalent for the circuit at the terminals AA in Figure 3.109.

exercise 3.9 The resistive network shown in Figure 3.110 is excited by two voltage sources $v_1(t)$ and $v_2(t)$.

- Express the current $i(t)$ through the 1-kilohm resistor as a function of $v_1(t)$ and $v_2(t)$.
- Determine the total energy dissipated in the 1-kilohm resistor due to both $v_1(t)$ and $v_2(t)$ from time T_1 to time T_2 .
- Derive the constraint between $v_1(t)$ and $v_2(t)$ such that the value for (b) can be computed by adding the energies dissipated when each source acts alone (that is, by superposition).

exercise 3.10 Find the Norton equivalent at the terminals marked x-x in the circuit in Figure 3.111.

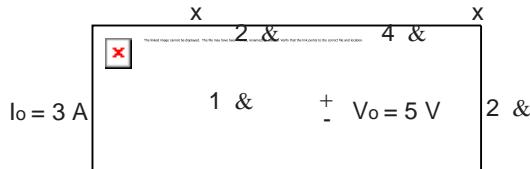


FIGURE 3.111

exercise 3.11 Find the Thévenine equivalent for the circuit in Figure 3.112 at the terminals AA.

FIGURE 3.106

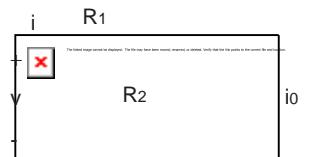


FIGURE 3.107

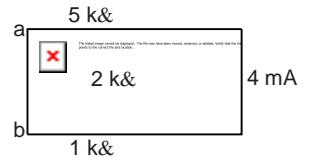


FIGURE 3.108

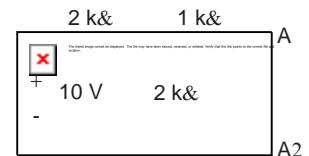


FIGURE 3.109

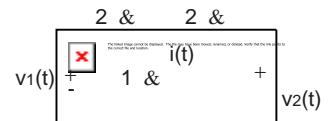


FIGURE 3.110

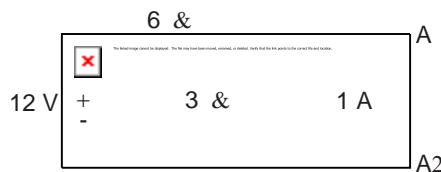


FIGURE 3.112

exercise 3.12 In the network in Figure 3.113, find an expression for v_2 .

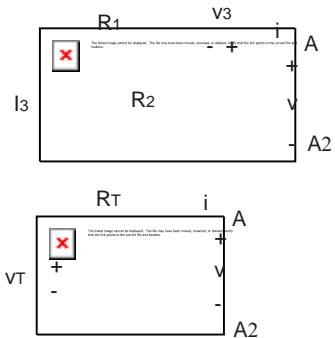


FIGURE 3.114

FIGURE 3.113

exercise 3.13 The networks in Figure 3.114 are equivalent (that is, have the same v_i relation) at terminals A – A₂. Find v_T and R_T .

exercise 3.14 For each of the circuits in Figure 3.115 give the number of independent node variables needed for a solution of the problem by the node method.

exercise 3.15 For the circuit shown in Figure 3.116, write a complete set of node equations for the voltages v_a , v_b , and v_c . Use conductance instead of resistance. Simplify the equations by collecting terms and arranging them in the “standard” form for linear equations in n unknowns. (Do not solve the equations.)

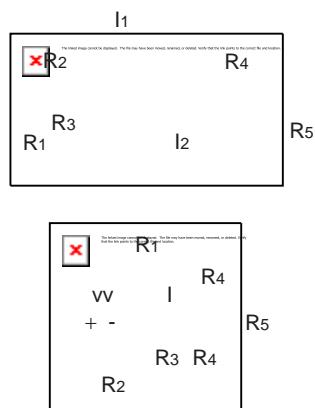


FIGURE 3.115

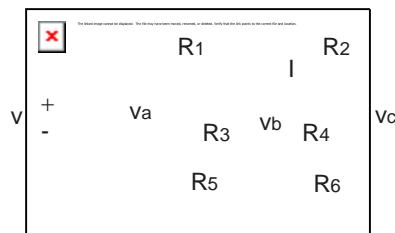


FIGURE 3.116

exercise 3.16 For the circuit shown in Figure 3.117, use superposition to find v in terms of the R 's and source amplitudes.

exercise 3.17 Find the Thévenine equivalent of the circuit in Figure 3.118 at the terminals indicated.

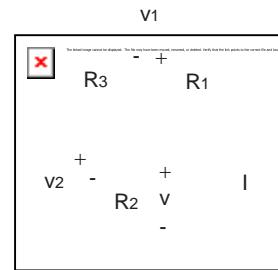
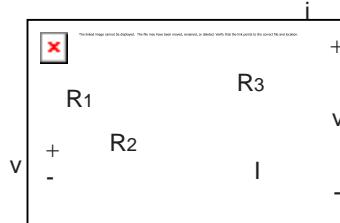


FIGURE 3.117

FIGURE 3.118

exercise 3.18 In the circuit shown in Figure 3.119 there are five nodes, only three of which are independent. Taken node E as a reference node, and treat nodes A, B, and D as the independent nodes.

- Write an expression for v_C , the voltage on node C, in terms of v_A , v_B , v_D , and v_1 .
- Write a complete set of node equations that can be solved to find the unknown voltages in the circuit. (Do not solve the set of equations but do group them neatly.)

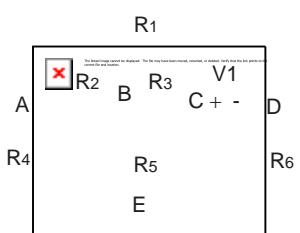


FIGURE 3.119

exercise 3.19 Consider the circuit in Figure 3.120.

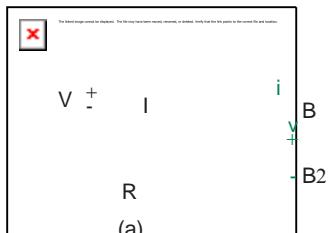
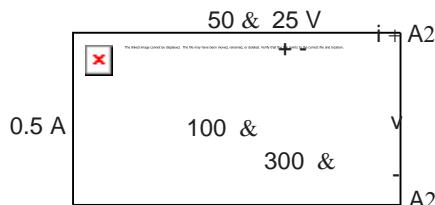


FIGURE 3.120

- Find a Nortone equivalent circuit for this circuit at terminals A \rightarrow A.
- Find the Thévenine equivalent circuit corresponding to your answer in (a).

exercise 3.20 Measurements made on terminals B \rightarrow B of a linear circuit in Figure 3.121a, which is known to be made up only of independent voltage sources and current sources, and resistors, yield the current-voltage characteristics shown in Figure 3.121b.

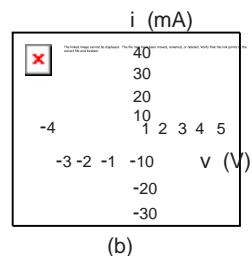


FIGURE 3.121

a) Find the Thévenine equivalent of this circuit.

b) Over what portions, if any, of the v_i characteristics does this circuit absorb power?

exercise 3.21

a) Write in standard form the minimum number of node equations needed to analyze the circuit in Figure 3.122.

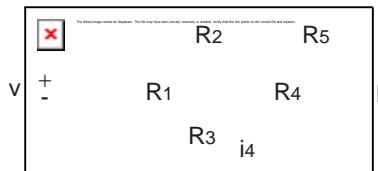


FIGURE 3.122

b) Determine explicitly the current i_4 .

exercise 3.22

a) Find the Thévenine equivalent of the circuit in Figure 3.123.

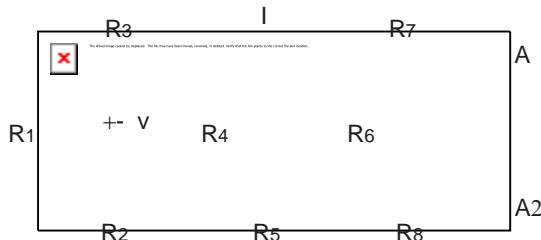


FIGURE 3.123

b) Find the Nortonequivalent of the circuit in Figure 3.124.

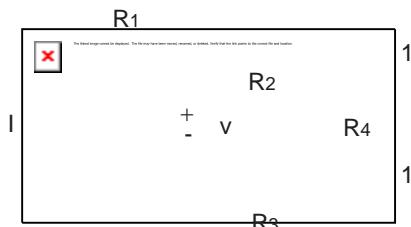


FIGURE 3.124

exercise 3.23

a) Find the Nortonequivalent of the circuit in Figure 3.125.

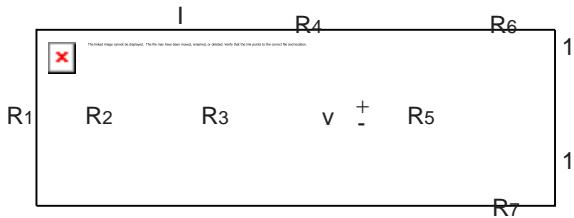


FIGURE 3.125

b) Find the Thévenine equivalent of the circuit in Figure 3.126.

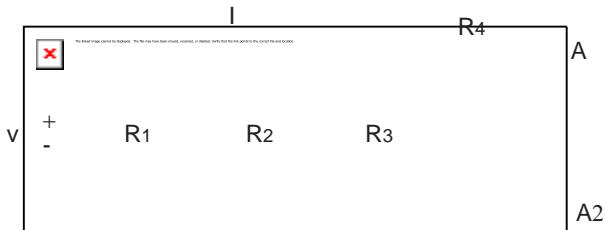


FIGURE 3.126

exercise 3.24 Find the Thévenine equivalent circuit as seen from the terminals a–b in Figure 3.127.

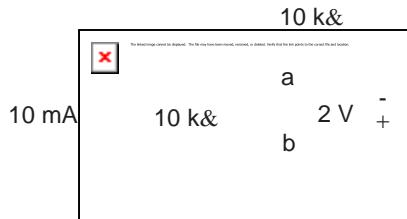


FIGURE 3.127

exercise 3.25 Find the node potential E in Figure 3.128.

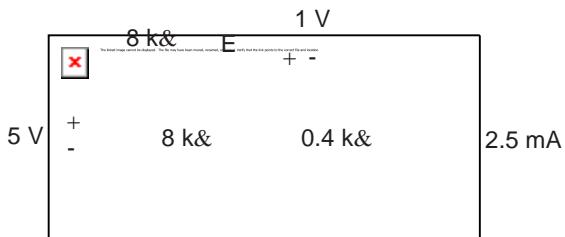


FIGURE 3.128

exercise 3.26 For the circuit in Figure 3.129, write the node equations. Do not solve, but write in matrix form: source terms on the left, unknown variables on the right.

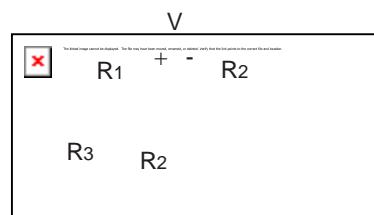


FIGURE 3.129

exercise 3.27 Find v_1 by superposition for the circuit in Figure 3.130.

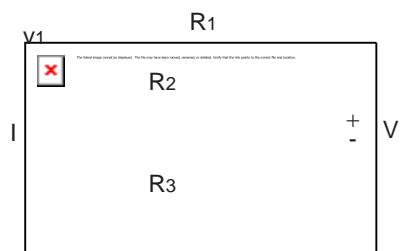


FIGURE 3.130

PROBLEMS

problem 3.1 A fuse is a wire with a positive temperature coefficient of resistance (in other words, its resistance increases with temperature). When a current is passed through the fuse, power is dissipated in the fuse, which raises its temperature.



FIGURE 3.131

Use the following data to determine the current I_0 at which the fuse (in Figure 3.131) will blow (that is, its temperature goes up without limit).

Fuse Resistance:

$$R = 1 + aT$$

$$a = 0.001/C$$

T = Temperature rise above ambient

Temperature rise:

$$T = \beta P$$

$$\beta = 1/225 \text{ } ^\circ\text{C/W}$$

P = power dissipated in fuse

problem 3.2

a) Prove, if possible, each of the following statements. If a proof is not possible, illustrate the failure with a counter-example and restate the theorem with a suitable restriction so it can be proved.

- In a network containing only linear resistors, every branch voltage and branch current must be zero.
- The equivalent of a one-port network containing only linear resistors is a linear resistor.

b) To demonstrate that you understand superposition, construct an example that shows explicitly that a network containing a nonlinear resistor will not be superposition. You may select any nonlinear element (provided you show that it is nonlinear) and any simple network containing that element.

problem 3.3 Find V_o in Figure 3.132. Solve by (1) node method, (2) superposition. All resistances are in ohms.

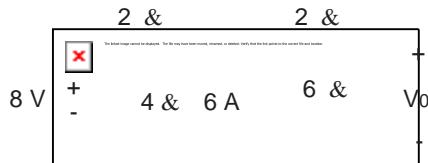


FIGURE 3.132

problem 3.4 Consider Figure 3.132. Find the Norton equivalent of the network as seen at the terminals on the right.

problem 3.5

a) Find R_{eq} , the equivalent resistance "looking into" the terminals on the right of the circuit in Figure 3.133.

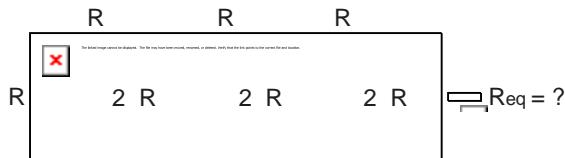
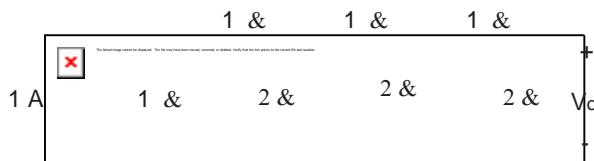


FIGURE 3.133

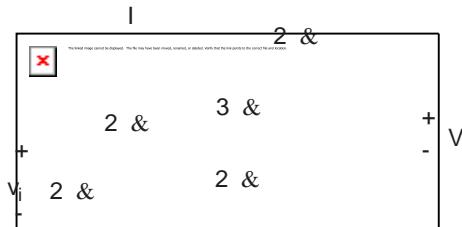
b) Find the Thévenin equivalent, looking into the terminals on the right of the circuit in Figure 3.134.

FIGURE 3.134

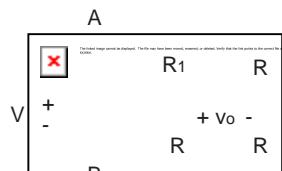


problem 3.6 Find v_i for $i=3A$, $V=2V$ in Figure 3.135. Strategy: To avoid numerical errors, derive expressions in literal form first, then check dimensions.

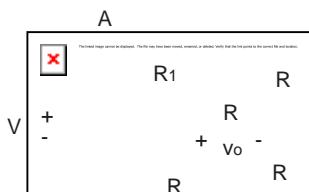
FIGURE 3.135



problem 3.7 For the circuits in Figures 3.136a and 3.136b:



(a)



(b)

FIGURE 3.136

FIGURE 3.137

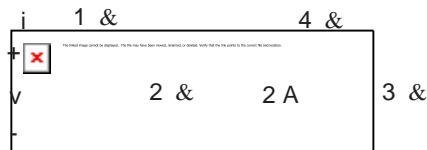
a) Find v_o for $R_1=R$.

b) Find v_o for $R_1=R$.

c) Find the Thévenine equivalent for the network to the right of points AB, assuming $R_1=R$.

problem 3.8

a) Determine the equation relating i to v in Figure 3.137.



b) Plot the $v-i$ characteristics of the network.

c) Draw the Thévenine equivalent circuit.

d) Draw the Norton equivalent circuit.

problem 3.9 In Figure 3.138, find v_o via (a) superposition, (b) the node method.

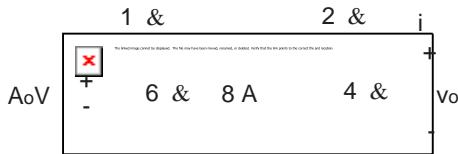


FIGURE 3.138

problem 3.10 Use the following three different methods to find i in Figure 3.139:

- 1) Nodemethod

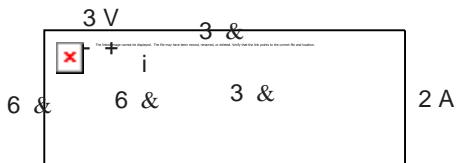


FIGURE 3.139

- 2) Superposition
- 3) AlternateThévenin/Nortontransformations

problem 3.11 A student is given an unknown resistive network as illustrated in Figure 3.140. She wishes to determine whether the network is linear, and if it is, what its Thévenine equivalent is.

The only equipment available to the student is a voltmeter (assumed ideal), 100-k Ω and 1-M Ω test resistors that can be placed across the terminals during a measurement (see Figure 3.141).



Unknown network

FIGURE 3.140

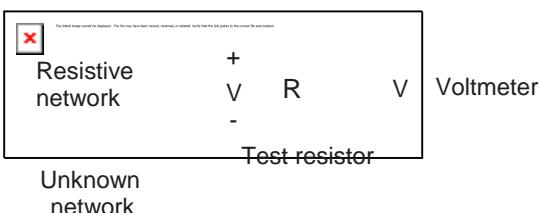


FIGURE 3.141

The following data were recorded:

Test Resistor	Voltmeter Reading
Absent	1.5V
100k	0.25V
1M	1.0V

What should the student conclude about the network from these results? Support your conclusion with plots of the network voltage characteristics.

problem 3.12

a) Devise an electrical circuit of voltage sources and resistors that will "calculate" the balance point (center of mass) of the massless bar shown in Figure 3.142, for three arbitrary masses hung at three arbitrary places along the bar. We want the circuit to generate a voltage that is proportional to the position of the balance point. Write the equation for your network, and show that it performs the required calculation. (Work with conductances and superposition for a simple solution.)

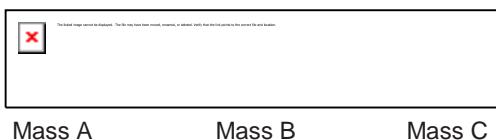


FIGURE 3.142

b) Extend your result in part (a) to two dimensions; that is, devise a new network (which will have more voltage sources and more resistors than above) that can find the center of mass of a triangle with arbitrary weights hanging from its three corners. The network will now have to give you two voltages, one representing the x-coordinate and the other the y-coordinate of the center of mass. This system is a barycentric coordinate calculator, and can be used as the input for video games, or to simulate trichromatic color vision in the human eye.

problem 3.13

a) Find the Thévenin equivalent for the network in Figure 3.143 at the terminals CB. The current source is a controlled source. The current flowing through the current



FIGURE 3.143

source is βI_1 , where β is some constant. (We will discuss controlled sources in more detail in the later chapters.)

b) Now suppose you connect a load resistor across the output of your equivalent circuit as shown in Figure 3.144. Find the value of R_L which will provide the maximum power transfer to the load.

problem 3.14 You have been hired by the MIT DAC Corporation to write a product description for a new 4-bit digital-to-analog converter resistance ladder. Because of mask tolerances in VLSI chips, each resistor shown in Figure 3.145 is guaranteed to be only within 3% of its nominal value. That is, if R_0 is the nominal design resistance, then each resistance labeled R can have a resistance anywhere in the range $(1 \pm .03)R_0$ and each resistance labeled $2R$ can have a resistance anywhere in the range $(2 \pm .06)R_0$.

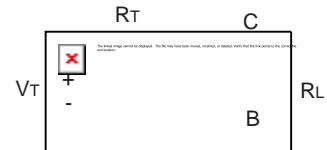


FIGURE 3.144

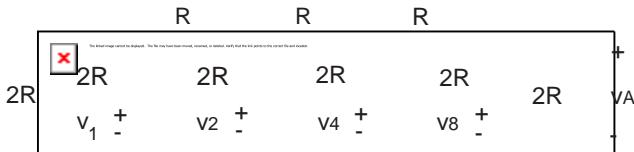


FIGURE 3.145

You are to write an honest description of the accuracy of this product. Remember that if you overstate the accuracy, your company will have many returns from dissatisfied customers, whereas if you understate the accuracy, your company won't have any customers.

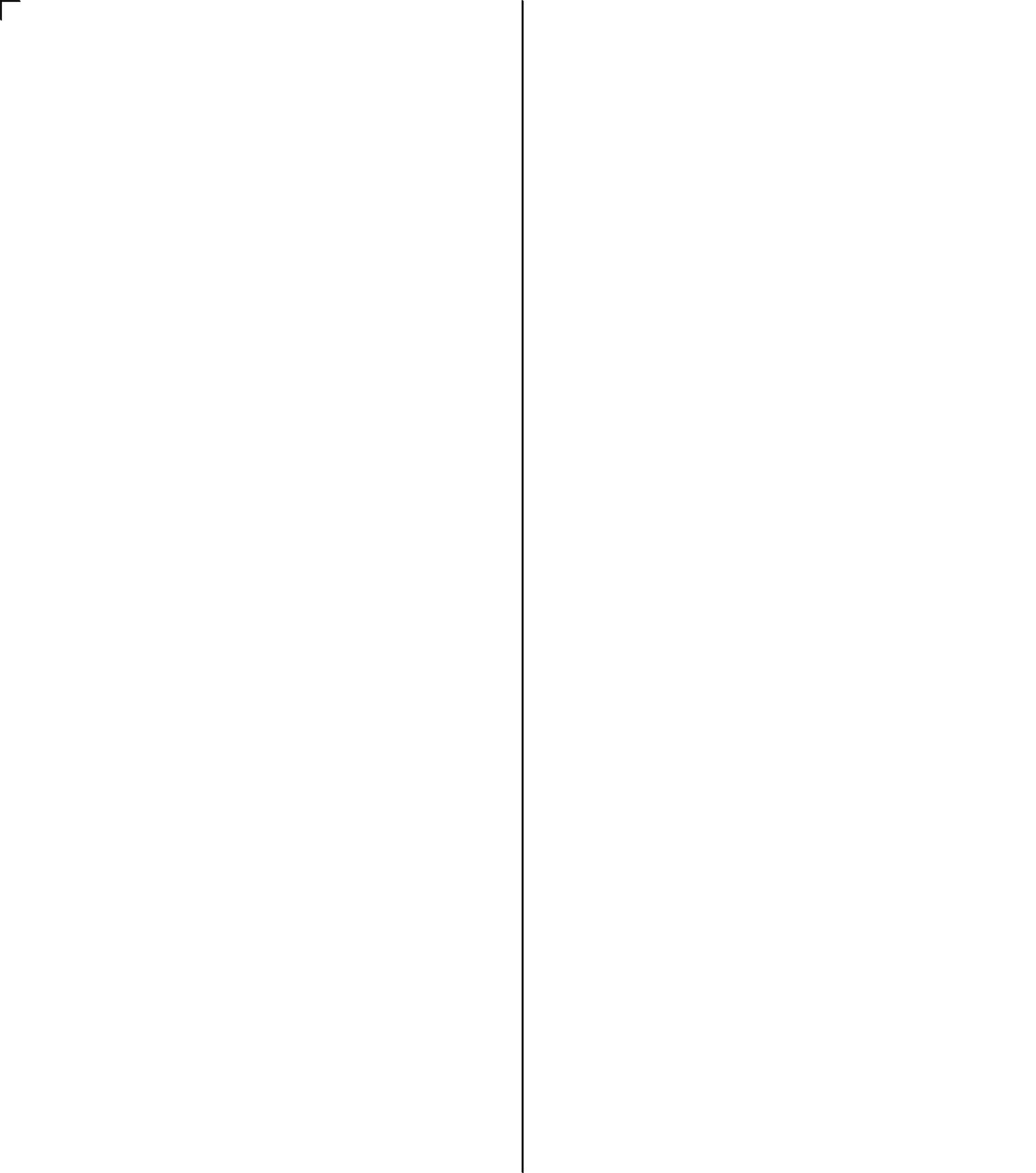
Note: Part of this problem is to describe what the problem is. How should accuracy be specified? Is there an error level that is clearly unacceptable? Does your product avoid that error level? Is there an obvious "worst case" that can be easily analyzed? Have fun. And remember, common sense is an important ingredient of sound engineering.

problem 3.15 You have a 6-volt battery (assumed ideal) and a 1.5-volt flashlight bulb, which is known to draw 0.5 A when the bulb voltage is 1.5 V (in Figure 3.146).

Design a network of resistors to go between the battery and the bulb to give $v_s = 1.5$ V when the bulb is connected, yet ensure that v_s does not rise above 2 V when the bulb is disconnected.



FIGURE 3.146



chapter 4

4.1 INTRODUCTION TO NONLINEAR ELEMENTS

4.2 ANALYTICAL SOLUTIONS

4.3 GRAPHICAL ANALYSIS

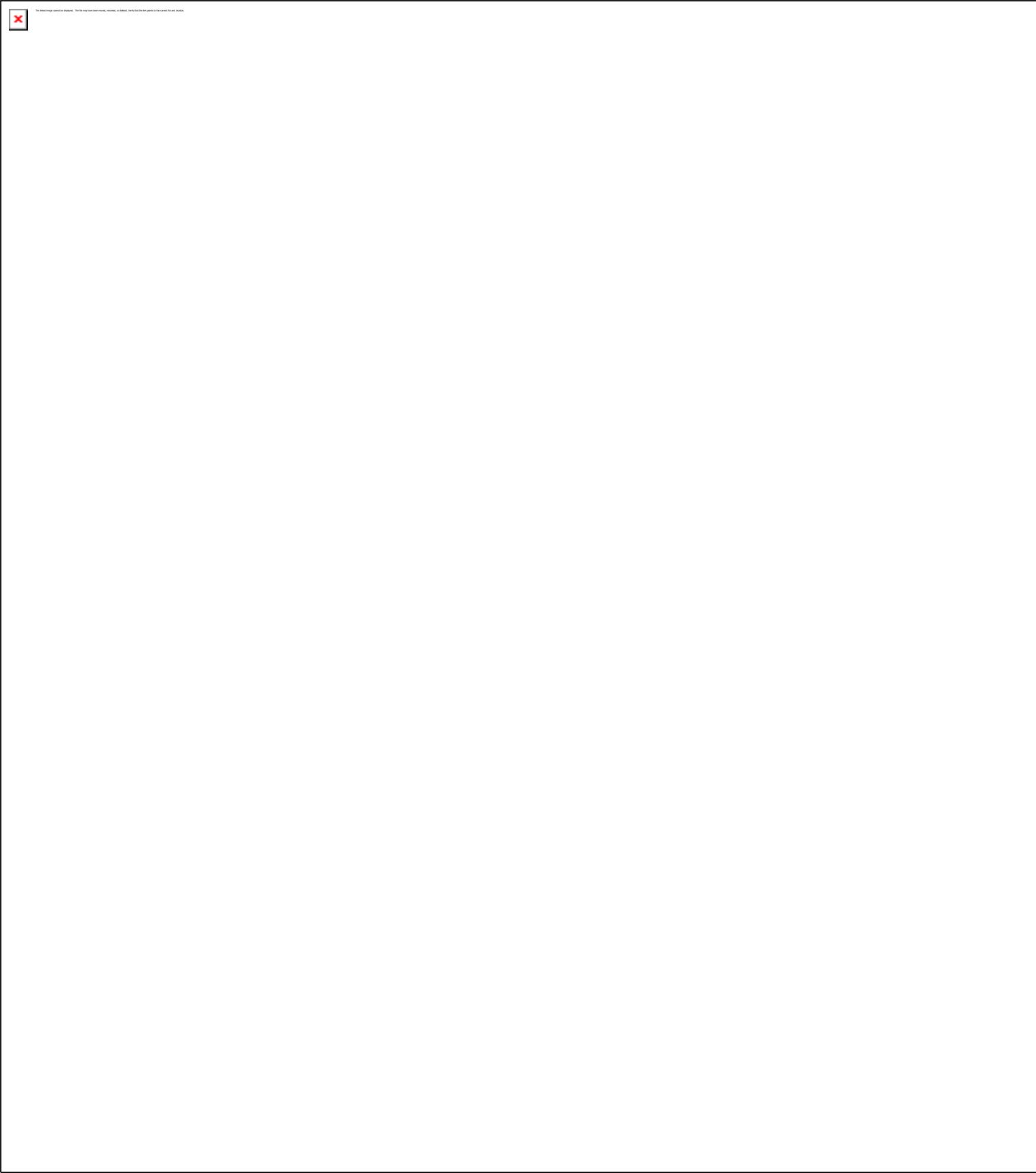
4.4 PIECEWISE LINEAR ANALYSIS

4.5 INCREMENTAL ANALYSIS

4.6 SUMMARY

EXERCISES

PROBLEMS



4

analysis of nonlinear circuits

Thus far we have discussed a variety of circuits containing linear devices such as resistors and voltage sources. We have also discussed methods of analyzing linear circuits built out of these elements. In this chapter, we extend our repertoire of network elements and corresponding analysis techniques by introducing an nonlinear two-terminal device called a nonlinear resistor. Recall, from Section 1.5.2, a nonlinear resistor is an element that has a nonlinear, algebraic relation between its instantaneous terminal current and its instantaneous terminal voltage. A diode is an example of a device that behaves like a nonlinear resistor. In this chapter, we will introduce methods of analyzing general circuits containing nonlinear elements, trying whenever possible to use analysis methods already introduced in the preceding chapters. Chapter 7 will develop further the basic ideas on nonlinear analysis and Chapter 8 will expand on the concept of incremental analysis introduced in this chapter. Chapter 16 will elaborate on diodes.

4.1 INTRODUCTION TO NONLINEAR ELEMENTS

Before we begin our analysis of nonlinear resistors, we will describe a few examples of several nonlinear resistive devices, by their $i-v$ characteristics, just as we did for the resistor, the battery, etc. The first of the nonlinear devices that we discuss is the diode. Figure 4.1 shows the symbol for a diode. The diode is a two-terminal, nonlinear resistor whose current is exponentially related to the voltage across its terminals.

An analytic expression for the nonlinear relationship between the voltage v_D and the current i_D for the diode is the following:

$$i_D = I_s(e^{v_D/V_{TH}} - 1). \quad (4.1)$$

For silicon diodes the constant I_s is typically 10^{-12} A and the constant V_{TH} is typically 0.025 V. This function is plotted in Figure 4.2.

An analytic expression for the relationship between voltage v_H and current i_H for another hypothetical nonlinear device is shown in Equation 4.2. In the equation, I_k is a constant. The relationship is plotted in Figure 4.3.

$$i_H = I_k v_H^{\frac{3}{2}}. \quad (4.2)$$



FIGURE 4.1 The symbol for a diode.

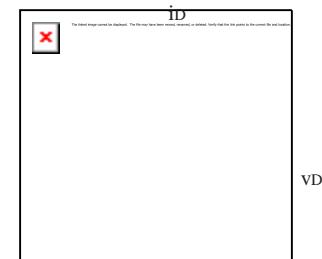


FIGURE 4.2 v - i -characteristics of a silicon diode.

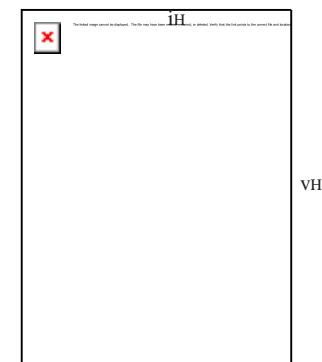


FIGURE 4.3 Another nonlinear v - i -characteristics.

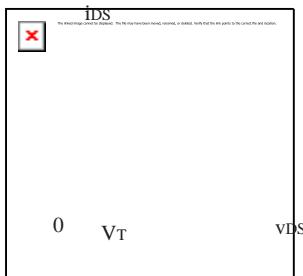


FIGURE 4.4 The $v-i$ -characteristics for a square law device.

The $v-i$ -relationship for yet another two-terminal nonlinear device is shown in Equation 4.3. Figure 8.11 in Chapter 8 introduces such a nonlinear device. For this device the current is related to the square of the terminal voltage. In this equation, K and V_T are constants. The variables i_{DS} and v_{DS} are the terminal variables for the device. The relationship is plotted in Figure 4.4.

$$i_{DS} = \begin{cases} K(v_{DS}-V_T)^2 & \text{for } v_{DS} \geq V_T \\ 0 & \text{for } v_{DS} < V_T \end{cases} . \quad (4.3)$$

example 4.1 square law device

For the nonlinear resistor device following the square law in Figure 4.4, determine the value of i_{DS} for $v_{DS}=2V$. We are given that $V_T=1V$ and $K=4mA/V^2$.

For the parameters that we have been given ($v_{DS}=2V$ and $V_T=1V$), it is easy to see that

$$v_{DS} \geq V_T.$$

From Equation 4.3, the expression for i_{DS} when $v_{DS} \geq V_T$ is

$$i_{DS} = \frac{K(v_{DS}-V_T)^2}{2}.$$

Substituting the known numerical values,

$$i_{DS} = \frac{4 \times 10^{-3}(2-1)^2}{2} = 2mA.$$

How does i_{DS} change if v_{DS} is doubled?

If v_{DS} is doubled to 4V,

$$i_{DS} = \frac{K(v_{DS}-V_T)^2}{2} = \frac{4 \times 10^{-3}(4-1)^2}{2} = 18mA$$

In other words, i_{DS} increases to 18mA when v_{DS} is doubled.

What is the value of i_{DS} if v_{DS} is changed to 0.5V?

For $v_{DS}=0.5V$ and $V_T=1V$,

$$v_{DS} < V_T.$$

From Equation 4.3, we get

$$i_{DS}=0.$$

When operating within some circuit, the current through our square law device is measured to be 4mA. What must be the voltage across the device?

We are given that $i_{DS} = 4\text{mA}$. Since there is a current through the device, the equation that applies is

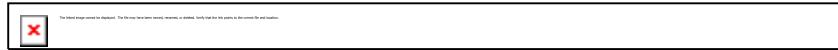
$$i_{DS} = K(v_{DS} - V_T)^2.$$

Substituting known values,

$$8 \times 10^{-3} = \frac{4 \times 10^{-3}(v_{DS} - 1)^2}{2}$$

Solving for v_{DS} , we get

$$v_{DS} = 3\text{V}.$$



example 4.2 diode example For the diode shown in Figure 4.1,

determine the value of i_D for $v_D = 0.5\text{V}, 0.6\text{V}$, and 0.7V . We are given that $V_{TH} = 0.025\text{V}$ and $I_S = 1\text{pA}$.

From the device law for a diode given in Equation 4.1, the expression for i_D is

$$i_D = I_S(e^{v_D/V_{TH}} - 1).$$

Substituting the known numerical values for $v_D = 0.5\text{V}$, we get

$$i_D = 1 \times 10^{-12}(e^{0.5/0.025} - 1) = 0.49\text{mA}.$$

Similarly, for $v_D = 0.6\text{V}$, $i_D = 26\text{mA}$, and for $v_D = 0.7\text{V}$, $i_D = 1450\text{mA}$. Notice the dramatic increase in current as v_D increases beyond 0.6V .

What is the value of i_D if $v_D = -0.2\text{V}$?

$$i_D = I_S(e^{v_D/V_{TH}} - 1) = 1 \times 10^{-12}(e^{-0.2/0.025} - 1) = -0.9997 \times 10^{-12} \quad \text{A.}$$

The negative sign for i_D simply reflects the fact that when v_D is negative, so is the current.

When operating within some circuit, the current through the diode is measured to be 8mA . What must be the voltage across the diode?

We are given that $i_D = 8\text{mA}$. Using the diode equation, we get

$$8 \times 10^{-3} = I_S(e^{v_D/V_{TH}} - 1) = 1 \times 10^{-12}(e^{v_D/0.025} - 1).$$

Simplifying, we get

$$e^{v_D/0.025} = 8 \times 10^9 + 1.$$

Taking logs on both sides, and solving for V_D , we get

$$V_D = 0.025 \ln(8 \times 10^9 + 1) = 0.57V.$$

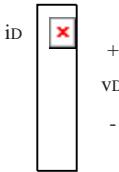


FIGURE 4.5 An nonlinear device.

example 4.3 another square law device problem

The nonlinear device shown in Figure 4.5 is characterized by this device equation:

$$i_D = 0.1 V_D^2 \text{ for } V_D \geq 0, \quad (4.4)$$

i_D is given to be 0 for $V_D < 0$.

Given that $V = 2V$, determine i_D for the circuit in Figure 4.6.

Using the device equation for $V_D \geq 0$,

$$i_D = 0.1 V_D^2 = 0.1 \times 2^2 = 0.4A \quad (4.5)$$

The nonlinear device is connected to some arbitrary circuit as shown in Figure 4.7. Following the associated variables discipline, the branch variables v_B and i_B for the device are defined as shown in the same figure. Suppose that a measurement reveals that $i_B = -1mA$. What must be the value of v_B ?

Notice that the polarity of the branch variables has been reversed in Figure 4.7 from those in Figure 4.5. With this definition of the branch variables, the device equation becomes

$$-i_B = 0.1 v_B^2 \text{ for } v_B \leq 0. \quad (4.6)$$

Furthermore, i_B is 0 for $v_B > 0$.

Given that $i_B = -1mA$, Equation 4.6 yields

$$-(-1 \times 10^{-3}) = 0.1 v_B^2 \text{ where } v_B \leq 0.$$

In other words, $v_B = -0.1V$.

Given that $V = 2V$, determine i for the circuit in Figure 4.8.

Since the voltage across each of the nonlinear devices connected in parallel is $V_D = 2V$, the current through each nonlinear device is the same as that calculated in Equation 4.5. In other words,

$$i_1 = i_2 = 0.4A.$$

Therefore, $i = i_1 + i_2 = 0.8A$.

FIGURE 4.6 A circuit containing the nonlinear device.

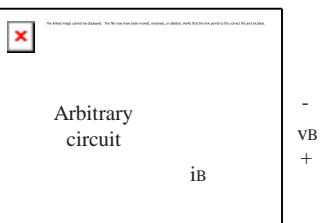


FIGURE 4.7 The nonlinear device connected to an arbitrary circuit.

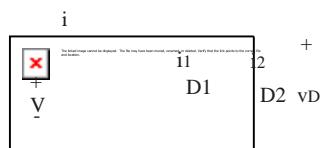


FIGURE 4.8 Nonlinear devices connected in parallel.

Given the analytic expression for the characteristic of a nonlinear device, such as that for the diode in Equation 4.1, how can we calculate the voltages and currents in a simple circuit such as Figure 4.9? In the following sections we will discuss four methods for solving such nonlinear circuits:

1. Analytical solutions
2. Graphical analysis
3. Piecewise linear analysis
4. Incremental or small signal analysis

4.2 ANALYTICAL SOLUTIONS

We first try to solve the simple nonlinear resistor circuit in Figure 4.9 by analytical methods. Assume that the hypothetical nonlinear resistor in the figure is characterized by the following v_i relationship:

$$\begin{aligned} i_D &= K v_D^2 \text{ for } v_D > 0 \\ i_D &= 0 \quad \text{for } v_D \leq 0. \end{aligned} \quad (4.7)$$

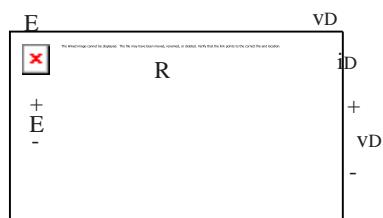
The constant K is positive.

This circuit is amenable to a straightforward application of the node method. Recall that the node method and its foundational Kirchhoff's voltage and current laws are derived from Maxwell's Equations with no assumptions about linearity. (Note, however, that the superposition method, the Thévenin method, and the Norton method do require a linearity assumption.)

To apply the node method, we first choose a ground node and label the node voltages as illustrated in Figure 4.10. v_D is our only unknown node voltage.

Next, following the node method, we write KCL for the node that has an unknown node voltage. As prescribed by the node method, we will use KVL and the device relation ($i_D = K v_D^2$) to obtain the currents directly in terms of the node voltage differences and element parameters. For the node with voltage v_D ,

$$\frac{v_D - E + i}{R} = 0 \quad (4.8)$$



Nonlinear resistor

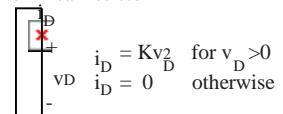


FIGURE 4.9 A simple circuit with a nonlinear resistor.

FIGURE 4.10 The nonlinear circuit with the ground node chosen and node voltages labeled.

Note that this is not quite our node equation, because of the presence of the i_D term. To get the node equation we need to substitute for i_D in terms of node voltages. Recall that the nonlinear device v_i relationship is

$$i_D = K_v \frac{v_D^2}{R} \quad (4.9)$$

Note that this device equation applies for positive v_D . We are given that $i_D = 0$ when $v_D \leq 0$.

Substituting the nonlinear device v_i relationship for i_D in Equation 4.8, we get the required node equation in terms of the node voltages:

$$\frac{v_D - E}{R} + K_v \frac{v_D^2}{R} = 0. \quad (4.10)$$

For our device, note that Equation 4.9 holds only for $v_D > 0$. For $v_D \leq 0$, $i_D \neq 0$.

Simplifying Equation 4.10, we obtain the following quadratic equation.

$$RKv_D^2 + v_D - E = 0.$$

Solving for v_D and choosing the positive solution

$$v_D = \frac{-1 + \sqrt{1 + 4RK(E)}}{2RK} \quad (4.11)$$

The corresponding expression for i_D can be obtained by substituting the previous expression for v_D into Equation 4.9 as follows:

$$i_D = K_v \frac{-1 + \sqrt{1 + 4RK(E)}}{2RK} \quad (4.12)$$

It is worth discussing why we ignored the negative solution. As shown in Figure 4.11, two mathematical solutions are possible when we solve Equations 4.10 and 4.9. However, the dotted curve in Figure 4.11 is part of

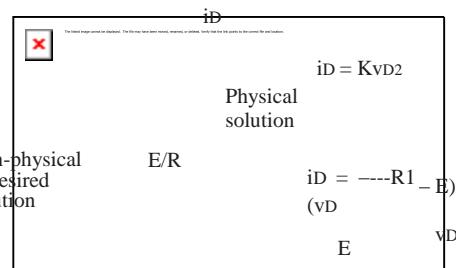


FIGURE 4.11 Solutions to equations Equations 4.10 and 4.9.

Equation 4.9 but not the physical device. Because, recall, Equation 4.9 applies only for positive v_D . When E is negative, i_D will be equal to 0 and v_D will be equal to E .

example 4.4 one nonlinear device, several sources, and resistors Shown in Figure 4.12 is a circuit of no obvious value, which we use to illustrate how to solve nonlinear circuits with more than one source present, using the nonlinear analysis method just discussed. Let us assume that we wish to calculate the nonlinear device current i_D .

Assume that the nonlinear device is characterized by the following relationship:

$$\begin{aligned} i_D &= K v_D^2 \quad \text{for } v_D > 0 \\ i_D &= 0 \quad \text{for } v_D \leq 0. \end{aligned} \tag{4.13}$$

The terminal variables for the nonlinear device are defined as shown in Figure 4.9, and the constant K is positive.

Linear analysis techniques such as superposition cannot be applied to the whole circuit because of the nonlinear element. But because there is only one nonlinear device, it is permissible to find the Thévenin (or Norton) equivalent circuit faced by the nonlinear device (see Figures 4.13a and b), because this part of the circuit is linear. Then we can compute easily the terminal voltage and current for the nonlinear device using the circuit in Figure 4.13b from Equations 4.11 and 4.12.

First, to find the open-circuit voltage, we draw the linear circuit as seen from the nonlinear device terminals in Figure 4.13c. Superposition or any other linear analysis method can now be used to calculate the open-circuit voltage:

$$V_{TH} = \frac{R_2}{R_1 + R_2} - I_0 R_3. \tag{4.14}$$

The Thévenin equivalent resistance, R_{TH} , the resistance seen at the terminals in Figure 4.13d, with the source set to zero is

$$R_{TH} = (R_1 || R_2) + R_3. \tag{4.15}$$

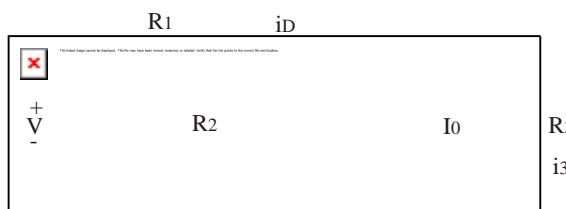


FIGURE 4.12 Circuit with several sources and resistors.

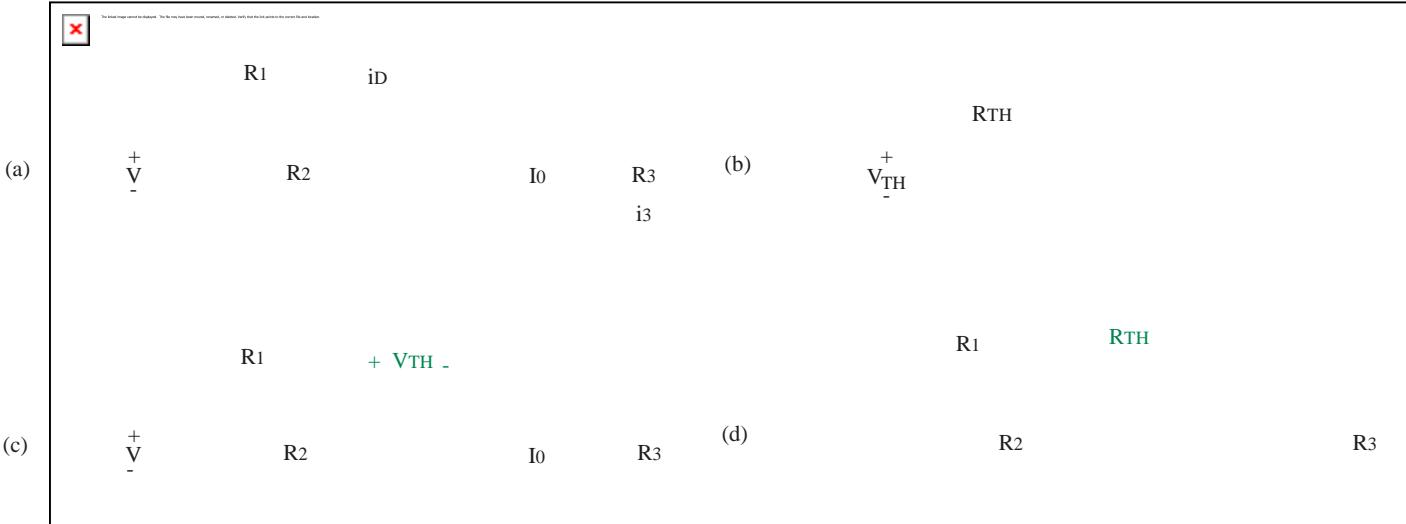


FIGURE 4.13 Analysis using Thévenin's Theorem.

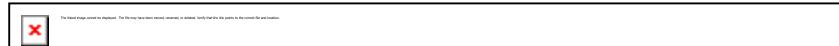
When we reconnect the nonlinear device to this Thévenin circuit, as in Figure 4.13e, we are back to a familiar example: one nonlinear device, one source, and one resistor. The desired device current i_D can be found by an nonlinear analysis method, such as that used to solve the circuit in Figure 4.9.

One further comment: If in the problem statement we had been asked to find one of the resistor currents, say i_3 , rather than i_D , then the Thévenin circuit, Figure 4.13e, would not give this current directly, because the identity of currents internal to the Thévenin network are in general lost, as noted in Chapter 3. Nonetheless, the Thévenin approach is probably the best, as it is a simple matter to work back through the linear part of the network to relate i_3 to i_D . In this case, once we have computed i_D , we can easily determine i_3 from Figure 4.13a using KCL,

$$i_3 = i_D + I_0. \quad (4.16)$$



example 4.5 node method



example 4.6 another simple nonlinear circuit

Let us try to solve the nonlinear circuit containing a diode in Figure 4.16 by analytical methods. Following the node method, we first choose the ground node and label the node voltages as illustrated in Figure 4.17.

Next, we write KCL for the node with the unknown node voltage, and substitute for the diode current using the diode equation

$$\frac{v_D - E + i_D}{R} = 0 \quad (4.18)$$

$$i_D = I_S (e^{v_D/V_{TH}} - 1). \quad (4.19)$$

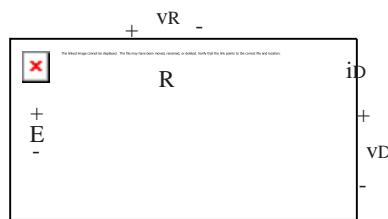


FIGURE 4.16 A simple nonlinear circuit containing a diode.

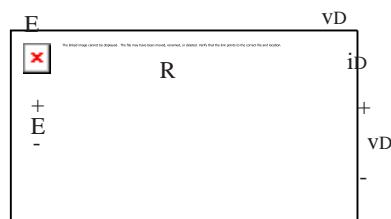


FIGURE 4.17 The circuit with the ground node and the node voltages marked.

If i_D is eliminated by substituting Equation 4.19 into Equation 4.18, the following transcendental equation results:

$$\frac{v_D - E}{R} + I_S(e^{v_D/V_{TH}} - 1) = 0.$$

This equation must be solved by trial and error. Easy via computer, but not very insightful.

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example 4.7 series-connected diodes

Referring to the series-connected diodes in Figure 4.18, determine v_1 , v_2 , v_3 , and v_4 , given that $I = 2A$. The parameters in the diode relation are given to be $I = 10^{-12}A$, $V = 0.025V$.

We will first use the node method to solve this problem. Figure 4.18 shows the ground node and the node voltages. There are four unknown node voltages. Next, we write KCL for each of the nodes. As prescribed by the node method, we will use KV and the diode relation (Equation 4.1) to obtain the currents directly in terms of the node voltage differences and element parameters. For the node with voltage v_1 ,

$$10^{-12}(e^{v_1/0.025} - 1) = 10^{-12}(e^{(v_2-v_1)/0.025} - 1). \quad (4.20)$$

The term on the left-hand side is the current through the lowermost device expressed in terms of node voltages. Similarly, the term on the right-hand side is the current through the device that is second from the bottom.

Similarly, we can write the node equations for the nodes with voltages v_2 , v_3 , and v_4 as follows:

$$10^{-12}(e^{(v_2-v_1)/0.025} - 1) = 10^{-12}(e^{(v_3-v_2)/0.025} - 1) \quad (4.21)$$

$$10^{-12}(e^{(v_3-v_2)/0.025} - 1) = 10^{-12}(e^{(v_4-v_3)/0.025} - 1) \quad (4.22)$$

$$10^{-12}(e^{(v_4-v_3)/0.025} - 1) = I. \quad (4.23)$$

Simplifying, and taking the log on both sides of Equations 4.20 through 4.23, we get

$$v_1 = v_2 - v_1 \quad (4.24)$$

$$v_2 - v_1 = v_3 - v_2 \quad (4.25)$$

$$v_3 - v_2 = v_4 - v_3 \quad (4.26)$$

$$v_4 - v_3 = 0.025 \ln(10^{12}I + 1). \quad (4.27)$$

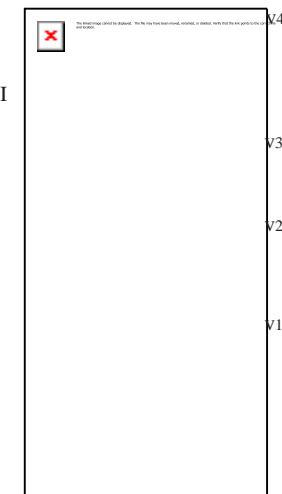


FIGURE 4.18 Seriesconnected diodes.

Given that $I=2A$, we can solve for v_1, v_2, v_3 , and v_4 , to get

$$v_1 = 0.025 \ln(10^{12}I + 1) = 0.025 \ln(10^{12} \times 2 + 1) = 0.71V$$

$$v_2 = 2v_1 = 1.42V$$

$$v_3 = 3v_1 = 2.13V$$

$$v_4 = 4v_1 = 2.84V.$$

Notice that we could have also solved the circuit intuitively by observing that the same 2-A current flows through each of the four identical diodes. Thus, the same voltage must drop across each of the diodes. In other words,

$$I = 10^{-12}(e^{v_1/0.025} - 1)$$

or,

$$v_1 = 0.025 \ln(10^{12}I + 1).$$

For $I=2A$,

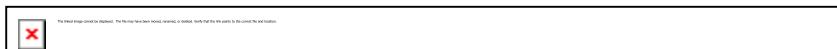
$$v_1 = 0.025 \ln(10^{12} \times 2A + 1) = 0.71V.$$

Once the value of v_1 is known, we can easily compute the rest of the node voltages from

$$v_1 = v_2 - v_1 = v_3 - v_2 = v_4 - v_3.$$



example 4.8 making simplifying assumptions



example 4.9 voltage-controlled nonlinear resistor

4.3 GRAPHICAL ANALYSIS

Unfortunately, the preceding examples are a rather special case. There are many nonlinear circuits that cannot be solved analytically. The simple circuit in Figure 4.16 is one such example. Usually we must resort to trial-and-error solutions on a computer. Such solutions provide answers, but usually give little insight about circuit performance and design. Graphical solutions, on the other hand, provide insight at the expense of accuracy. So let us re-examine the circuit in Figure 4.16 with a graphical solution in mind. For concreteness, we will assume that $E = 3V$ and $R = 500$, and that we are required to determine v_1 and v_2 .

We have already found the two simultaneous equations, Equations 4.18 and 4.19, that describe the circuit. For convenience, let us rewrite these equations here after moving a few terms around:

$$i_D = -\frac{V_D - E}{R} \quad (4.31)$$

$$i_D = I_s(e^{V_D/V_{TH}} - 1). \quad (4.32)$$

To solve these expressions graphically, we plot both on the same coordinates and find the point of intersection. Because we are assuming that we have a graph of the nonlinear function, in this case Figure 4.2, the simplest course of action is to plot the linear expression, Equation 4.31, on this graph, as shown in Figure 4.20. The linear constraint of Equation 4.31 is usually called a “loadline” for historical reasons arising from amplifier design (as we will see in Chapter 7).

Equation 4.31 plots as a straight line of slope $-1/R$ intersecting the V_D axis, ($i_D = 0$) at $v = E$. (The negative sign may be a bit distressing, but does not represent a negative resistance, just the fact that i_D and V_D are not associated variables for the resistors.) For the particular values in this circuit, the graph indicates that i_D must be about 5 mA, and V_D , about 0.6 V. Once we know that i_D is 5 mA, it immediately follows that

$$V_R = i_D R = 5 \times 10^{-3} \times 500 = 2.5 V.$$

It is easy to see from the construction that if E were made three times as large, the voltage across the diode would increase by only a small amount, perhaps to about 0.65 V. This illustrates the kind of insight available from graphical analysis.

The graphical method described here is really more general than it might at first appear. For circuits containing many resistors and sources, but only one nonlinear element, the rest of the circuit, exclusive of the one nonlinear element, is by definition linear. Hence, as described previously in Example 4.4, regardless of circuit complexity we can reduce the circuit to the form in Figure 4.16 by

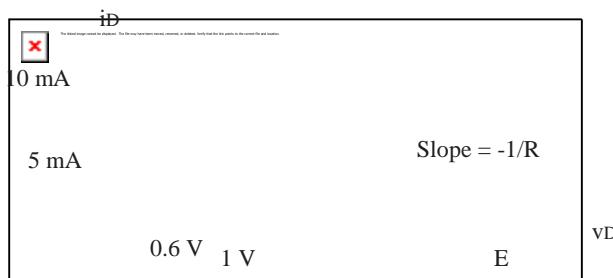


FIGURE 4.20 Graphical solution for diode circuit. The graph assumes that $E = 3$ V and $R = 500$.

the application of Thévenin's Theorem to the linear circuit facing the nonlinear element.

For circuits with two nonlinear elements, the method is less useful, as it involves sketching one nonlinear characteristic on another. Nonetheless, crude sketches can still provide much insight.

example 4.10 half-wave rectifier Let us carry the diode-resistor example of Figure 4.16 and Figure 4.20 a step further, and allow the driving voltage to be a sinusoid rather than DC. That is, let $v_i = E_0 \cos(\omega t)$. Also, for reasons that will become evident, let us calculate the voltage across the resistor rather than the diode voltage. The graphical solution is no different than before, except that now we must solve for the voltage assuming a succession of values of v_i , and visualize how the resultant time waveform should appear.

The circuit now looks like Figure 4.21a. The diode characteristic with a number of different plots of Equation 4.31 (or load lines), corresponding to a representative set of values of v_i , is shown in Figure 4.21b. In Figures 4.21c and 4.21d we show the input sinusoid $v_i(t)$, and the corresponding succession of values of $v_o(t)$ derived from the graphical analysis in Figure 4.21b. Note from Figure 4.21a (or Equation 4.31) that

$$v_o = v_i - v_D \quad (4.33)$$

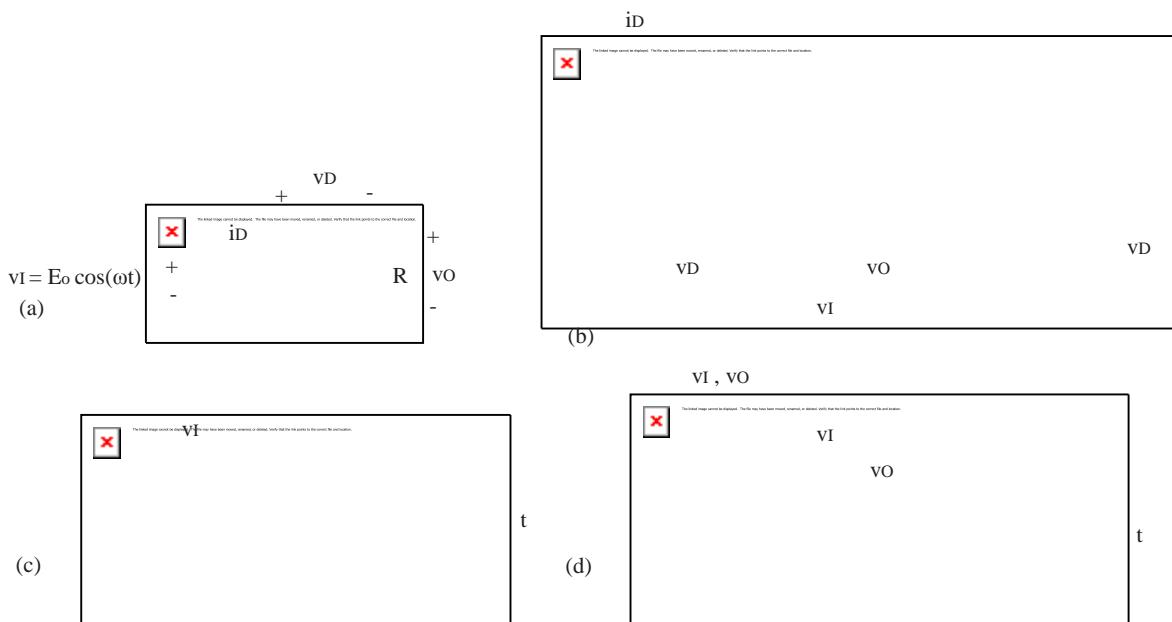


FIGURE 4.21 Half-wave rectifier.

and thus in the graph v_o is the horizontal distance from the load line intersection on the v_D axis to v_I .

A number of interesting conclusions can be drawn from this simple example. First, we really do not have to repeat the load line construction fifty times to visualize the output wave. It is clear from the graph that whenever the input voltage is negative, the diode current is so small that v_O is almost zero. Also, for large positive values of v_I , the diode voltage stays relatively constant at about 0.6 volts (due to the nature of the exponential), so the voltage across the resistor will be approximately $v_I - 0.6\text{V}$. This kind of insight is the principal value of the graphical method.

Second, in contrast to all previous examples, the output waveform in this circuit is a gross distortion of the input waveform. Note in particular that the input voltage waveform has no average value, (no DC value), whereas the output has a significant DC component, roughly 0.3E_o . The DC motors in most toys, for example, will run nicely if connected across the resistor in the circuit of Figure 4.21a, whereas they will not run if driven directly by the sinusoid $v_I(t)$. This circuit is called a half-wave rectifier, because it reproduces only half of the input wave. Rectifiers are present in power supplies of most electronic equipment to generate DC from the 60-Hz “sinusoidal” wave from 110-V AC power line.

4.4 PIECEWISE LINEAR ANALYSIS

In the third of the four major methods of analysis for networks containing nonlinear elements, we represent the nonlinear v_i characteristics of each nonlinear element by a succession of straight-line segments, then make calculations within each straight-line segment using the linear analysis tools already developed. This is called piecewise linear analysis. We will first illustrate piecewise linear analysis by using an example a very simple piecewise linear model for the diode called the ideal diode model.

First, let us develop a simple piecewise linear model for the diode, and then use the piecewise linear method to analyze the circuit in Figure 4.16.

As can be seen from Figure 4.22a, the essential property of a diode is that for an applied positive voltage v_D in excess of 0.6 volts, large amounts of current

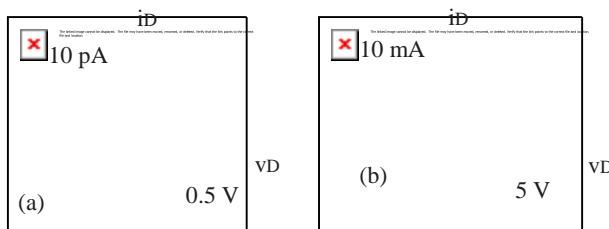


FIGURE 4.22 v_i -characteristics of a silicon diode plotted using different scales.

flow, whereas for negative voltages very small currents flow. Figure 4.22b draws the v-i curve using a larger scale and highlights this dichotomy. The crudest approximation that preserves this dichotomy is the characteristic shown in Figure 4.23a: two linear segments intersecting at the origin, one of zero slope, indicating the behavior of an open circuit, the other infinite, indicating a short circuit. The abstraction is so sufficient that we give it a special symbol, as shown in Figure 4.23b. This is yet another primitive in our vocabulary, called an ideal diode.

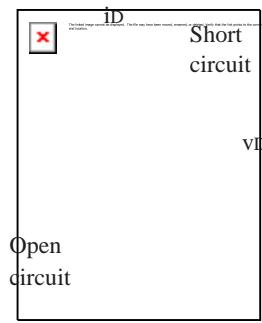
The behavior of this piecewise linear model can be summarized in two statements, one for each of the segments:

$$\text{DiodeON(shortcircuit):} vD=0 \quad \text{for all positive } iD. \quad (4.34)$$

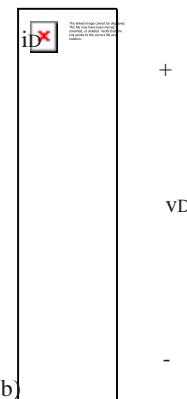
$$\text{DiodeOFF(opencircuit):} iD=0 \quad \text{for all negative } vD. \quad (4.35)$$

We now use the diode model comprising two straight-line segments to illustrate the piecewise linear analysis method applied to the circuit in Figure 4.16 (also shown in Figure 4.24a). In particular, we will determine the voltage v_R across the resistor and the current iD through the resistor for two values of the input voltage, $E = 3V$ and $E = -5V$, and given that $R = 500$.

The piecewise linear analysis technique proceeds by focusing on one straight-line segment at a time, and using our previously developed linear analysis tools to make calculations within each segment. Notice that we are able to apply your linear analysis tools because the nonlinear device characteristics are approximated as linear within each segment. To facilitate our calculations, let us first draw the circuit that results for each of the straight-line segments comprising the ideal diode model.

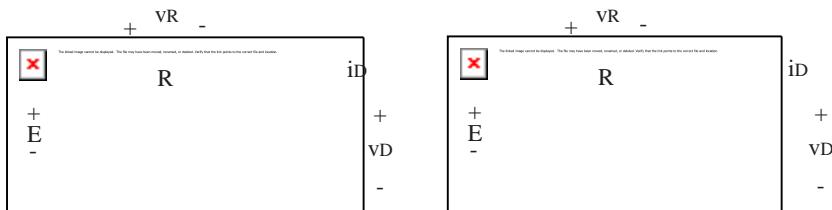


(a)

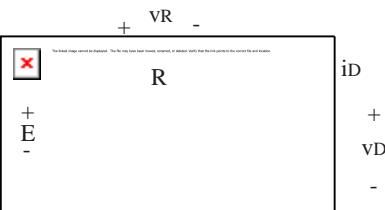


(b)

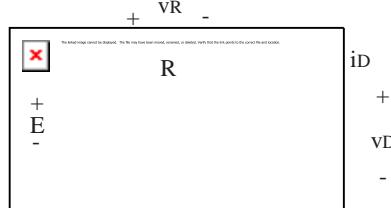
FIGURE 4.23 A piecewise linear approximation for the diode: the ideal diode model.



(a)



(b) Short circuit segment



(c) Open circuit segment

FIGURE 4.24 Piecewise linear analysis of a simple diode circuit.

Short circuit segment: Figure 4.24b shows the resulting circuit when the diode is operating as a short circuit. When i_D and v_D are in this straight-line segment of the characteristic, trivial calculations show that

$$i_D = RE \quad (4.36)$$

and

$$v_R = i_D R = \frac{ER - E}{R} \quad (4.37)$$

Open circuit segment: Figure 4.24c shows the corresponding circuit when the diode is operating as an open circuit. When i_D and v_D are in this part of the characteristic, it is clear that

$$i_D = 0 \quad (4.38)$$

and

$$v_R = 0. \quad (4.39)$$

Combining the results: All that remains now is to determine which of the two segments of operations apply when $E = 3V$ and when $E = -5V$. A little bit of intuition tells us that when $E = 3V$, the short circuit segment applies. Notice that both the resistor and the diode (an nonlinear resistor) do not produce power, and so the direction of the current must be such that the voltage source delivers power. In other words, when E is positive, some i_D . From Equation 4.34, when i_D is positive, the diode is ON. In this segment, from Equations 4.36 and 4.37

$$i_D = \frac{E - 3}{R} = \frac{3}{500} = 6mA \quad (4.40)$$

and

$$v_R = 3V.$$

Compared with the numbers obtained earlier in Section 4.3 using graphical analysis for $E = 3V$, we see that piecewise linear analysis using an approximate model for the diode has yielded reasonably accurate results (6mA versus 5mA for i_D , and 3V versus 2.5V for v_R).

Intuition also tells us that when $E = -5V$, the open circuit segment applies. For the negative input voltage, v is negative. From Equation 4.35, when v_D is negative, the diode is OFF. In this segment, from Equations 4.38 and 4.39, both i_D and v_R are 0.

Notice that the piecewise linear analysis method enabled us to break down an nonlinear analysis problem into multiple linear problems, each of which was very simple. However, an interesting aspect of the method is figuring out the

segment of operation associated with each of the nonlinear devices. This was not too hard with a single nonlinear device such as an ideal diode, but can be challenging when there are a number of nonlinear devices. It turns out that the approach that we discussed in this example generalizes to the method of assumed states, which will be discussed in more detail in Chapter 16.

example 4.11 piecewise linear analysis of a hypothetical nonlinear device Figure 4.25a shows a circuit containing some hypothetical nonlinear device whose v_i -characteristics are approximated using the piecewise-linear graph shown in Figure 4.25b. The nonlinear device with its terminal voltage and current defined as shown in Figure 4.26a might have an actual v_i curve as illustrated in Figure 4.26b. Figure 4.26c shows the correspondence between the device's actual v_i curve and the piecewise linear model.

The behavior of the piecewise linear model for our nonlinear device can be summarized in two statements, one for each of the straight-line segments:

$$\text{Resistance } R_1 \text{ for all positive } i_D \quad (4.41)$$

$$\text{Resistance } R_2 \text{ for all negative } i_D \quad (4.42)$$

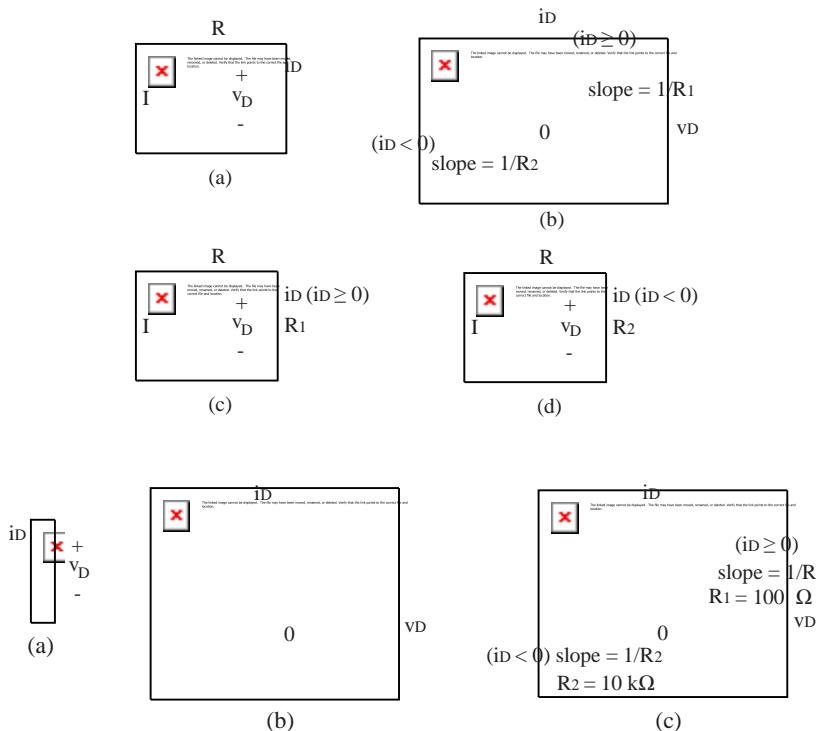


FIGURE 4.25 A circuit containing a nonlinear device whose characteristics are modeled using a piecewise linear approximation. In (b), $R_1=100$ and $R_2=10k$.

FIGURE 4.26 A hypothetical nonlinear device whose characteristics are modeled using a piecewise linear approximation.

Let us apply the piecewise linear analysis method to the circuit in Figure 4.25(a). Specifically, let us determine the voltage v_D across the nonlinear device for various values of the current I sourced by the independent current source. Specifically, we will determine v_D for $I = 1\text{ mA}$, $I = -1\text{ mA}$, and when I is a sinusoidal current of the form $0.002\text{ A} \cos \omega t$.

Following the piecewise linear analysis technique, let us focus on one straight-line segment at a time. Accordingly, we draw the circuit that results for each of the segments.

R_1 segment: Figure 4.25c shows the resulting circuit when the nonlinear device is operating in its R_1 segment. This segment applies when I is positive. Since $i_D = I$, the R_1 segment applies when I is positive. A simple application of Ohm's Law for the R resistor yields

$$v_D = IR_1. \quad (4.43)$$

R_2 segment: Figure 4.25d shows the circuit when the nonlinear device is operating in its R_2 segment. This segment applies when I is negative; in other words, when I is negative. In this segment, we obtain

$$v_D = IR_2. \quad (4.44)$$

Summarizing,

$$\text{When } I \geq 0: v_D = IR_1 \quad (4.45)$$

$$\text{When } I < 0: v_D = IR_2. \quad (4.46)$$

Thus, for $I = 1\text{ mA}$, Equation 4.45 applies. Therefore

$$v_D = IR_1 = 0.001 \times 100 = 0.1\text{ V}.$$

Similarly, for $I = -1\text{ mA}$, Equation 4.46 applies. Therefore

$$v_D = IR_2 = -0.001 \times 10000 = -10\text{ V}.$$

Let us now determine v_D for the cosine current input depicted in Figure 4.27a. When $I \geq 0$,

$$v_D = IR_1 = I \times 100$$

as shown in Figure 4.27b. Similarly, when $I < 0$,

$$v_D = IR_2 = I \times 10000$$

as shown in Figure 4.27c. Piecing together the two results for $I \geq 0$ and $I < 0$, we obtain the complete waveform for the output v_D as shown in Figure 4.27d.

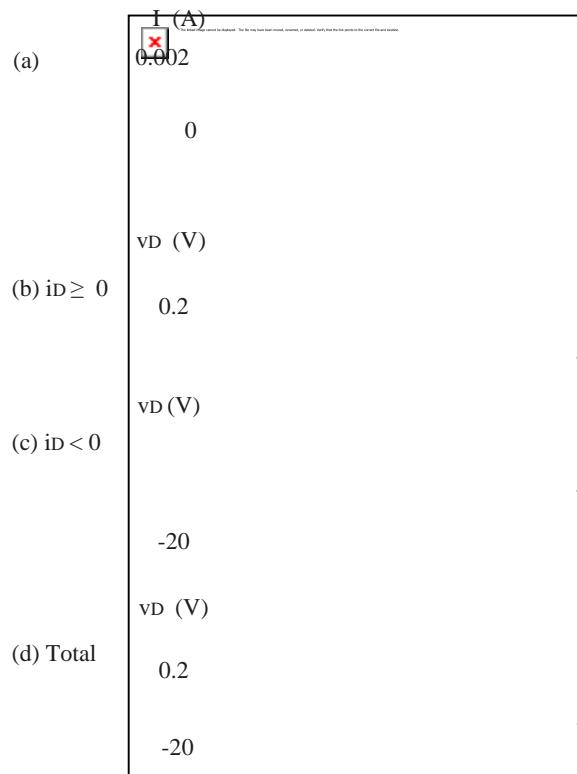


FIGURE 4.27 Cosineinput.

example 4.12 superposition applied in linear segments Although the previous examples illustrated the piecewise linear analysis method, they did not do full justice to the power of the technique, since the equivalent circuits with one each of the linear segments were very simple (for example, the circuits in Figures 4.24b and 4.24c, or the circuits in Figures 4.25c and 4.25d, and did not require any of four powerful analysis techniques such as superposition that rely on linearity. We will now work as a slightly more complicated example to illustrate the full power of the piecewise linear analysis method.

Consider the circuit in Figure 4.28 containing the hypothetical nonlinear device from Example 4.11 (shown in Figure 4.26a) and two independent sources. Suppose we are asked to determine the value of v_B . The presence of the nonlinear device does not allow the application of superposition, since superposition relies on the assumption of linearity.

Let us use the piecewise linear analysis method to solve this problem. The piecewise linear model for the device characteristics is shown in Figure 4.26c. Recall, the nonlinear device

FIGURE 4.28 A circuit containing a nonlinear device and multiple sources.

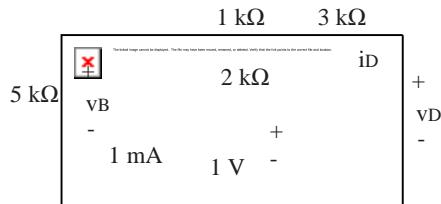
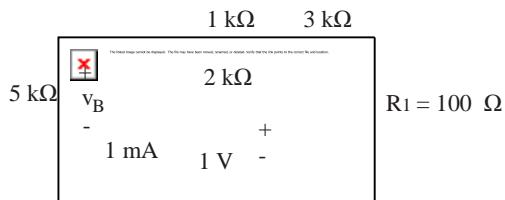


FIGURE 4.29 Equivalent circuit in the linear segment with slope $1/R_1$.



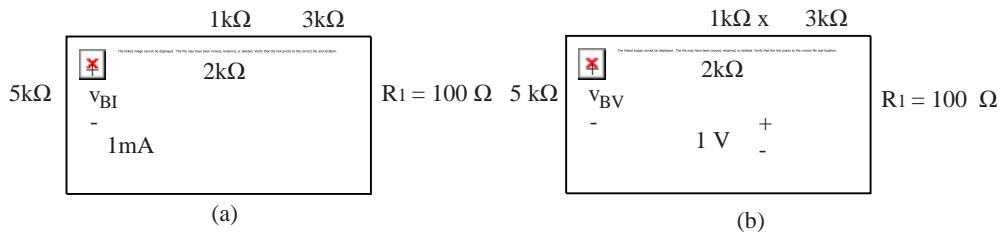
behaves like a resistor of value R_1 when $i_D \geq 0$, and like a resistor of value R_2 when $i_D < 0$.

For the polarities of the current source and the voltage source shown in Figure 4.28, the current i_D through the nonlinear device will be positive. Accordingly, the R_1 segment of device operation applies and the equivalent circuit is as shown in Figure 4.29. In Figure 4.29, we have replaced the nonlinear device with a resistor of value R_1 .

The circuit in Figure 4.29 is linear, so any of our linear techniques can be used. We will use superposition to solve this circuit. According to the first step of the superposition method, for each independent source, we must form a subcircuit with all other independent sources set to zero. Setting a voltage source to zero implies replacing the voltage source with a short circuit, and setting a current source to zero implies replacing the current source with an open circuit. Figure 4.30a shows the subcircuit with the voltage source set to zero, and Figure 4.30b shows the subcircuit with the current sources set to zero.

Now, according to the second step of the superposition method, we must find the response of each independent source acting alone from the corresponding subcircuit. Let us denote the response of the current source acting alone as v_{B1} , and the response of the voltage source acting alone as v_{B2} .

1. In general, we can determine the polarity of i_D by applying a Thévenin reduction on the circuit facing the nonlinear device. i_D will be positive if the Thévenin voltage driving the device is also positive.



vbi: We will analyze the circuit in Figure 4.30 using the intuitive approach of series-parallel reductions discussed in Section 2.4 to obtain vbi. In this approach, we will first collapse all the resistances into an equivalent resistance Req seen by the current source and multiply that resistance by 1 mA. The equivalent resistance seen by the current source is given by

$$Req = (((3k+100)2k)+1k)5k.$$

Simplifying, we get

Req=1.535k.

Multiplying Req by the current source current we get

$$VBI = 1.535k \times 1 \quad mA = 1.535V.$$

vBV: WenowanalyzethecircuitinFigure4.30btoobtainvBV.Wewillagainusethe intuitiveapproachsuggestedinSection2.4involvingfirstcollapsing,then expandingthecircuit.Suppouseweknowthevoltage v_x atnodex,thenwecan easilyobtainvBVbythevoltagedividerrelation.Wecanobtain v_x byfirst collapsingthecircuitinFigure4.30bintotheequivalentcircuitinFigure4.31 andapplyingthevoltagedividerrelation. R_x inthecircuitinFigure4.31is foundbycollapsingthel-1-k,5-k,3-k, andthel100-resistancesintoan equivalentresistanceasfollows:

$$R_x = (1k + 5k)(3k + 100) = 2.05k.$$

By the voltage divider relation

$$v_x = 1V \quad \frac{R_x}{2k+R} x = 1V \quad \frac{2.05k}{2k+2.05k} = 0.51V.$$

We now obtain V_{BV} by expanding the circuit in Figure 4.31 to the original circuit in Figure 4.30 and using the voltage divider relation as follows:

$$VBV=Vx \quad \frac{5k}{1k+5k} = 0.51 V \quad 1k+5k = \frac{5k}{0.425V}$$

FIGURE 4.30 Circuits with each of the sources acting alone.

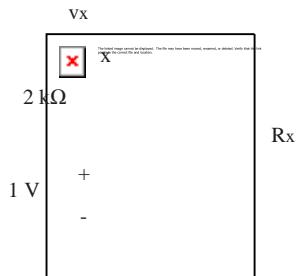


FIGURE 4.31 Collapsed circuit.

As the final step of the superposition method, we obtain the total response by summing together each of the individual responses:

$$v_B = v_{BI} + v_{BV} = 1.535V + 0.425V = 1.96V.$$

Thus, we have our desired answer. Notice that we were able to apply the powerful superposition method by focusing on a straight line segment of the nonlinear device.



example 4.13 half-wave rectifier re-examined

4.4.1 IMPROVED PIECEWISE LINEAR MODELS FOR NONLINEAR ELEMENTS *

example 4.14 another example using piecewise linear modeling



example 4.15 the diode resistance



example 4.16 a more complicated piecewise linear model

4.5 INCREMENTAL ANALYSIS

There are many applications in electronic circuits where nonlinear devices are operated only over a very restricted range of voltage or current, as in many sensor applications and most audio amplifiers, for example. In such cases, it makes sense to find a piecewise linear device model in a way that ensures maximum accuracy of fit over that narrow operating range. This process of linearizing device models over a very narrow operating range is called incremental analysis or small-signal analysis. The benefit of incremental analysis is that the incremental variables satisfy KV and KCL, as well as linear voltage relations over the narrow operating range.

We note, however, that this almost linear mode of operation of nonlinear devices over a narrow operating range is more common with MOSFET circuits (discussed in Chapter 8) than with nonlinear resistors. However, because of the simplicity of nonlinear resistor circuits, we introduce the concept of incremental analysis here, recognizing that the principal application will come later.

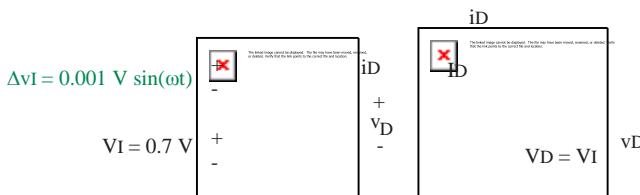


FIGURE 4.37 Incremental analysis.

We will discuss incremental analysis using the diode as an example. Suppose we wish to determine the value of the diode current i_D in the circuit in Figure 4.37. Here we have a diode and a pair of voltage sources as in many previous examples, but in this case one source, V_I , is fixed at a value of, say, 0.7 V, and the other, v_I , is a 1-mV sinusoid. Input of this form — a DC value plus a small time-varying component — occur frequently in practice, and so it is important to find a simple way to solve for the circuit response for this type of input. We could, of course, take the obvious analytical approach and write

$$i_D = I_s e^{(0.7 \text{ V} + 0.001 \text{ V} \sin(\omega t)) / V} \quad (4.53)$$

but it leaves us with a complicated expression from which the form of the output is not readily apparent.

We will abandon the straightforward approach, and instead, cast off in a slightly different direction. Clearly, with the given values of the drive, this is a case where the diode is being operated only over a very restricted region of its nonlinear characteristics: the diode will always have a large positive DC offset voltage across it (given by V_I), and the diode current will vary only by a small amount around I_D (as depicted in the graphical sketch in Figure 4.37) due to the small signal v_I superimposed on the DC input voltage. Thus a sensible approach is to model the diode characteristic accurately in the vicinity of I_D (as depicted by the small straight-line segment tangent to the curve at the V_I, I_D point, as shown in Figure 4.37) and disregard the rest of the curve. The Taylor Series expansion is the appropriate tool to employ for this task:

$$y = f(x) = f(x_0) + \frac{df}{dx} \Big|_{x_0}^0 (x - x_0) + \frac{1}{2!} \frac{d^2f}{dx^2} \Big|_{x_0} (x - x_0)^2 + \dots \quad (4.54)$$

This is an expansion of the y versus x relation about the point $f(x_0), x_0$. For our device i_D versus v_D relation,

$$i_D = f(v_D)$$

we need to develop the corresponding expansion about $f(V_D), V_D$, where $I_D = f(V_D)$.

For our example, the source voltages V_I and v_i are applied directly across the diode, so the corresponding diode voltages are given by $V_D = V_I$ and $v_D = v_i$.

Thus, in terms of diode parameters, the corresponding Taylor Series expansion of $i_D = f(v_D)$ about $f(V_D), V_D$ is:

$$i_D = f(v_D) = f(V_D) + \frac{dv}{dv_D} \Big|_{V_D} (v_D - V_D) + \frac{1}{2!} \frac{d^2f}{dv_D^2} \Big|_{V_D} (v_D - V_D)^2 + \dots \quad (4.55)$$

For our diode example, mathematically we wish to expand the diode equation

$$i_D = I_s e^{(V_D + v_D)/V_{TH}} - 1 \quad (4.56)$$

about the operating point V_D, I_D . In circuit terms we are calculating the response i_D when a voltage $v_D = V_D + v_D$ is applied to diode, as in Figure 4.37. The current i_D will be of the form

$$i_D = I_D + i_d. \quad (4.57)$$

The Taylor series expansion of Equation 4.56 is

$$\begin{aligned} i_D &= I_s e^{V_D/V_{TH}} - 1 + V_{TH} \frac{1}{V_{TH}} I_s e^{V_D/V_{TH}} V_D \\ &\quad + \frac{1}{2} \frac{1}{V_{TH}}^2 I_s e^{V_D/V_{TH}} (V_D)^2 + \dots \end{aligned} \quad (4.58)$$

Simplifying,

$$i_D = I_s e^{V_D/V_{TH}} - 1 + I_s e^{V_D/V_{TH}} \frac{1}{V_{TH}} V_D + \frac{1}{2} \frac{1}{V_{TH}} (V_D)^2 + \dots \quad (4.59)$$

Now if we are assured that the excursions away from the DC operating point V_D, I_D are small, so that v_D is very small compared to V_{TH} (as in this case, since V_{TH} is typically 0.025 V and we are given that $v_D = 0.001$ V) we can ignore the second and higher order terms in the expansion:

$$i_D = I_s e^{V_D/V_{TH}} - 1 + I_s e^{V_D/V_{TH}} \frac{1}{V_{TH}} V_D. \quad (4.60)$$

We know that the output current is composed of a DC component I_D and a small perturbation i_D . Thus, we can write

$$I_D + i_D = I_s e^{V_D/V_{TH} - 1} + I_s e^{\frac{1}{V_{TH}} V_D} \quad . \quad (4.61)$$

Equating corresponding DC terms and corresponding incremental terms:

$$I_D = I_s e^{V_D/V_{TH} - 1} \quad (4.62)$$

$$i_D = I_s e^{V_D/V_{TH}} - \frac{1}{V_{TH}} V_D \quad (4.63)$$

Note that I_D is simply the DC bias current related to the DC input voltage V_D . Accordingly, the DC terms relating I_D to V_D can be equated as in Equation 4.62 because the operating point values I_D, V_D satisfy Equation 4.1, which is the diode equation. When the DC terms are eliminated from both sides of Equation 4.61, the incremental relation shown in Equation 4.63 results.

Thus the response current to an applied voltage $V_D + v_D$ contains two terms: a large DC current I_D and a small current proportional to v_D , if we keep v_D small enough.

A graphical interpretation of this result is often helpful. As shown in Figure 4.37, Equation 4.61 is the straight line passing through the DC operating point V_D, I_D and tangent to the curve at that point. The higher order terms in Equation 4.58 that were neglected would add quadratic, cubic, etc., terms to the model, thereby improving the fit over a wider region.

For the particular case of incremental analysis with the diode equation, we commonly make the following approximation to Equation 4.63:

$$i_D = I_s e^{V_D/V_{TH} - 1} - \frac{1}{V_{TH}} V_D \quad (4.64)$$

where the -1 term is artificially included because it is small in comparison to $e^{V_D/V_{TH}}$. With the inclusion of the -1 term, we can simplify further and write an approximate expression for the incremental diode current:

$$i_D = I_s V_D - \frac{1}{V_{TH}} V_D \quad (4.65)$$

Figure 4.38 provides further insight into the results in Equations 4.62 and 4.63 (or its simplified form in Equation 4.65). Equation 4.62 establishes the V_D, I_D operating point or the bias point of the diode. I_D/V_{TH} is the slope of the i -curve at the point V_D, I_D . The product of the slope of the v -curve at V_D, I_D (given by I_D/V_{TH}) and the small perturbation in applied diode voltage

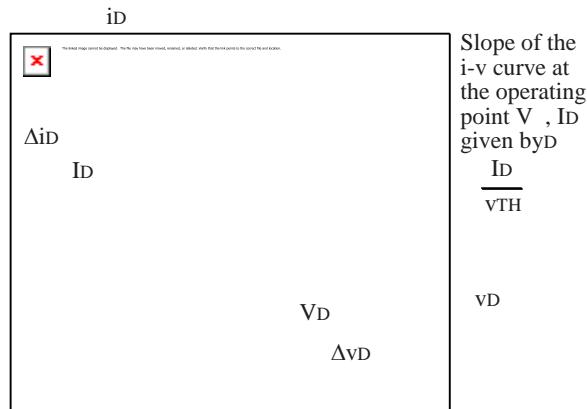


FIGURE 4.38 Graphical interpretation of operating point and incremental signals.

(given by v_D) yields an approximation $i_D = I_D/V_{TH}v_D$ to the resulting perturbation in the diode current.

It is a simple matter to estimate the quality of fit. Taking the ratio of the third term to the second term on Equation 4.58, we obtain

$$\frac{\text{third term}}{\text{second term}} = \frac{1}{2V_{TH}} \frac{1}{v_D}. \quad (4.66)$$

At room temperature, V_{TH} is roughly 25 mV. Thus, if we want the third term to be no more than 10% of the second, v_D must be restricted to be less than 5 mV.

We do not have to go through the mechanics of a Taylor series expansion each time that we wish to find the relationship between the incremental parameters i_D and v_D . Rather, we can find the relationship between the incremental parameters directly from the $i_D = f(v_D)$ relationship using

$$i_D = \frac{v_D}{\frac{d^2f}{dv_D^2} v_D} \quad (4.67)$$

The relationship in Equation 4.67 is itself derived from the Taylor series expansion as follows. Recalling Equation 4.55,

$$i_D = f(v_D) = f(V_D) + \frac{dv}{dv_D} \frac{1}{v_D} (v_D - V_D) + \frac{1}{2!} \frac{d^2f}{dv_D^2} \frac{1}{v_D} (v_D - V_D)^2 + \dots \quad (4.68)$$

and replacing i_D by its DC value plus an increment ($i_D = I_D + \Delta i_D$), the difference ($v_D - V_D$) by Δv_D , and

$$I_D = f(V_D) \quad (4.69)$$

we rewrite Equation 4.68 as

$$I_D + \Delta i_D = I_D + \frac{dv}{dV_D} V_D + \frac{\frac{1}{2} \frac{df}{dV_D} (\Delta v_D)^2}{2!} \quad (4.70)$$

$$\Delta i_D = \frac{dv}{dV_D} V_D \quad (4.71)$$

In words, the incremental change in the current is equal to $f'(V_D)$ evaluated

~~Non-Operating~~ at V_D . This is the slope of the change in the current.

You can verify that applying Equation 4.71 to the diode equation enough that we can ignore second-order terms in Δv_D we get

$$i_D = f(V_D) = I_S (e^{v_D/V_{TH}} - 1)$$

yields the same expression for i_D as that in Equation 4.63.

The same result can be developed graphically from Figure 4.38. The incremental current Δi_D is simply the product of Δv_D and the slope of the i_D versus v_D curve at the point (I_D, V_D) . The slope of the i_D versus v_D curve at the point (I_D, V_D) is given by:

$$\text{Slope of the } i_D \text{ versus } v_D \text{ curve} = \frac{df(v_D)}{dv_D} \Big|_{v_D} \quad .$$

To wrap up our example of Figure 4.37, let us obtain the numerical value of Δi_D for the given form of v_D . We are given that the input is of the form

$$v_I = V_I + v_I = 0.7V + 0.001V \sin(\omega t).$$

Since the input is applied directly across the diode, the corresponding relation in terms of diode voltages is

$$v_D = V_D + v_D = 0.7V + 0.001V \sin(\omega t).$$

When v_D is small enough, Δi_D can be written in the form

$$\Delta i_D = I_D + \Delta i_D.$$

From Equation 4.69,

$$I_D = f(V_D) = I_S e^{0.7/V_D} - 1$$

and, from Equation 4.71,

$$i_D = \frac{d}{dv_D} V_D = I_S e^{0.7/V_{TH}} \cdot \frac{1}{V_{TH}} 0.001 \sin(\omega t)$$

Substituting $I_S = 1 \text{ pA}$ and $V_{TH} = 0.025 \text{ V}$ (at room temperature), the diode parameters, we find that $I_S = 1.45 \text{ A}$ and $i_D = 0.058 \text{ A} \sin(\omega t)$. The values of i_D immediately confirm that it is the sum of a DC term and a small time-varying sinusoidal term. Observe further the ease with which we obtained the form of i_D , and contrast with the uninsightful expression in Equation 4.53 that resulted from the brute-force analytical approach.

Although this process yielded fairly quickly the form of i_D , a bit of insight will simplify the process even further by enabling the use of linear circuit techniques to solve the problem as promised in the introduction of this section. We proceed by drawing attention to Equation 4.61. Equation 4.61 is certainly nonlinear. But an important interpretation central to all incremental arguments allows us to solve the problem by linear circuit methods. Note from Equation 4.62 that the first term in Equation 4.61, the DC current I_D , is independent of v_D . It depends only on the circuit parameters and the DC voltage V_D which is the same as the DC source voltage V_I . Thus I_D can be found with v_D set to zero. On this basis, the second term in Equation 4.61 is linear in v_D , because we have shown that there is no hidden v_D dependence in I_D . Hence the second term, the change in the current, is linearly proportional to the change in v_D , can be found from a linear circuit.

But what is the form of this linear circuit that can facilitate the computation of i_D ? Observe that the constant of proportionality relating i_D and v_D is

$$\frac{i_D}{v_D} = g_d = \frac{1}{V_{TH} I_D} \quad (4.72)$$

or more generally, from Equation 4.71,

$$\frac{i_D}{v_D} = g_d = \frac{df}{dv_D} \Big|_{v_D}, \quad (4.73)$$

which can be interpreted as a linear conductance (the slope of the $v - i$ characteristic at V_D, I_D), or a linear resistance of value

$$r_d = \frac{V_{TH}}{I_D} \quad (4.74)$$

for a diode.

In general, the incremental behavior of a nonlinear device is that of a linear resistor, whose value r_d is given by

$$r_d = \frac{1}{\left. \frac{dv}{df} \right|_{V_D=V_D}}. \quad (4.75)$$

For a diode, because V_{TH} is about 25 mV at room temperature, for $I_D = 1 \text{ mA}$, the incremental resistance $r_d = 25$. Similarly, for $I_D = 1.45 \text{ A}$, $r_d = 0.017$. Note: The incremental resistance in general is not the same as the resistance used in the piecewise linear model of Figure 4.33c. There were trying for a fit over a larger range of current, and hence would compromise on a different resistance value. The difference between R_d and r_d can be clearly understood by comparing the two graphical interpretations, Figures 4.33d and 4.37.

In circuit terms, Equation 4.73 can be interpreted as depicted in Figure 4.39. $i_D = V_D \frac{1}{r_d} = 0.059 \text{ A} \sin(\omega t)$, where $r_d = 1/g_d$. For $I_D = 1.45 \text{ A}$, r_d is 0.017 at room temperature, and

$$i_D = V_D \frac{1}{r_d} = 0.059 \text{ A} \sin(\omega t).$$

In summary, we began our analysis with the goal of determining the current (i_D) through the diode when an input voltage in the form of a DC value (V_D) plus a small time-varying component (Δv_D) is applied across it. Equation 4.61 shows that the resulting diode current is made up of two terms, a DC term, I_D , which depends only on the DC voltage applied V_D , and a small-signal or incremental term Δi_D , which depends on the small-signal voltage and also on the DC voltage V_D . But for fixed V_D , the incremental current Δi_D is linearly related to Δv_D . The constant of proportionality is a conductance g_d given by Equation 4.73. Because the incremental circuit model of Figure 4.39 correctly represents the relationship between i_D and V_D , this linear circuit can be used to solve for i_D . In many situations, only the incremental change in the output

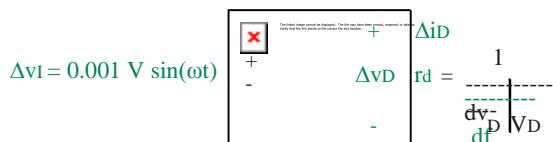


FIGURE 4.39 Linear circuit for determining the value of r_d .

is of interest, and our analysis will end here. If the total value of the output (i_D) is desired, then it can be obtained by summing i_D and the DC component I_D .

Thus, based on the preceding discussion, a systematic procedure for finding incremental voltages and currents for a circuit with a nonlinear device characterized by the $v_i = f(v_D)$ relation is as follows:

1. Find the DC operating variables, I_D and V_D , using the subcircuit derived from the original circuit by setting all small-signal sources to zero. Any of the methods of analyzing nonlinear circuits discussed in the preceding sections — analytical, graphical, or piecewise linear — is appropriate.
2. Find the incremental output voltage and incremental nonlinear device current (the change away from the DC variables calculated in Step 1) by forming an incremental subcircuit in which the nonlinear device is replaced by a resistor of value r (computed as shown in Equation 4.75), and all DC sources are set to zero. (That is, voltage sources are replaced by short circuits, and current sources by open circuits.) The incremental subcircuit is linear, so incremental voltages and currents can be calculated by any of the linear analysis techniques developed in Chapter 3, including superposition, Thévenin, etc.

One final note on notation before we work a few examples to illustrate the small-signal approach. For convenience, we will introduce the following notation to distinguish between total variables, their DC operating or bias values, and their incremental excursions about the operating points. As illustrated in Figure 4.40, we will denote total variables with small letters and capital subscripts, DC operating point variables using all capitals, and incremental values using all small letters. Thus, V_D denotes the total voltage across the device, v_d the DC operating point, and $v_d = v_D - V_D$ the incremental component. Since the total variable is the sum of the two components, we have

$$v_D = V_D + v_d.$$

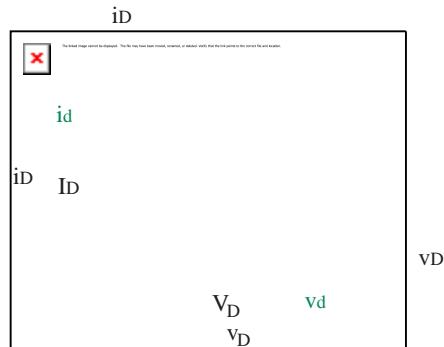


FIGURE 4.40 Notation for operating point, small signal, and total variables.

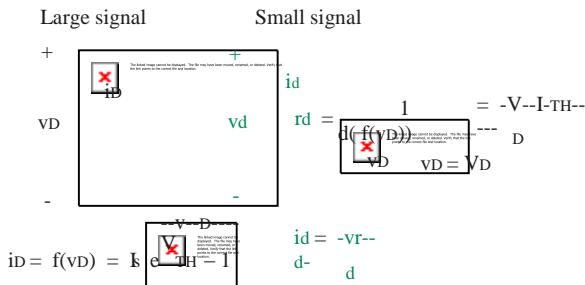


FIGURE 4.41 Large signal and small signal diode models.

Similarly, for the current

$$i_D = I_D + i_d.$$

Figure 4.41 summarizes the large and small signal models for the diode in terms of our new notation.

example 4.17 incremental model for square law device

Derive an incremental model for the square law device shown in Figure 4.42a. Assume that the device is characterized by the following v_i - i relationship:

$$\begin{aligned} i_D &= K V_D^2 && \text{for } V_D > 0 \\ &= 0 && \text{for } V_D \leq 0 \end{aligned}$$

where $K = 1 \text{ mA/V}^2$, and that the operating point values for V_D and I_D are 1 V and 1 mA respectively.

We know from Equation 4.75 that the incremental model for an nonlinear device is linear resistor of value r_d as depicted in Figure 4.42. The value of the resistance is given by

$$r_d = \frac{1}{\frac{dv_D}{di_D} \Big|_{V_D=V_D=1V}}.$$

Substituting, $f(V_D) = Kv^2$, we obtain

$$r_d = \frac{1}{2Kv_D \Big|_{V_D=V_D=1V}} = 500.$$

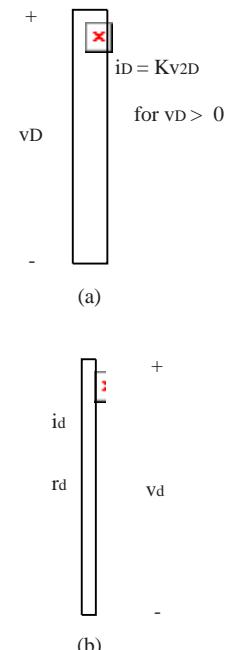


FIGURE 4.42 A square law device and its incremental model. (a) a square law device, (b) incremental model.

example 4.18 incremental model for a resistor

We will show that the incremental model for a linear resistor of value R is also a resistor of value R . Intuitively, since the v_i - i relation for a linear resistor is a straight line, the slope (given by $1/R$) is the same for all values of the resistor voltage and current. Further, since the incremental resistance is the reciprocal of the slope, it follows that $r_d = R$.

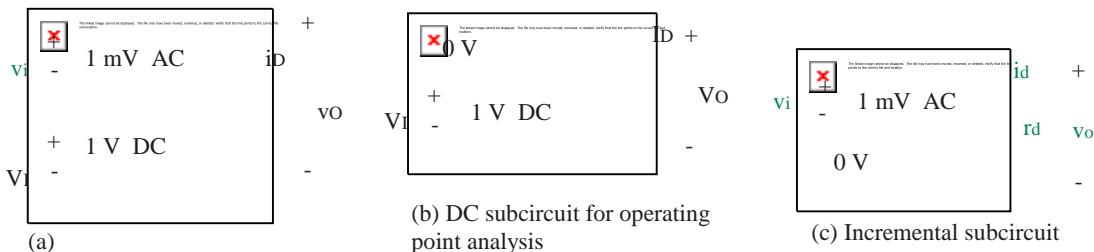


FIGURE 4.43 Incremental analysis of nonlinear resistor. Parts (b) and (c) show the DC and the incremental subcircuits, respectively.

We can also show the same result mathematically as follows. The relation for the resistor is given by

$$i = Rv.$$

We obtain the incremental resistance r for resistor voltage and current (V, I) using Equation 4.75:

$$r = \frac{1}{\frac{dv}{d(v)}} = R.$$

example 4.19 incremental law device Suppose we are interested in finding the current i_D through the square law device in Figure 4.43. The device is driven by a DC voltage in series with a small AC voltage. The square law device is characterized by the following relationship:

$$i_D = K v_o^2 \quad \text{for } v_o > 0. \quad (4.76)$$

The current i_D is 0 for $v_o \leq 0$. Assume $K = 1 \text{ mA/V}^2$.

Since the input to the nonlinear device is the sum of a DC component and a relatively small AC component, incremental analysis is the appropriate tool for our task. Incremental analysis comprises the following steps:

1. Find the DC operating variables I_D and V_o by setting all small-signal sources to zero.
2. Find the incremental device current i_d by forming an incremental subcircuit in which the nonlinear device is replaced by a linear resistor of value r_d (from Equation 4.75), and all DC sources are set to zero.

Following the first step of incremental analysis, we draw the DC subcircuit Figure 4.43b and mark the operating-point variables I_D, V_o . The AC source is set to zero. By inspection from Figure 4.43b

$$V_o = V_i = 1 \text{ V}.$$

and

$$I_D = KV_20 = 1 \text{ mA}.$$

Next, following the second step of incremental analysis we draw the incremental sub-circuit in Figure 4.43b. Here, we set the DC source to zero, and replace the nonlinear device with a linear resistor of value r_d , where

$$r_d = \frac{1}{\frac{dV_o}{d(V_20)}} = \frac{1}{2KV_0}.$$

Substituting $V_o = 1 \text{ V}$, we obtain

$$r_d = 500 \Omega.$$

Now that we know the value of r_d , we can obtain the small-signal component i_d from the small-signal circuit. Accordingly,

$$i_d = r_d \frac{dV_o}{dI}.$$

Substituting numerical values, we find that i_d is a $2\text{-}\mu\text{A}$ AC current. Thus, the total current I_D is the sum of a 1-mA DC current and a $2\text{-}\mu\text{A}$ AC current. This completes our analysis.

example 4.20 voltage regulator based on a nonlinear resistor To illustrate the use of incremental analysis, we examine the nonlinear device circuit shown in Figure 4.44a, a crude form of voltage regulator based on the hypothetical nonlinear resistor discussed earlier. Assume $R = 1\text{k}\Omega$ and that the nonlinear device is characterized by the following $i-v$ relationship:

$$i_D = KV_20 \quad \text{for } V_o > 0. \quad (4.77)$$

The current i_D is 0 for $V_o \leq 0$. Assume $K = 1\text{ mA/V}_2$.

We assume that the supposedly DC source (V_i) supplying the circuit in reality has 5 volts of DC (V_i) with 50 mV of AC (v_i , also called a ripple) superimposed. The regulator is designed to reduce this unwanted AC component relative to the DC. Our task is to determine the magnitude of the ripple in the output, and the extent to which our regulator has been able to reduce the ripple amplitude relative to the DC voltage.

To understand how the circuit operates, we will perform an incremental analysis on the circuit by following these two steps:

1. Find the DC operating variables I_D and V_o by setting all small-signal sources to zero. This will require an nonlinear analysis using one of the nonlinear approaches

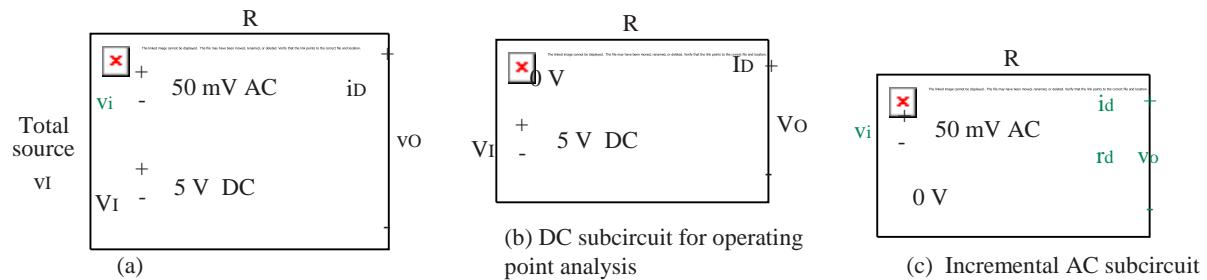


FIGURE 4.44 Nonlinear resistor voltage regulator. Parts (b) and (c) show the DC and the incremental subcircuits, respectively. The subcircuits are derived according to the discussion preceding this example. For more discussion of DC and incremental subcircuits, see Section 8.2.1 in Chapter 8.

previously discussed, for example, analytical (using the node method), graphical or piecewise linear.

- Find the incremental output voltage v_o and incremental nonlinear device current i_d by forming an incremental subcircuit in which the nonlinear device is replaced by a linear resistor of value r_d (from Equation 4.75), and all DC sources are set to zero. The incremental circuit will be linear, so any of our linear analysis techniques will apply, for example, superposition, Thévenin.

Following the first step of incremental analysis, we draw the DC subcircuit Figure 4.44b and mark the operating-point variables i_D , V_O . Notice that we have set the small-signal source to zero.

We will now use the analytical analysis method to determine i_D and V_O . By inspection from Figure 4.44b,

$$-V_I + i_D R + V_O = 0 \quad (4.78)$$

$$i_D = KV^2_0 \quad (4.79)$$

Eliminating i_D , we get

$$RKV^2_0 + V_O - V_I = 0.$$

Solving for V_O , we get:

$$V_O = \frac{-1 + \sqrt{1 + 4V_I K}}{2R} \quad (4.80)$$

Substituting $K = 1 \text{ mA/V}^2$, $R = 1 \text{ k}$, and $V_I = 5 \text{ V}$, we obtain the operating point values:

$$V_O = 1.8 \text{ V}$$

$$i_D = 3.24 \text{ mA.}$$

V_O is the DC component of the output. This completes the first step of incremental analysis.

Next, following the second step of incremental analysis we draw the incremental sub-circuit in Figure 4.44c. This time around, we set the DC source to zero, and replace the nonlinear resistor with a linear resistor of value r_d .

We can now find the incremental values i_d , v_o from Figure 4.44c if we know the value of r_d . Accordingly, we first determine the value of r_d . We know from Equation 4.71 that

$$i_d = \frac{d(Kv_o)}{dv_o} \Big|_{v_o=V_o}$$

so

$$r_d = \frac{1}{\frac{dv_o}{d(Kv_o)} \Big|_{v_o=V_o}}.$$

Simplifying,

$$r_d = \frac{1}{2Kv_o}.$$

Substituting the numerical values, $r_d = 1/(2 \times 1 \times 10^{-3} \times 1.8) = 278$.

Now that we know the value of r_d , we can obtain the small-signal component of the output v_o from the small-signal AC circuit in Figure 4.44c. Notice that the circuit in Figure 4.44c is a voltage divider. Thus, the small-signal AC output

$$v_o = v_i \frac{r_d}{R + r_d} \quad (4.81)$$

$$= 50 \times 10^{-3} \frac{278}{1000 + 278} = 10.9 \text{ mV}.$$

and

$$i_d = \frac{v_o}{r_d} = \frac{0.0109}{278} = 0.039 \text{ mA.}$$

This completes our analysis. 2

Although both the DC and the AC components of the output voltage are smaller than the corresponding input components, the important parameter is the fractional ripple, the ratio of the ripple to the DC. At the input,

$$\text{fractional ripple} = \frac{50 \times 10^{-3}}{5} = 10^{-2} \quad (4.82)$$

2. As an interesting aside, we can alternatively obtain v_o mathematically by starting from the equation relating v_o to v_i :

$$v_o = \frac{-1 + \sqrt{1 + 4v_i R K}}{2 R K}$$

and at the output,

$$\text{fractional ripple} = \frac{10.9 \times 10^{-3}}{1.8} = 0.6 \times 10^{-2}, \quad (4.83)$$

so the ripple has been reduced relative to the DC by a factor of about 1.7. This level of reduction is not particularly exciting. As can be seen from Equation 4.81, we can improve the level of reduction by reducing the value of r_d . One way to do so is to replace the nonlinear resistor of this example with one whose v_i curve has a steeper slope as seen in the next example.

It is important to understand that the mathematical basis for incremental analysis and for the formation of the two subcircuits, as in Figure 4.44, is not superposition, but a particular interpretation of a Taylor series expansion. Even though we keep only the first two terms of the series, as in Equation 4.61, the relationship is still nonlinear, and hence superposition cannot apply.



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example 4.21 diode regulator



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example 4.22 small signal analysis using a piecewise linear diode model

Observing that the incremental change in v_o is given by the product of the incremental change in v_i and the slope of the v_o versus v_i curve evaluated at V_I , we can write

$$v_o = \frac{d}{dv_i} \left(\frac{-1 + \sqrt{1 + 4V_I R_K}}{2R_K} v_i \right) \Big|_{V_I} \quad (4.84)$$

Simplifying,

$$v_o = \frac{1}{1 + 4V_I R_K} v_i$$

$$= 10.9 \text{ mV}$$

which is the same as the value obtained by analyzing the small-signal circuit.

4.6 SUMMARY

This chapter introduced nonlinear circuits and their analyses. Nonlinear circuits include one or more nonlinear devices, which display a nonlinear v_i -relationship. Nonlinear circuits obey KVL and KCL and can be solved using the basic KVL/KCL method or the node method. Note that the KVL/KCL method or the node method do not make any assumptions about linearity.

We discussed four methods for solving nonlinear circuits including the analytical method, the graphical method, the piecewise linear method, and the small signal method (also known as the incremental method).

The analytical method uses KVL/KCL or the node method to write the circuit equations and solve them directly. The graphical method uses a graph of the v_i -relation of the nonlinear device and the graph capturing the circuit constraints to solve for the operating point. The piecewise linear method represents the v_i characteristics of an nonlinear element by a succession of straight-line segments, then makes calculations within each straight-line segment using linear analysis tools.

The small signal method applies to circuits in which nonlinear devices are operated only over a very small range of voltage or current values. For small perturbations of voltages or currents about an nominal operating point, nonlinear device behavior can be approximated using a piecewise linear model that provides a good fit in the narrow operating range. Thus, incremental variables not only satisfy KVL and KCL, but also linear v_i -relations over the narrow operating range.

We introduced the following notation to distinguish between total variables, DC operating values, and small signal variables:

We denote total variables with small letters and capital subscripts, e.g., v_D ,
DC operating point variables using all capitals, e.g., V_D ,
and incremental values using all small letters, e.g., v_d .

A systematic procedure for finding incremental voltages and currents for a circuit with a nonlinear device characterized by the v_i -relation:

$$i_D = f(v_D)$$

is the following:

1. Find the DC operating variables I_D and V_D using the subcircuit derived from the original circuit by setting all small-signal sources to zero. Any of the methods discussed in the preceding sections — analytical, graphical, or piecewise linear — is appropriate.

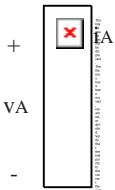
2. Find the incremental output voltage and incremental nonlinear device current by forming an incremental subcircuit in which the nonlinear device is replaced by a resistor of value r_d , where

$$r_d = \frac{1}{\left. \frac{dv}{df(V_D)} \right|_{V_D=V_D}},$$

other linear resistances are retained as is, and all DC sources are set to zero. The incremental subcircuit is linear, so incremental voltages and currents can be calculated by any of the linear analysis techniques.

EXERCISES

exercise 4.1 Consider a two-terminal nonlinear device (see Figure 4.47) whose $v-i$ characteristic is given by:



$$i_A = f(v_A) \quad (4.92)$$

Show that the incremental change in the current ($i_A - i_a$) for an incremental change in the voltage ($v - V_A$) at the DC operating point V_A, I_A is given by:

$$i_a = \frac{\overline{v_A}}{df(\overline{v_A})} \quad v_A = V_A$$

FIGURE 4.47

(Hint: Substitute $i_A = I_A + i_a$ and $v_A = V_A + v$ in Equation 4.92, expand using Taylor series, ignore second-order and higher terms in v , and equate corresponding DC and small-signal terms.)

exercise 4.2 Suppose the two-terminal nonlinear device from the previous exercise (see Figure 4.47) has the following $v-i$ characteristic:

$$i_A = f(v_A) = c_1 V_A^2 + c_2 V_A + c_3 \quad \text{for } V_A \geq 0, \text{ and } f(v_A) = 0 \text{ otherwise.}$$

- Find the operating point current I_A for an operating point voltage V_A , where $V_A > 0$.
- Find the incremental change in the current i_a for an incremental change in the voltage v_A at the operating point V_A, I_A .
- By what fraction does i_a change for a percent change in v_A ?
- Suppose the nonlinear device is biased at V instead of V_A , where V is percent greater than V_A . Find the incremental change in the current (i) for an incremental change in the voltage (v_A) at this new bias point. By what fraction is i different from the i_a calculated in part (b)?

e) Find the incremental change in the current $i_{A\text{cx}}$ for an incremental change in the parameter c_x (given by $c_x = cx$) from its nominal value of C_x , assuming the operating point values are V_A, I_A, A

Hint: Observe that if i_A depends on the parameters x_A and y_B , in other words,

$$i_A = f(x_A, y_B),$$

then the incremental change in i_A for an incremental change in y_B is given by

$$\frac{\delta i_A}{\delta y_B} = \frac{\partial f(x_A, y_B)}{\partial y_B} \Big|_{y_B=Y_B}$$

exercise 4.3 The nonlinear device (NLD) in the circuit in Figure 4.48 has the $v-i$ characteristics shown. Find the operating point i_D and v_D for $R=910$.

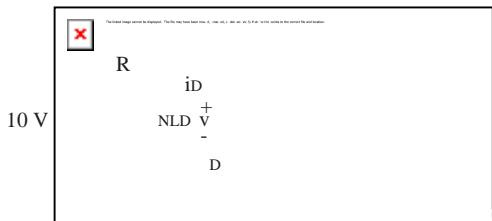


FIGURE 4.48

exercise 4.4

a) Plot the i_A vs. v_A characteristics for the nonlinear network shown in Figure 4.49. Assume the diode is ideal.

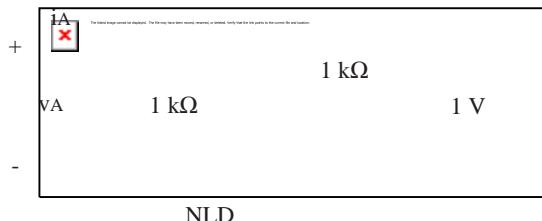
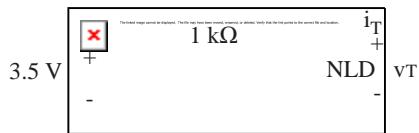


FIGURE 4.49

b) The nonlinear network from part (a) is disconnected as shown in Figure 4.50. Draw the load line on your $i-v$ characteristics from part (a), and find i_T .

FIGURE 4.50



(a)



(b)

FIGURE 4.51

exercise 4.5 Consider two identical semiconductor diodes, each of which has any ~~is~~ relation:

$$i_D = I_S e^{v_D/V_{TH}} - 1 \quad (4.93)$$

a) Find the relation of i to v for the pair connected in parallel as shown in Figure 4.51a.

b) Find the relation of i to v for the pair connected in series as shown in Figure 4.51b.

exercise 4.6 For the circuit in Figure 4.52, find the input characteristic, i versus v , and the transfer characteristic i_2 versus v . I is fixed and positive. Express your results in graphs, labeling all slopes, intercepts, and coordinates of any breakpoints.

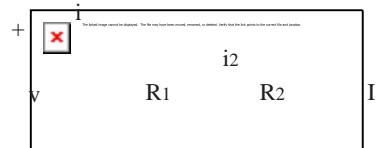


FIGURE 4.52

exercise 4.7 For the circuit in Figure 4.53 and the values shown below, sketch the waveform of $i(t)$. On your sketch, show when the ideal diode is on and when it is off.

$$v_i = 10 \sin(t) \quad V_0 = 5V \quad R = 1\Omega$$

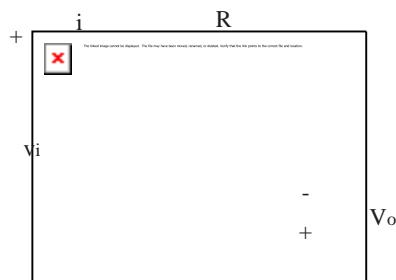
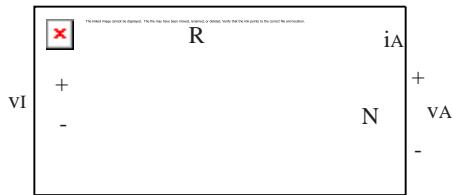


FIGURE 4.53

problem 4.1 Consider the circuit containing a nonlinear element N as shown in Figure 4.54. The relation for N is given by:

$$i_A = c \sqrt{v_A^2 + c_0} \text{ for } v_A \geq 0, \text{ and } i_A = 0 \text{ otherwise.}$$



- a) Solve for i_A and v_A using the analytical method.
- b) Find the operating point values of the nonlinear element's voltage and current for $v_i = V_i$, where V_i is positive.
- c) Find the incremental change in i_A (given by i_A) for an incremental change in v_i (given by v_i).
- d) Determine the incremental change in the voltage across the resistor R for an incremental change in the input v_i (given by v_i).
- e) Find the incremental change in i_A for a 2% increase in the value of R .
- f) Find the incremental change in i_A for an incremental change in v_A at the bias point V_A, i_A .
- g) Suppose we replace the source v_i with a DC voltage V_i in series with a small time-varying voltage $v_i = v_o \cos(\omega t)$. Determine the time-varying component of i_A .
- h) Suppose we now replace $v_i = V_i + v_i$, where $V_i = 10\text{V}$ and $v_i = 1\text{V}$.
 - i) Find the bias point DC current i_A corresponding to $V_i = 10\text{V}$.
 - ii) Find the value of i_A corresponding to $v_i = 1\text{V}$ using small-signal analysis.
 - iii) Find the value of i_A using small-signal analysis. (Use $i_A = I_B + i_s$.)
 - iv) Find the value of i_A using the analytical method for $v_i = V_i + v_i = 11\text{V}$.
 - v) Now, find the exact value of i_A using $i_A = i_s - I_B$.
 - vi) What is the error in the value of i_A computed using the small-signal method?

problem 4.2 The circuit shown in Figure 4.55 contains two nonlinear devices and a current source. The characteristics of the two devices are given. Determine the voltage v for (a) $i_S = 1\text{A}$, (b) $i_S = 10\text{A}$, (c) $i_S = 1 + \cos(t)$.

problem 4.3 A plot (hypothetical) of the v - i characteristics (terminal voltage as a function of the current drawn out, and not its associated variables) for a battery is shown in Figure 4.56(a).

PROBLEMS

FIGURE 4.54

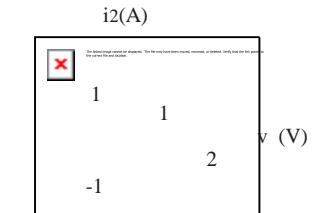
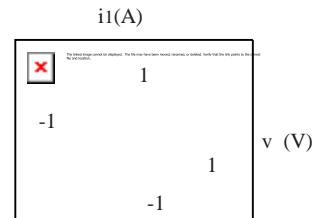
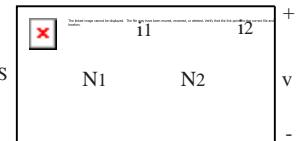


FIGURE 4.55

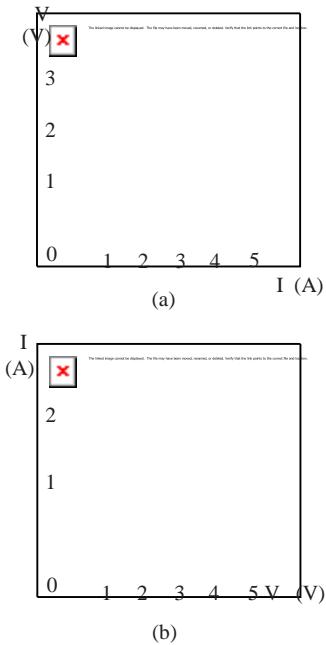


FIGURE 4.56

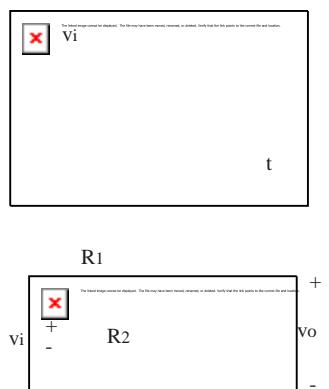


FIGURE 4.57

- a) If a 2-resistor is connected across the battery terminals, find the terminal voltage of the battery and the current through the resistor.
- b) A light bulb is a nonlinear resistance because of self-heating effects. A hypothetical v-i plot is shown in Figure 4.56(b). Find the bulb current and bulb voltage if the lamp is connected to the battery.
- c) Devise a piecewise-linear model for the battery which is reasonably accurate over the current range 0–2 A.
- d) Use this piecewise-linear battery model to find the battery voltage and bulb current if the bulb and 2-resistor are reconnected in series to the battery.

problem 4.4

- a) Assuming the diode can be modeled as an ideal diode, and $R_1 = R_2$, plot the waveform $v_o(t)$ for the circuit in Figure 4.57, assuming a triangle wave input. Write an expression for $v_o(t)$ in terms of v_i , R_1 , and R_2 .
- b) If the triangle wave has a peak amplitude of only 2 volts, and $R_1 = R_2$, a more accurate diode model must be used. Plot and write an expression for v_o assuming that the diode is modeled using an ideal diode in series with a 0.6-volt source. Draw the transfer curve v_o versus v_i .

problem 4.5 Figure 4.58 is an illustration of a crude Zener-diode regulator circuit.

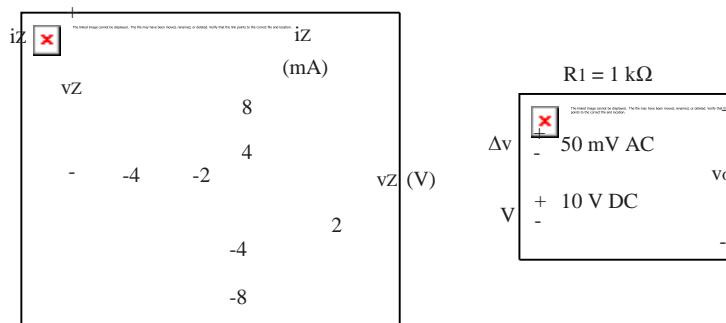


FIGURE 4.58

- a) Using incremental analysis, estimate from the graph an analytic expression for v_o in terms of V and v .
- b) Calculate the amount of DC and the amount of AC in the output voltage using the Zener-diode characteristic to find model values. (Numbers, please.)

c) What is the Thévenin output resistance of the power supply, that is, the Thévenin resistance seen looking in at the v terminals?

problem 4.6 The terminal voltage-current characteristic of a single solar cell is shown in Figure 4.59a. Note that this is a sketch of the terminal voltage as a function of current drawn out (i.e., not the associated variable convention). An array is made by connecting a total of 100 such cells as follows: Ten solar cells are connected in series. Ten sets of these are made. These ten series strips are then connected in parallel (see Figure 4.59b).

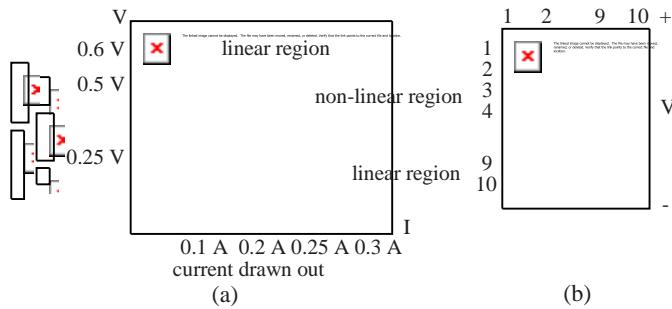
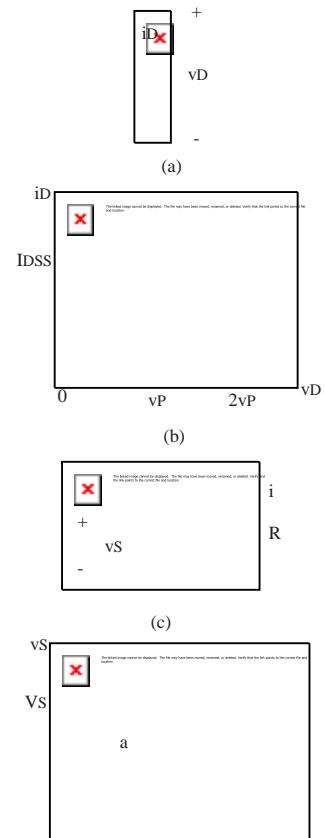
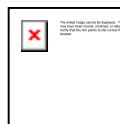
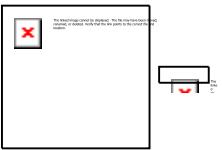


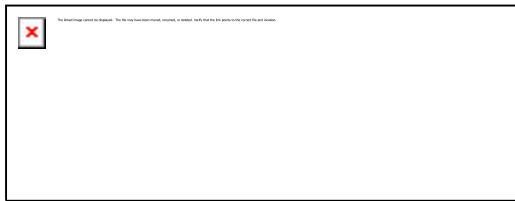
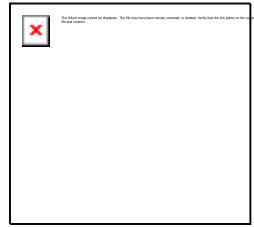
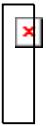
FIGURE 4.59

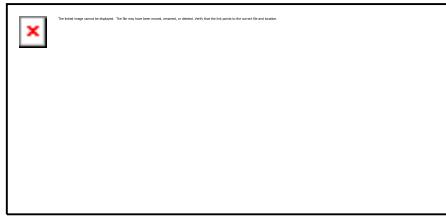
If a 3-resistor is connected across this new two-terminal element (the 100-cell array), determine the terminal voltage across and the current through the resistor.

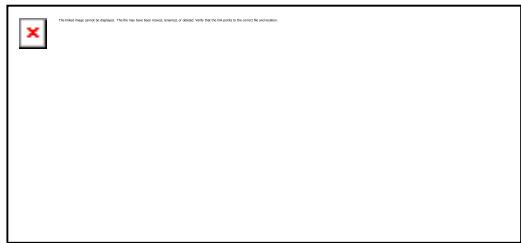
problem 4.7 The junction field-effect transistor (JFET) with the specific connection shown in Figure 4.60a (gate and source shorted together) behaves as a two-terminal device. The v_D i_D characteristics of the resulting two-terminal device shown in Figure 4.60b saturates at current ID_{SS} for v_D greater than a voltage V_P , called the pinch-off voltage. In the two-terminal configuration shown, the JFET characteristic is

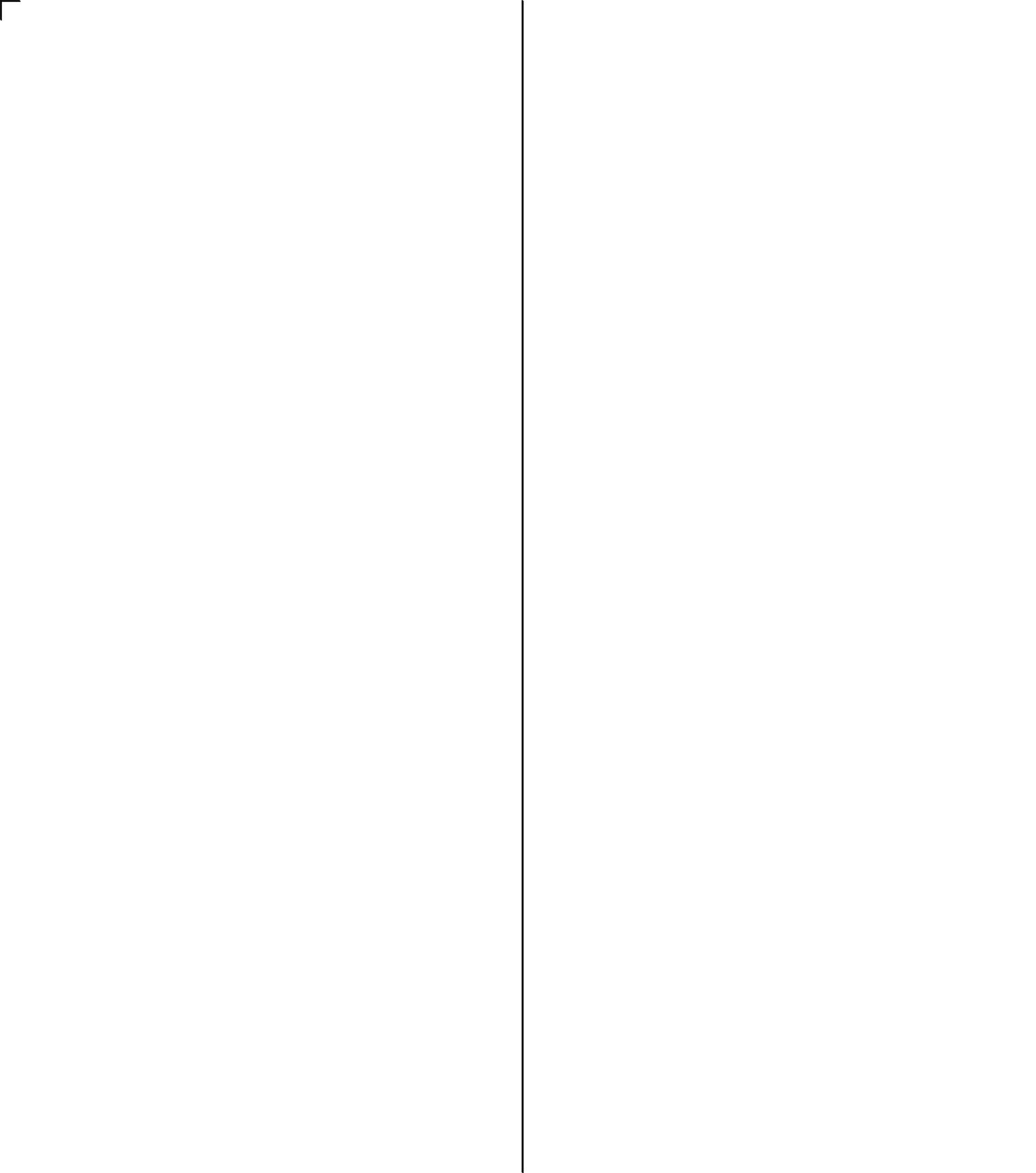


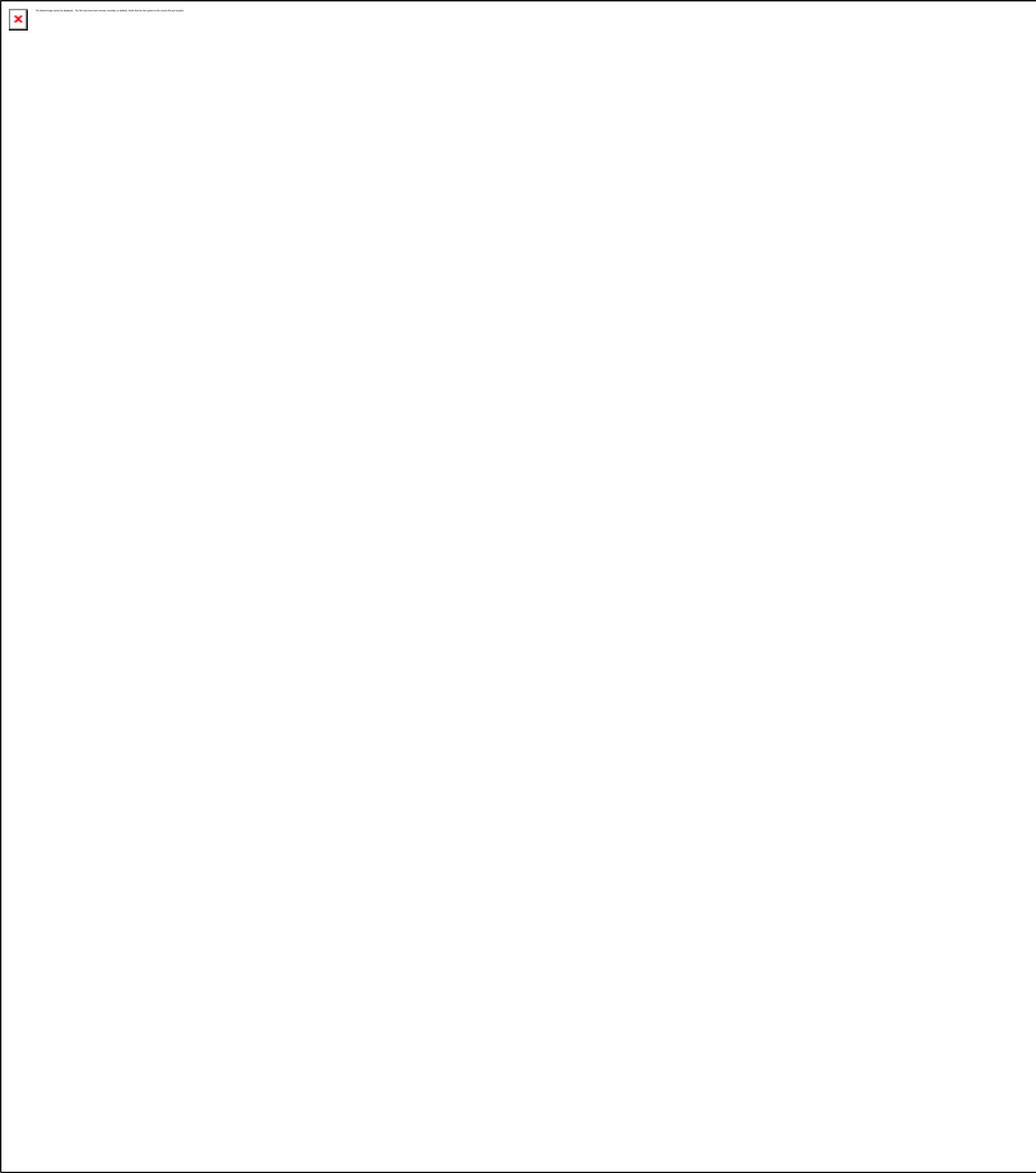




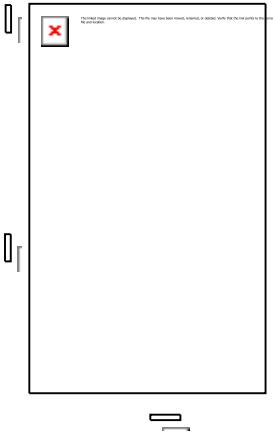


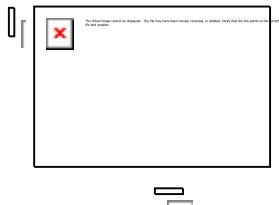
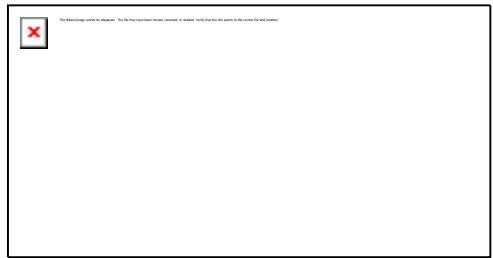




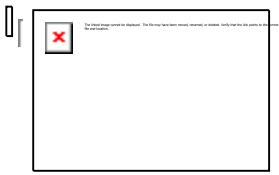






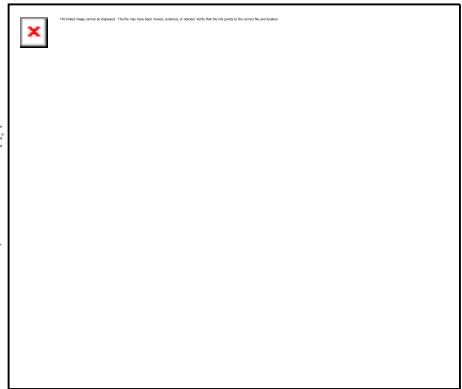


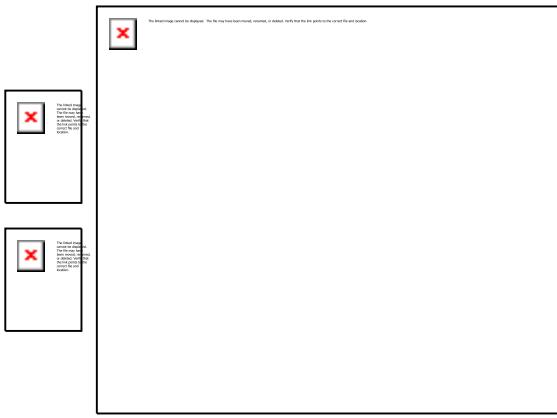
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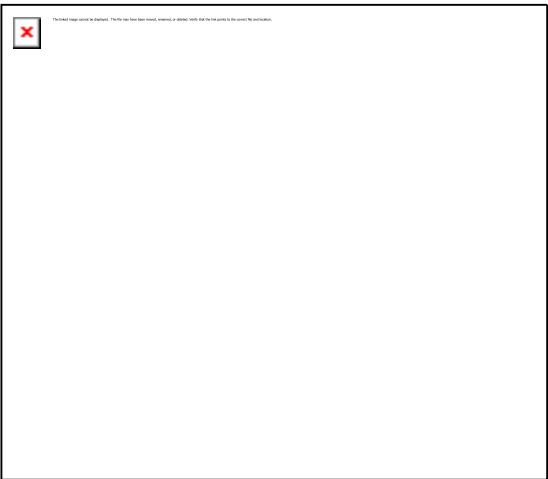


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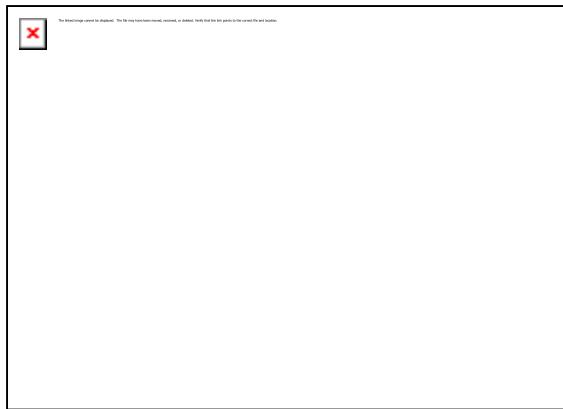
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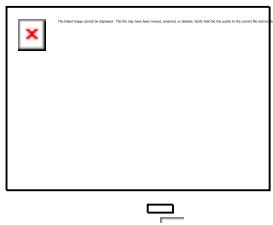
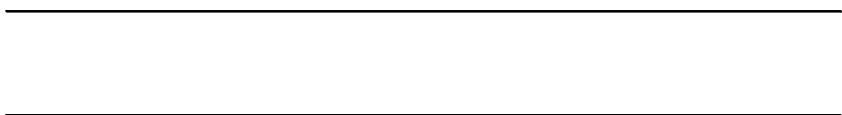
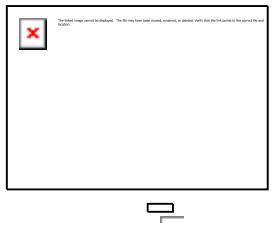


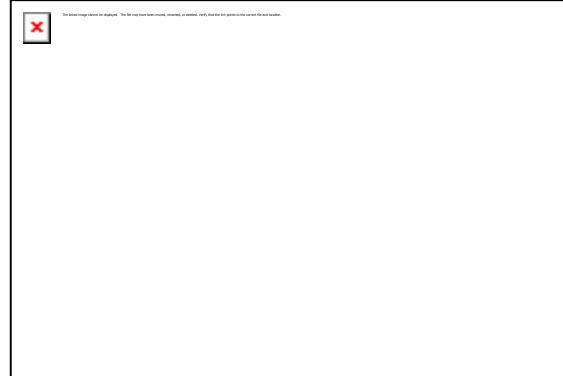


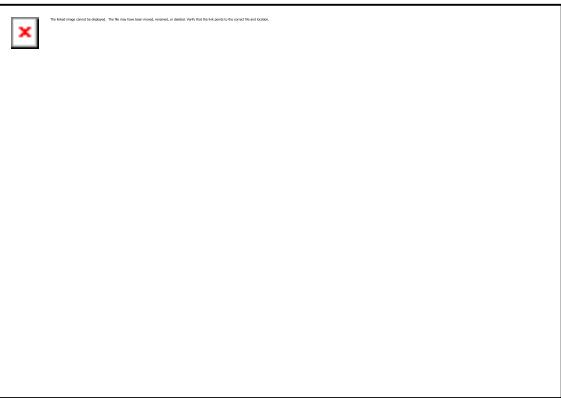


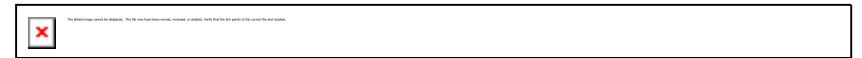










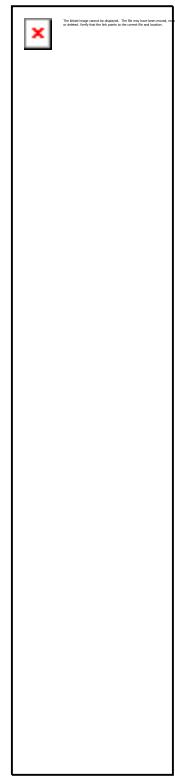


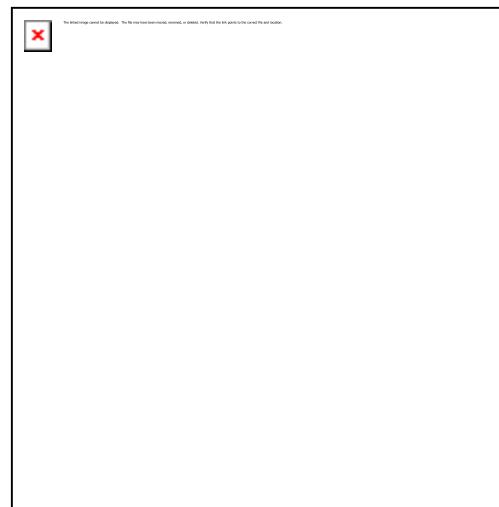
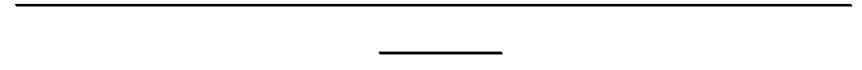


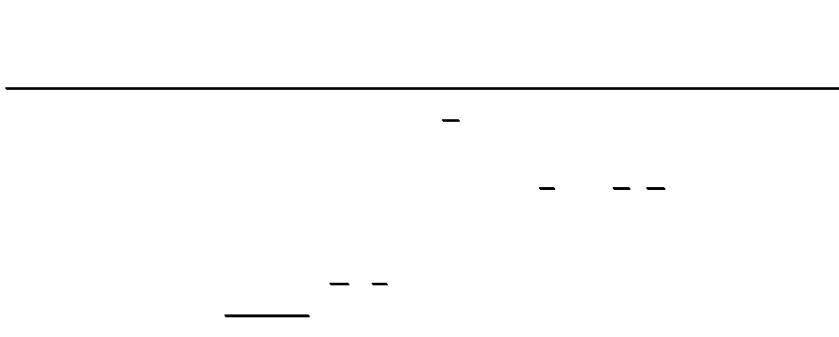
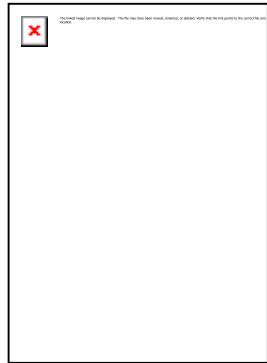
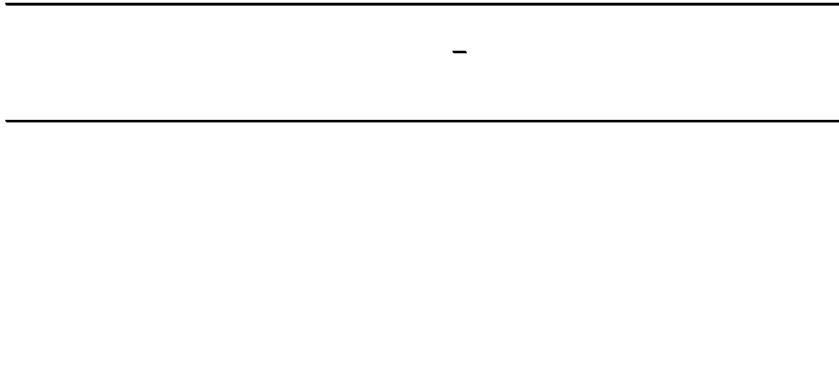
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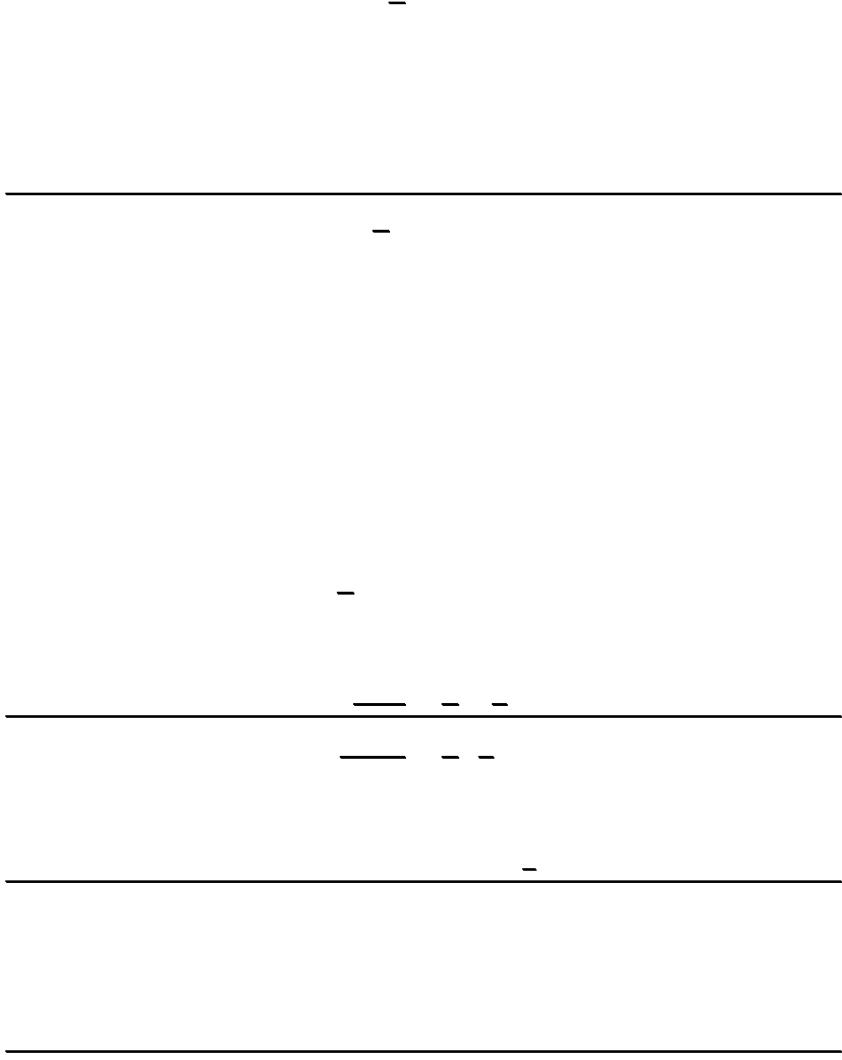
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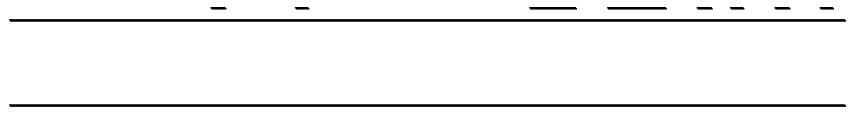
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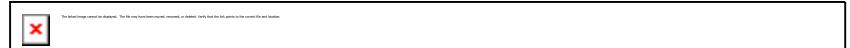
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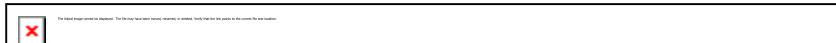
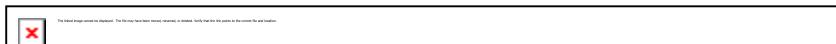
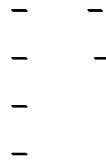
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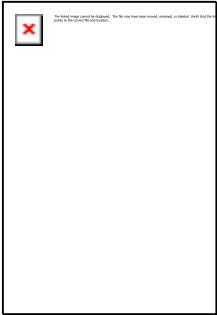
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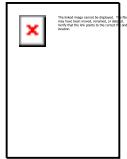


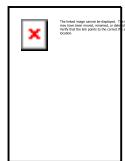
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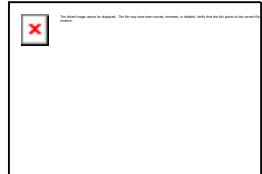
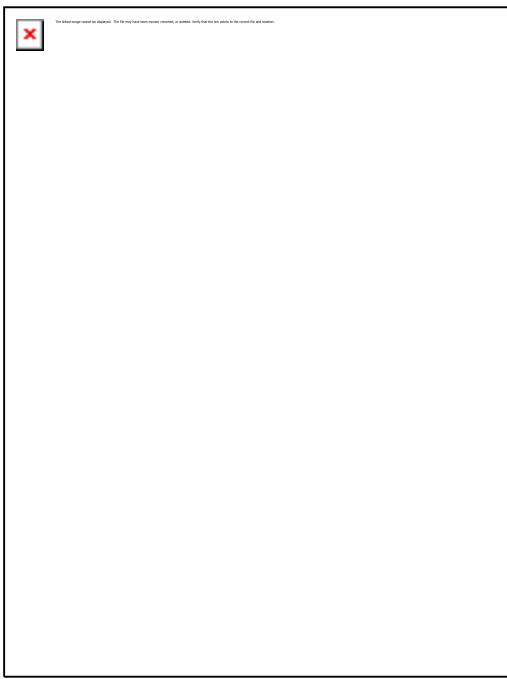


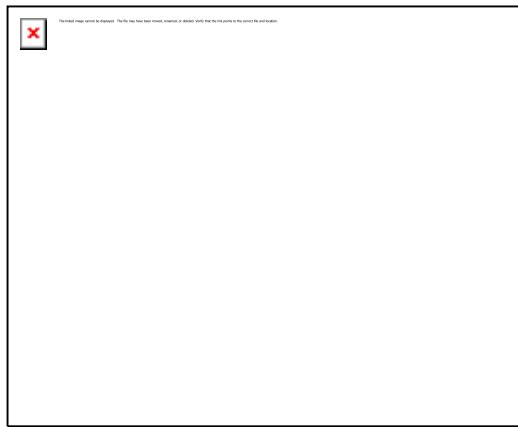
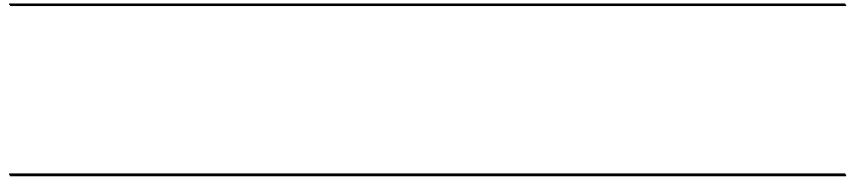


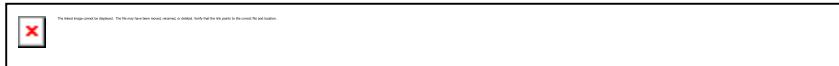
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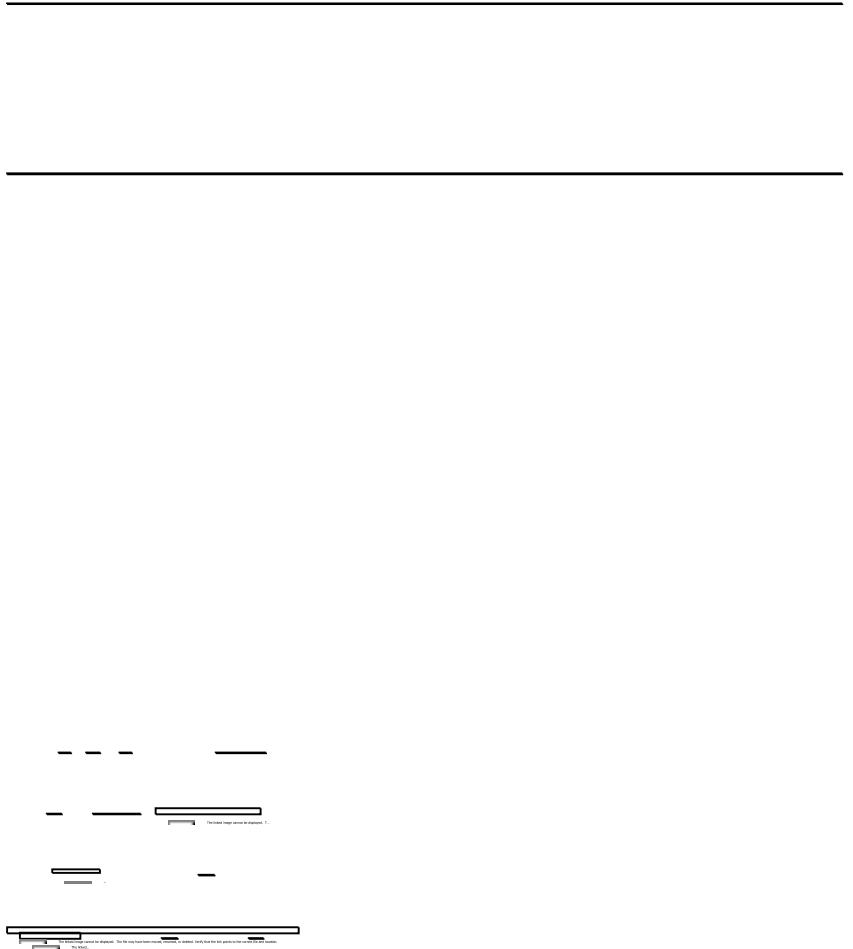




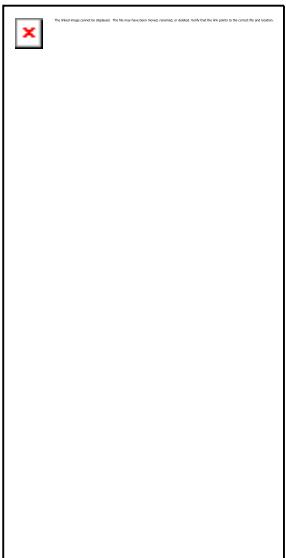


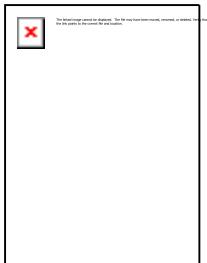
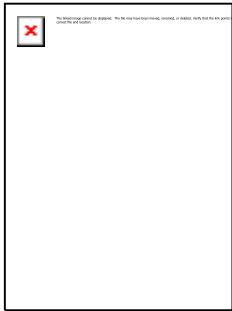


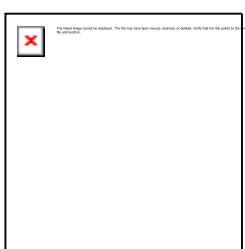
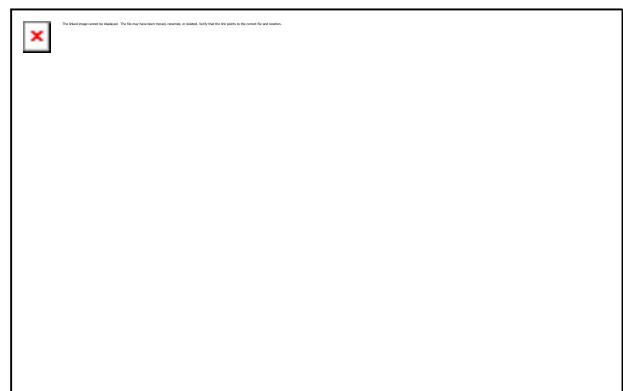
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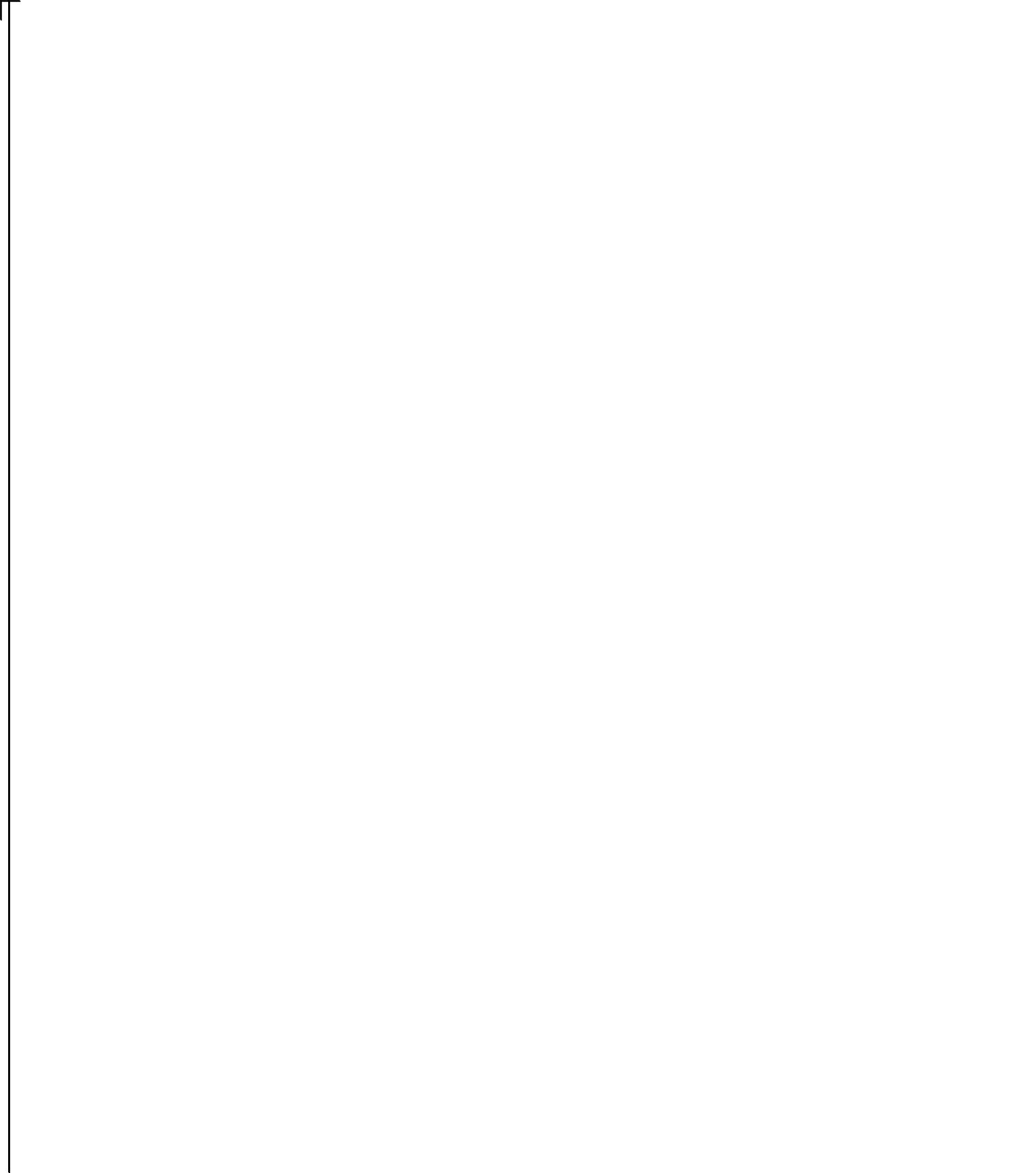


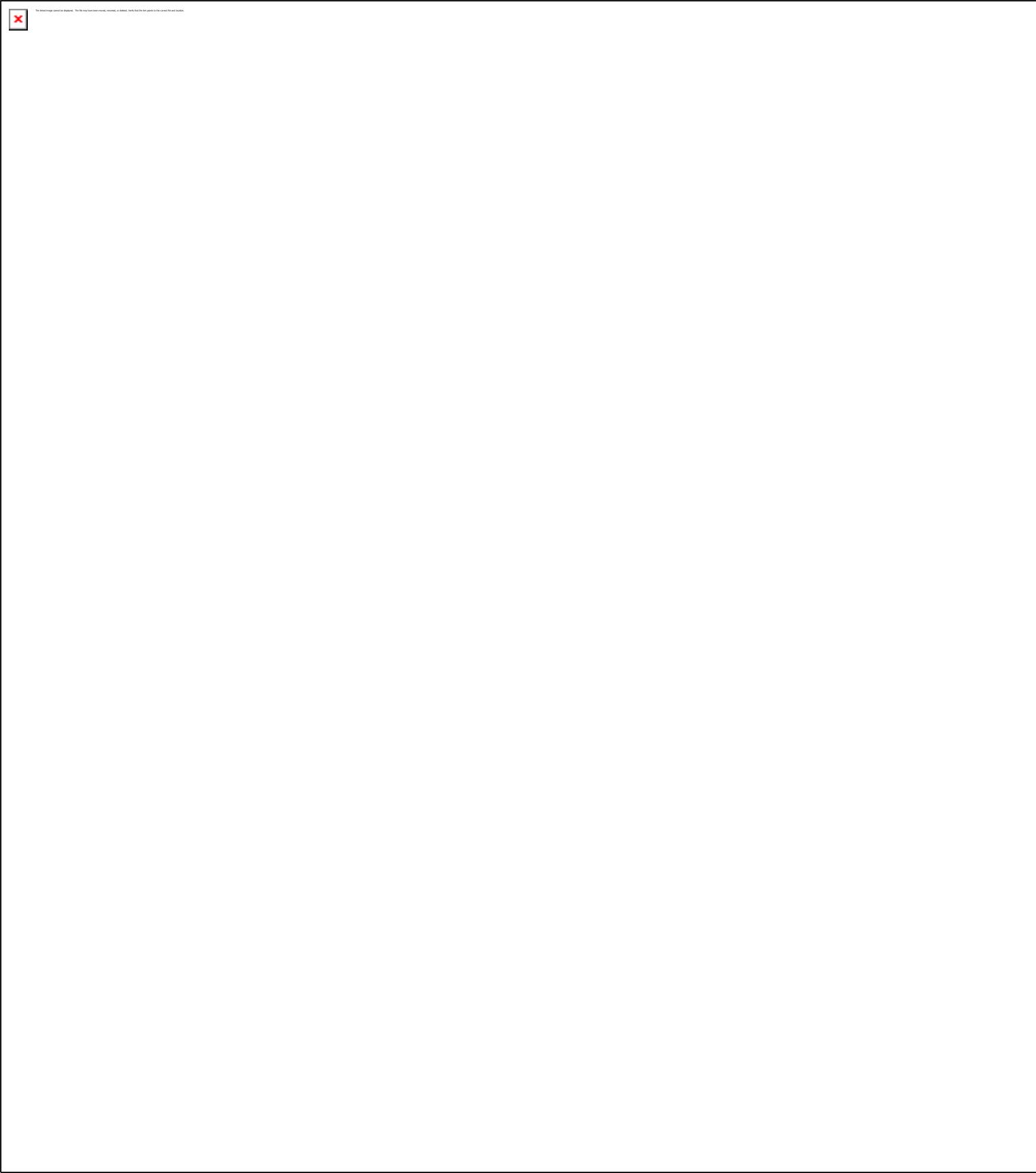


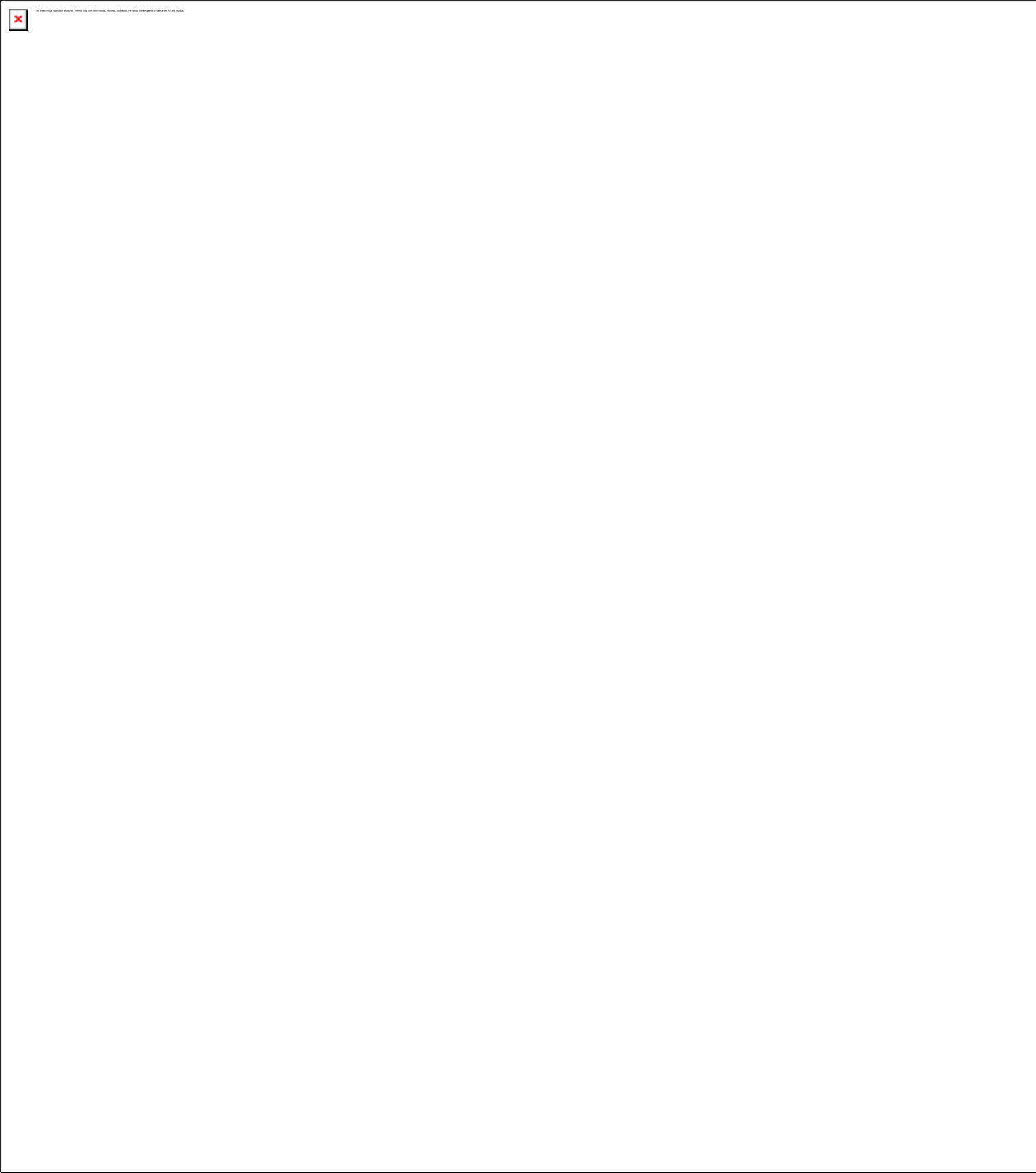


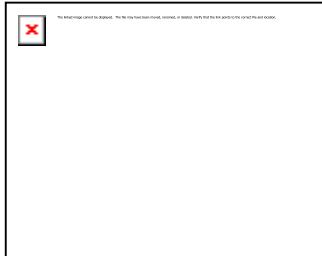


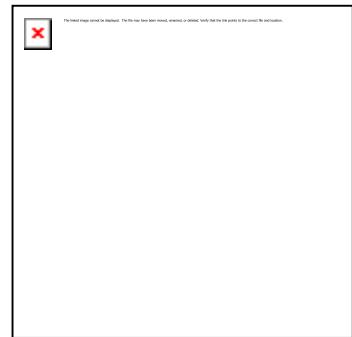
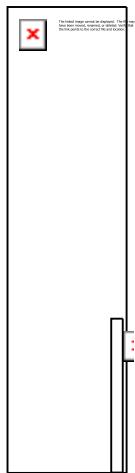


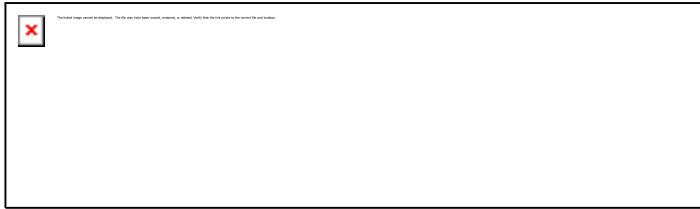






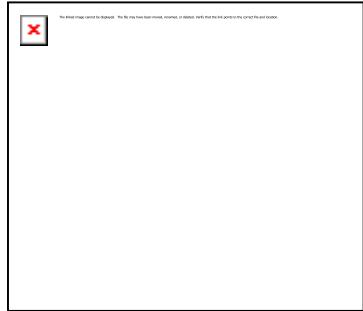
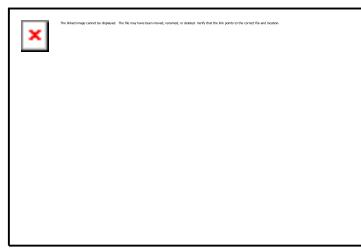


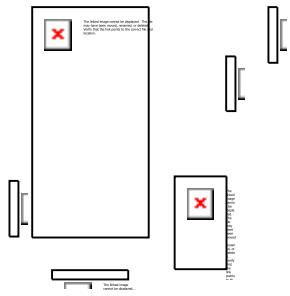
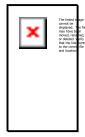


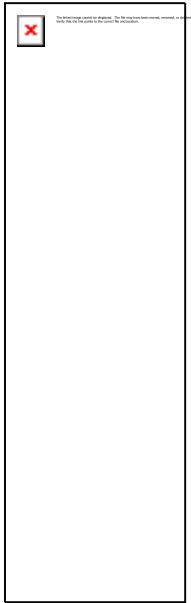
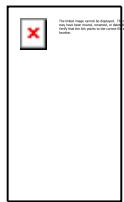


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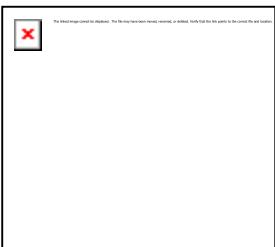
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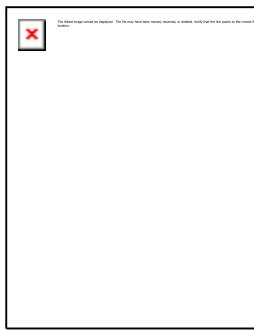
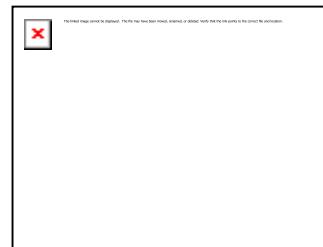
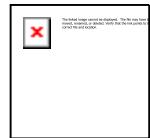
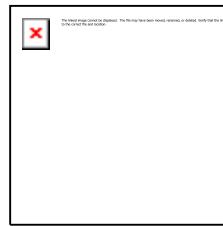


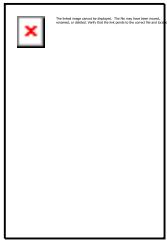
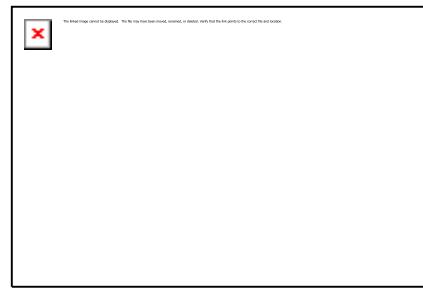


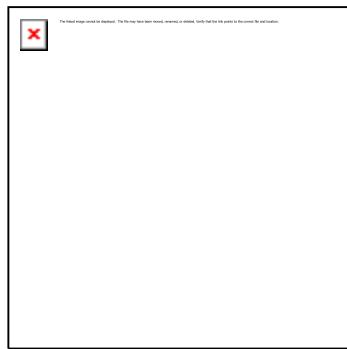
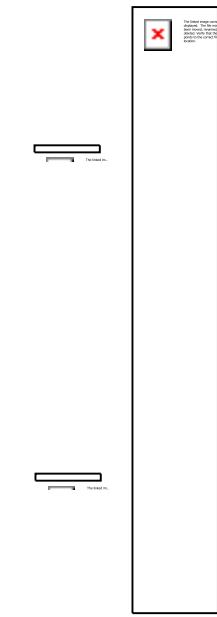
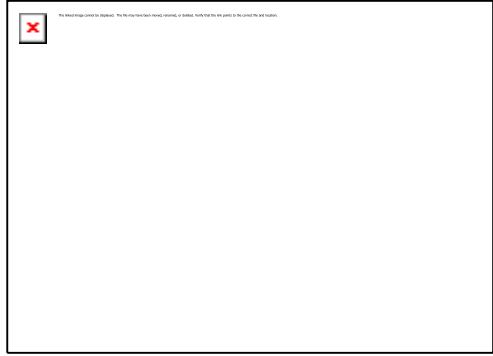


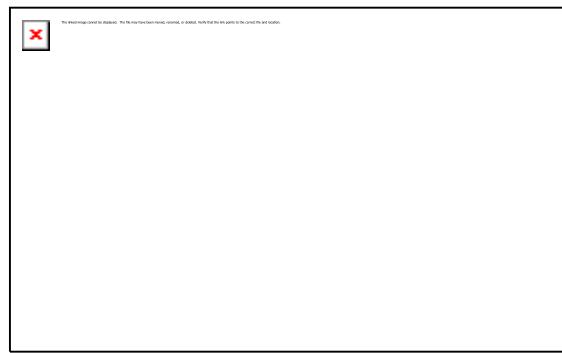
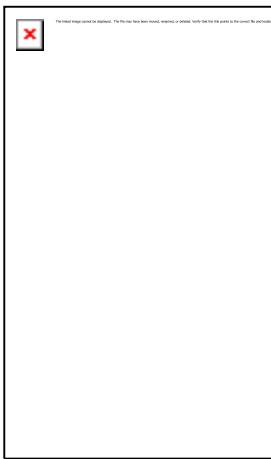
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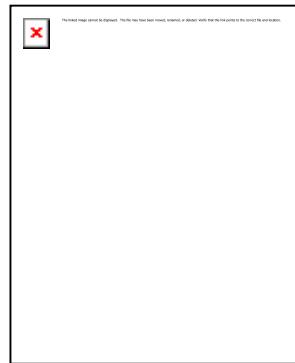


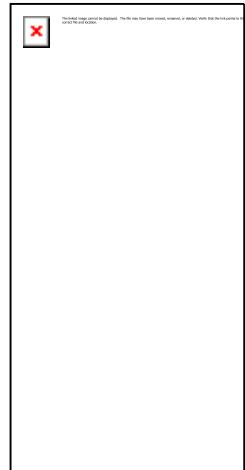


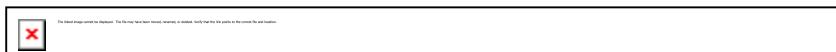


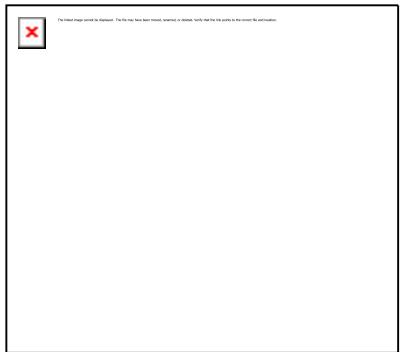


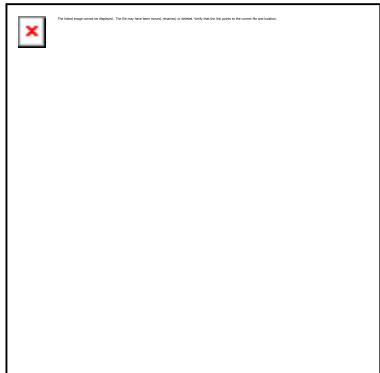
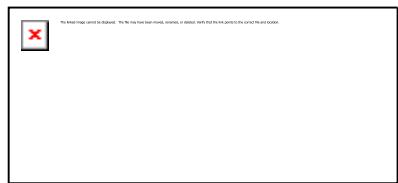


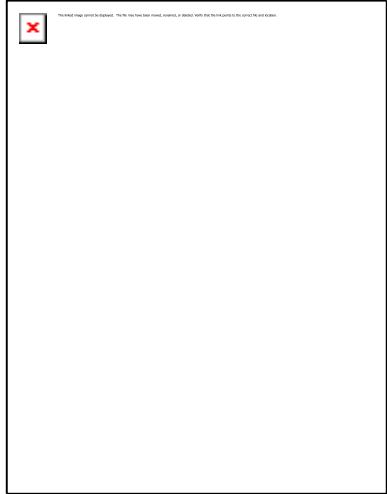


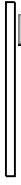
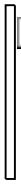


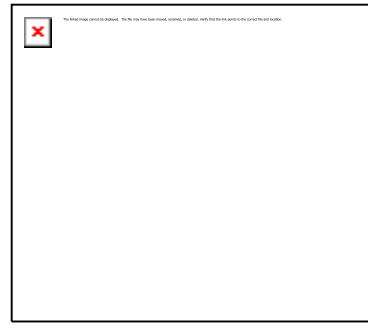




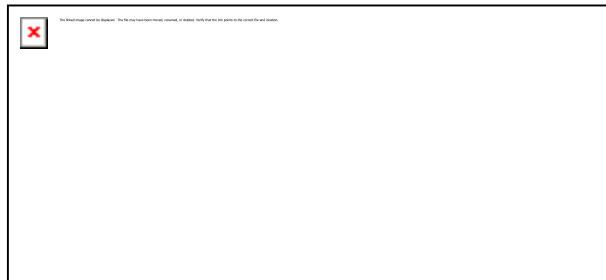
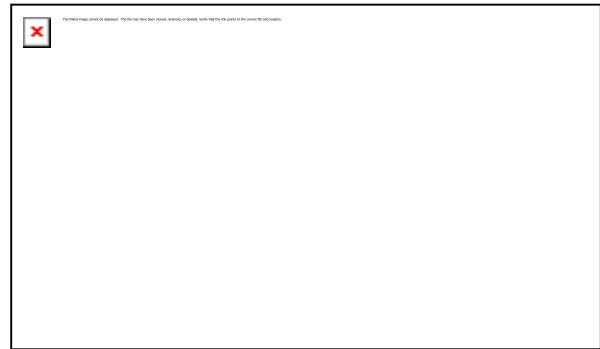


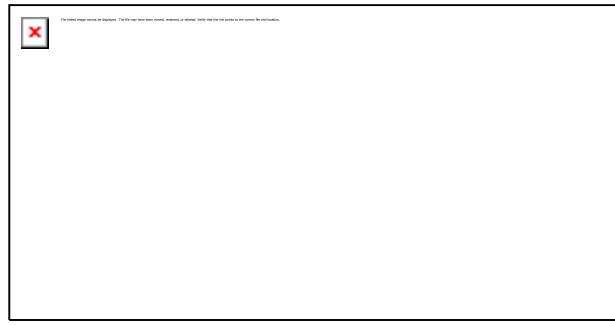
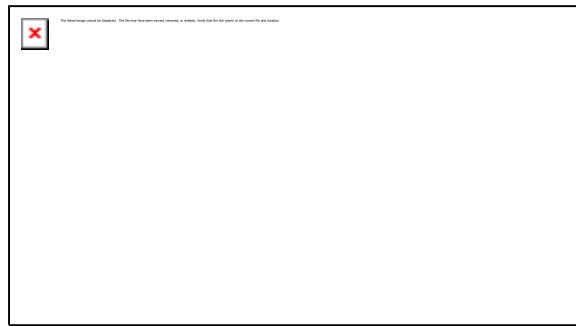






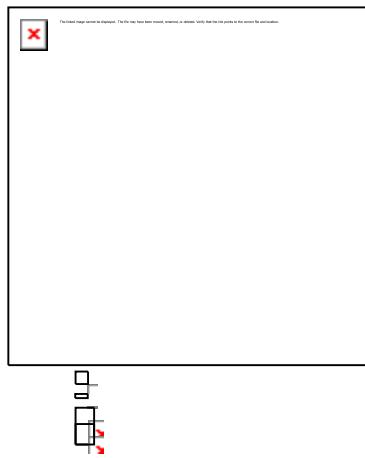






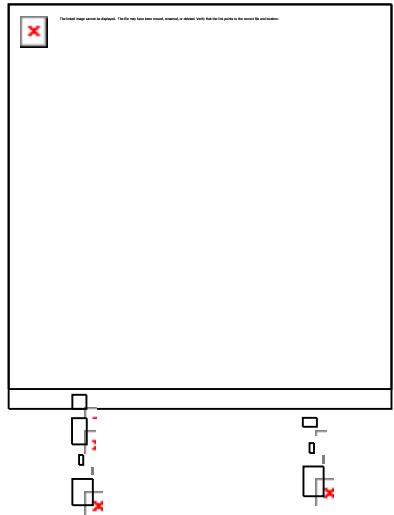
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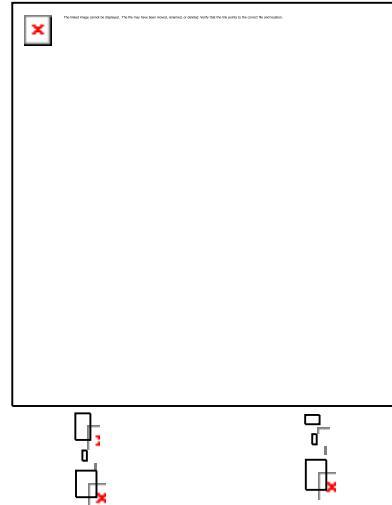


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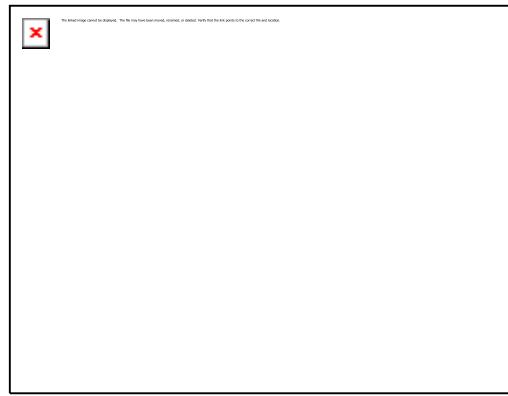




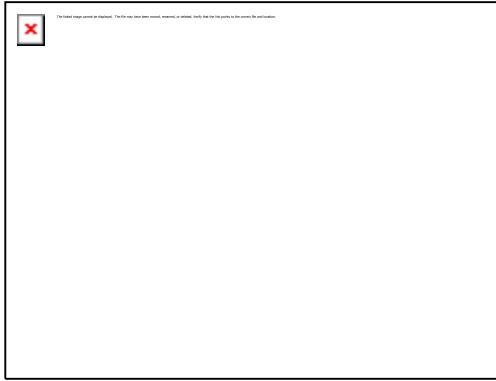


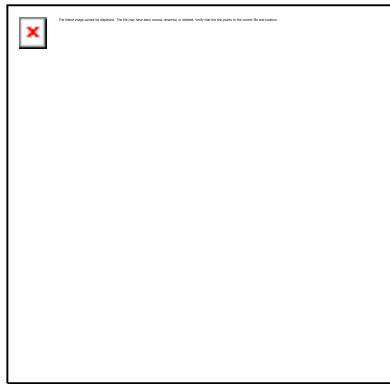


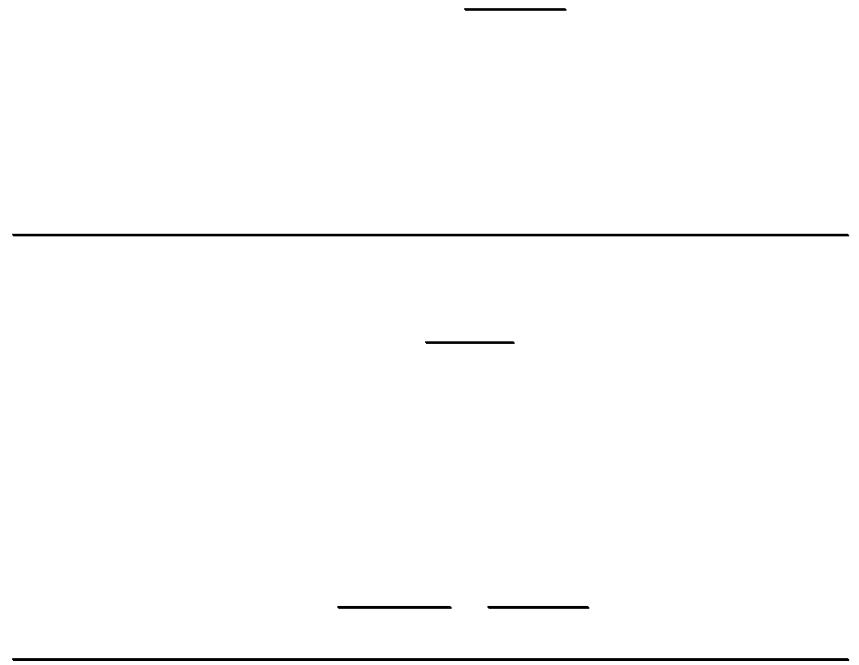
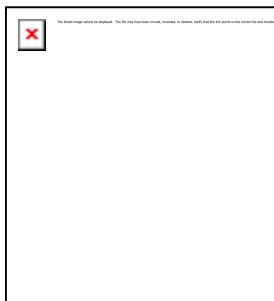
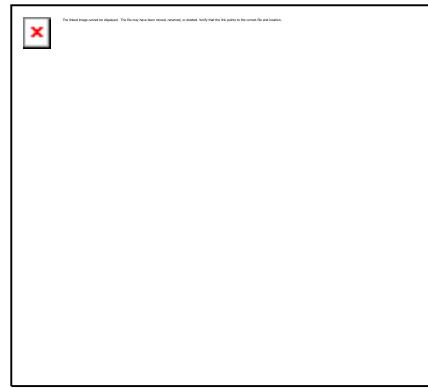
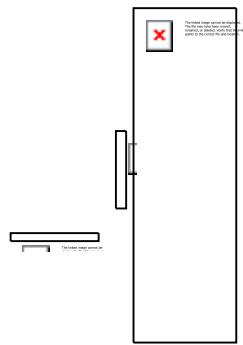


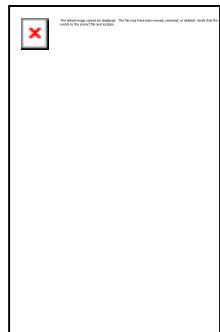
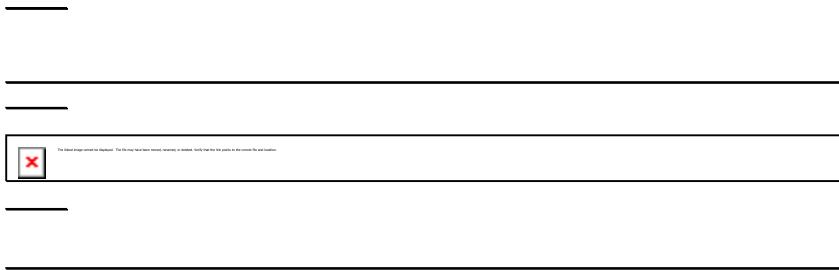


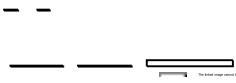
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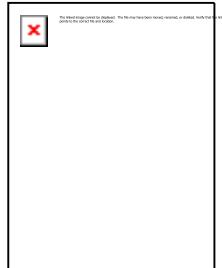
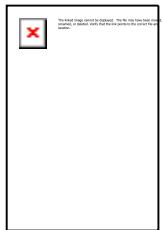
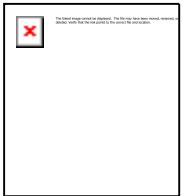
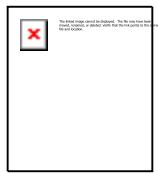


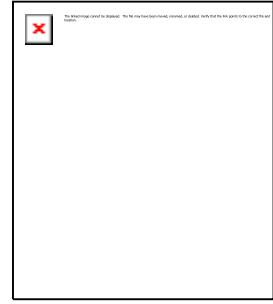
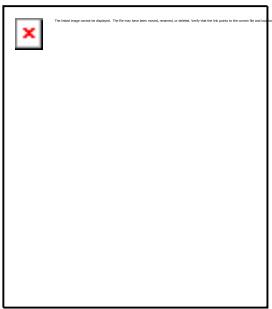


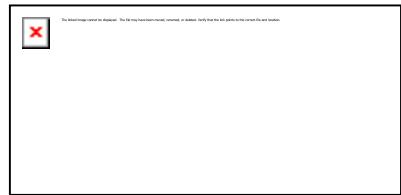


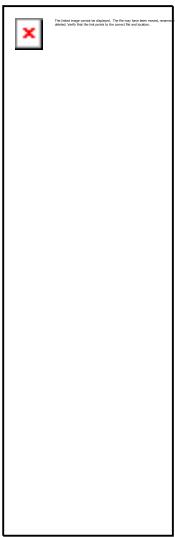


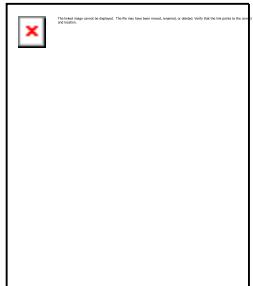


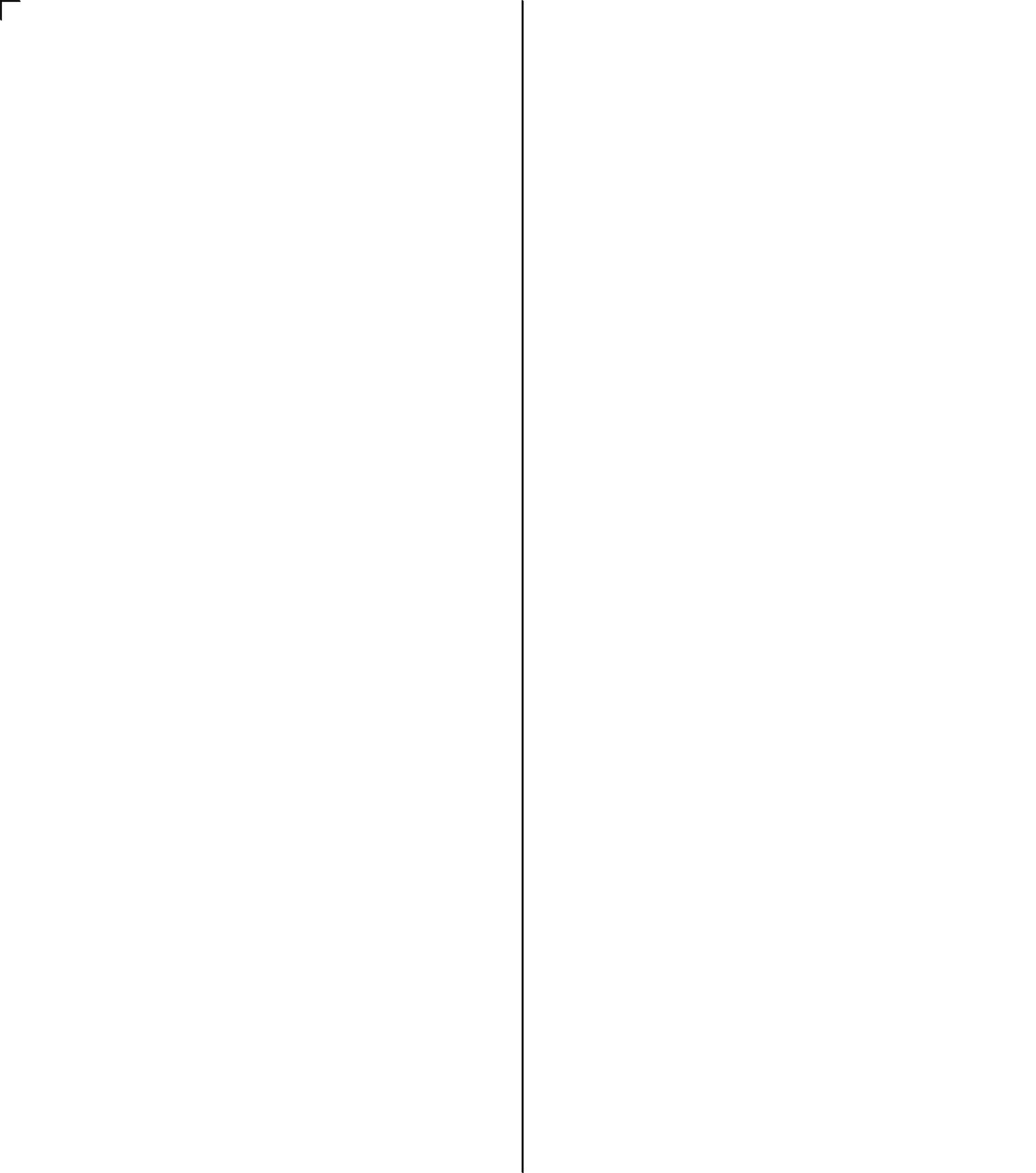




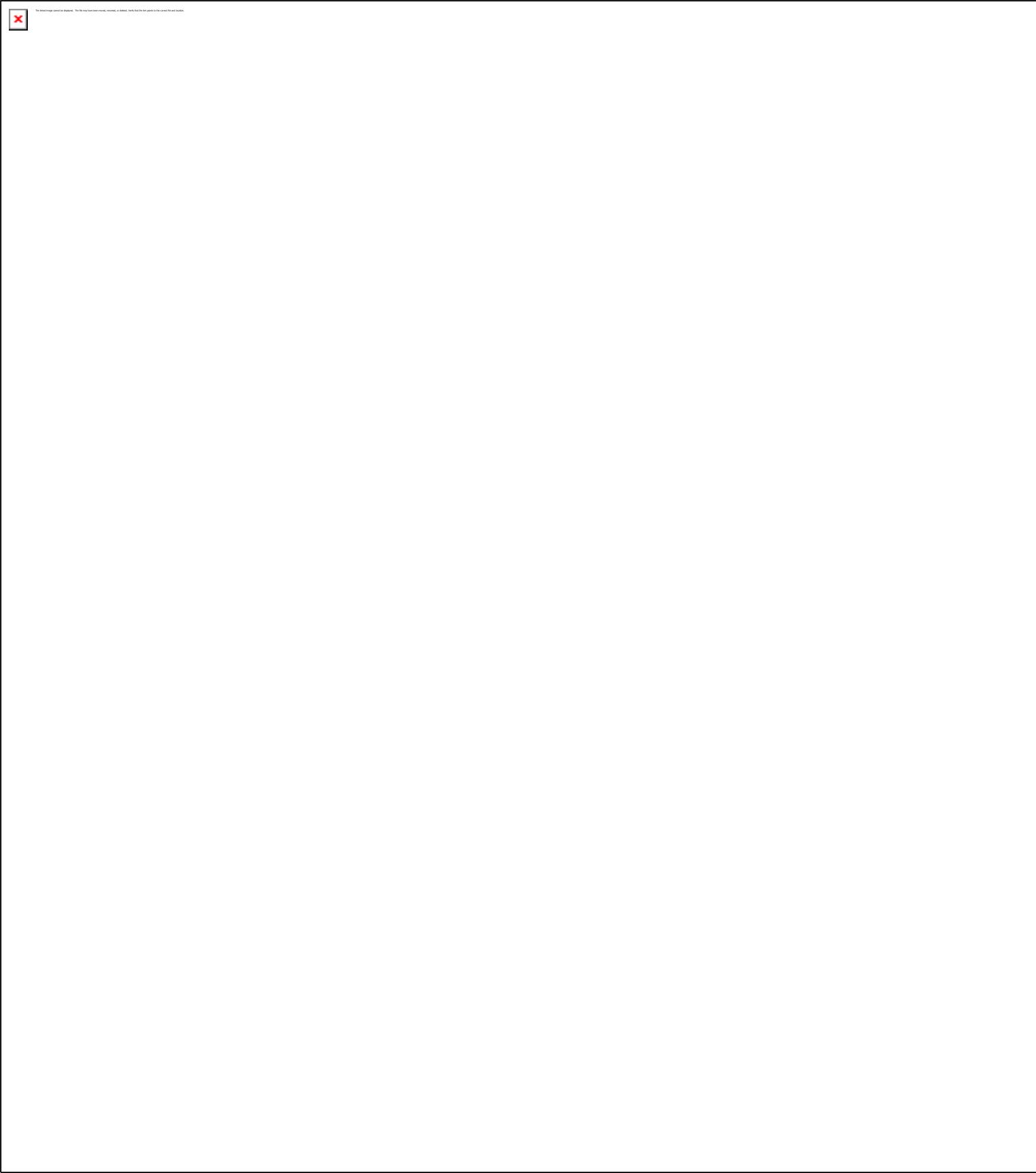








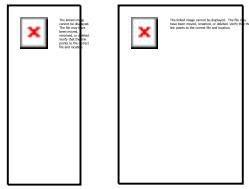


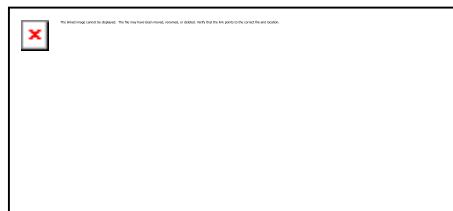




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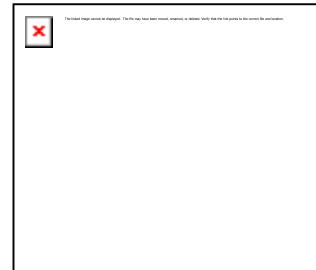
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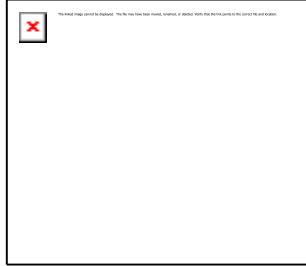
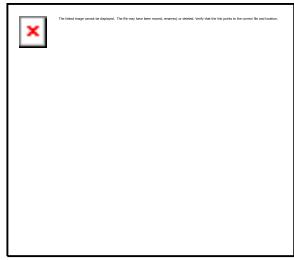
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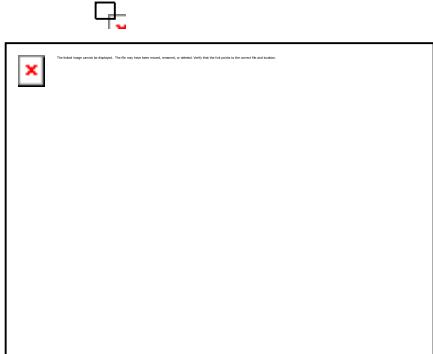
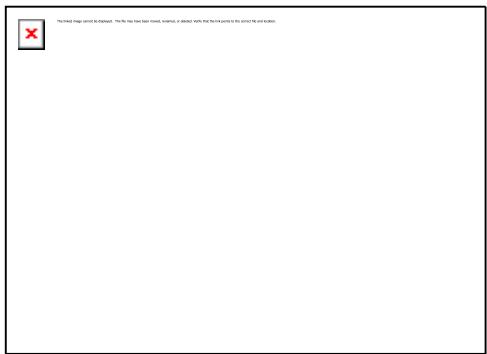
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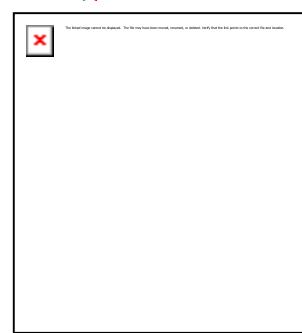
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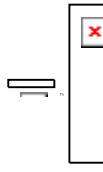
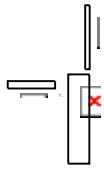


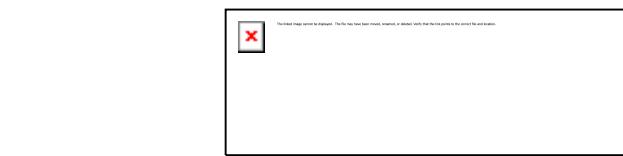
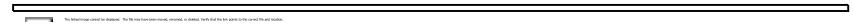
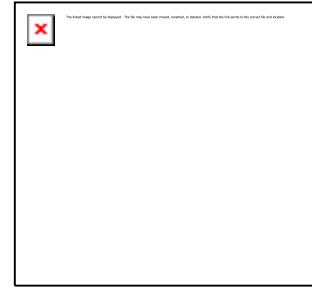
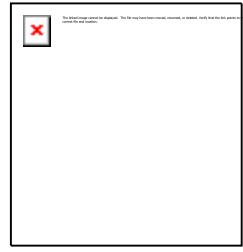


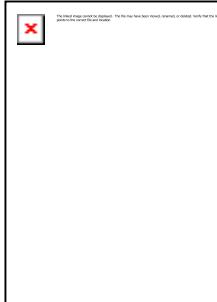
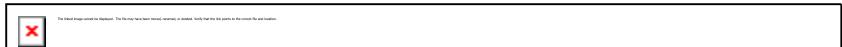
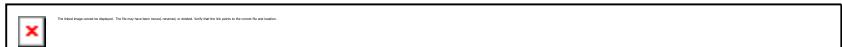


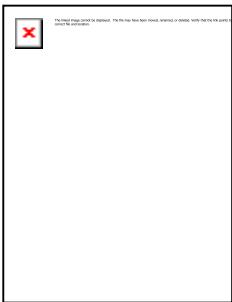


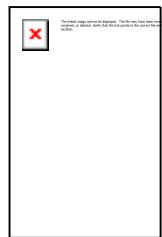
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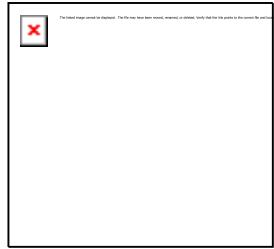




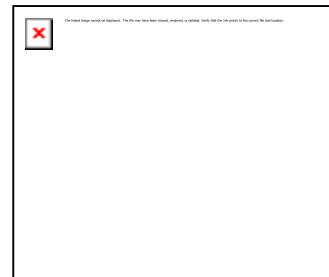




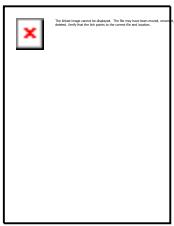




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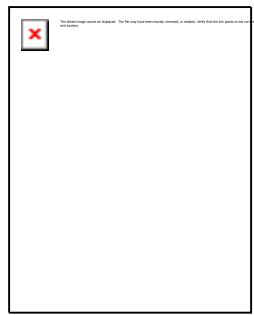
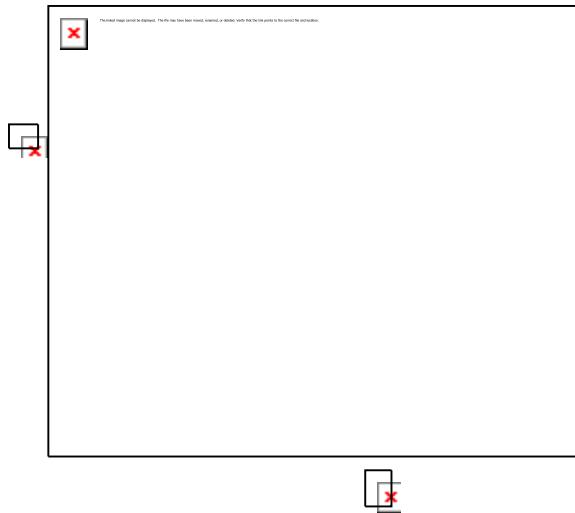


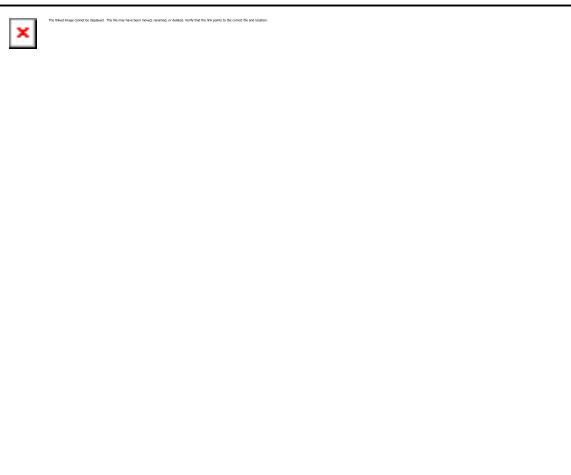
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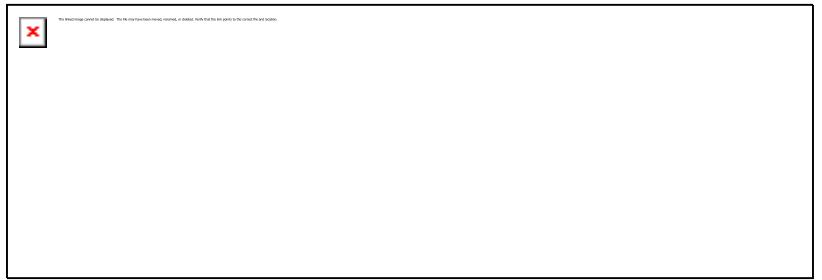
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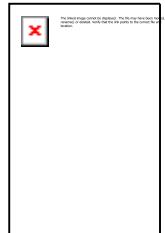
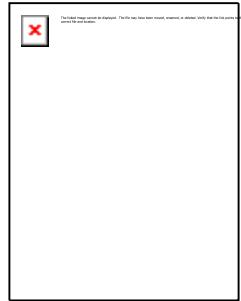


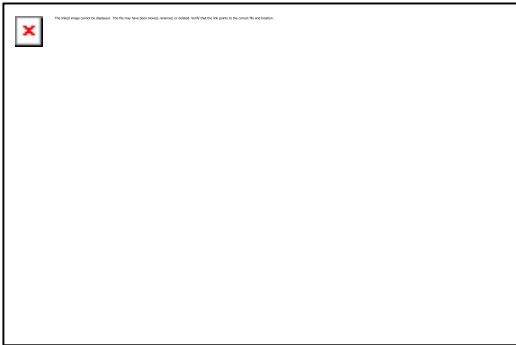


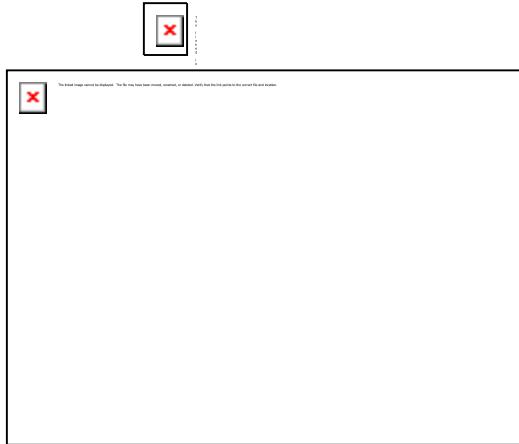
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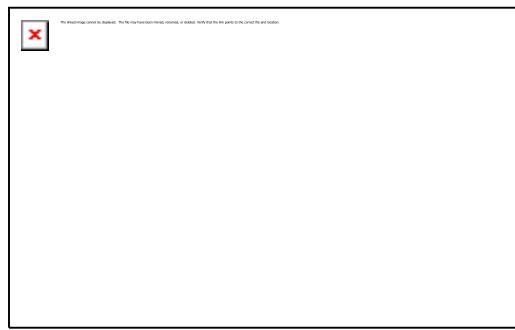


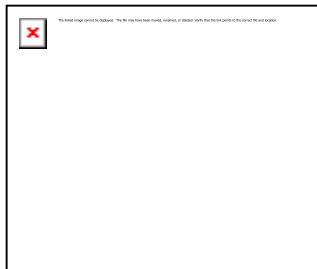


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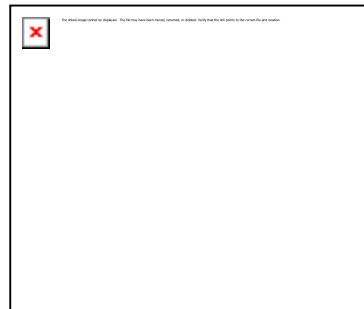


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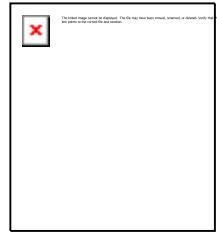


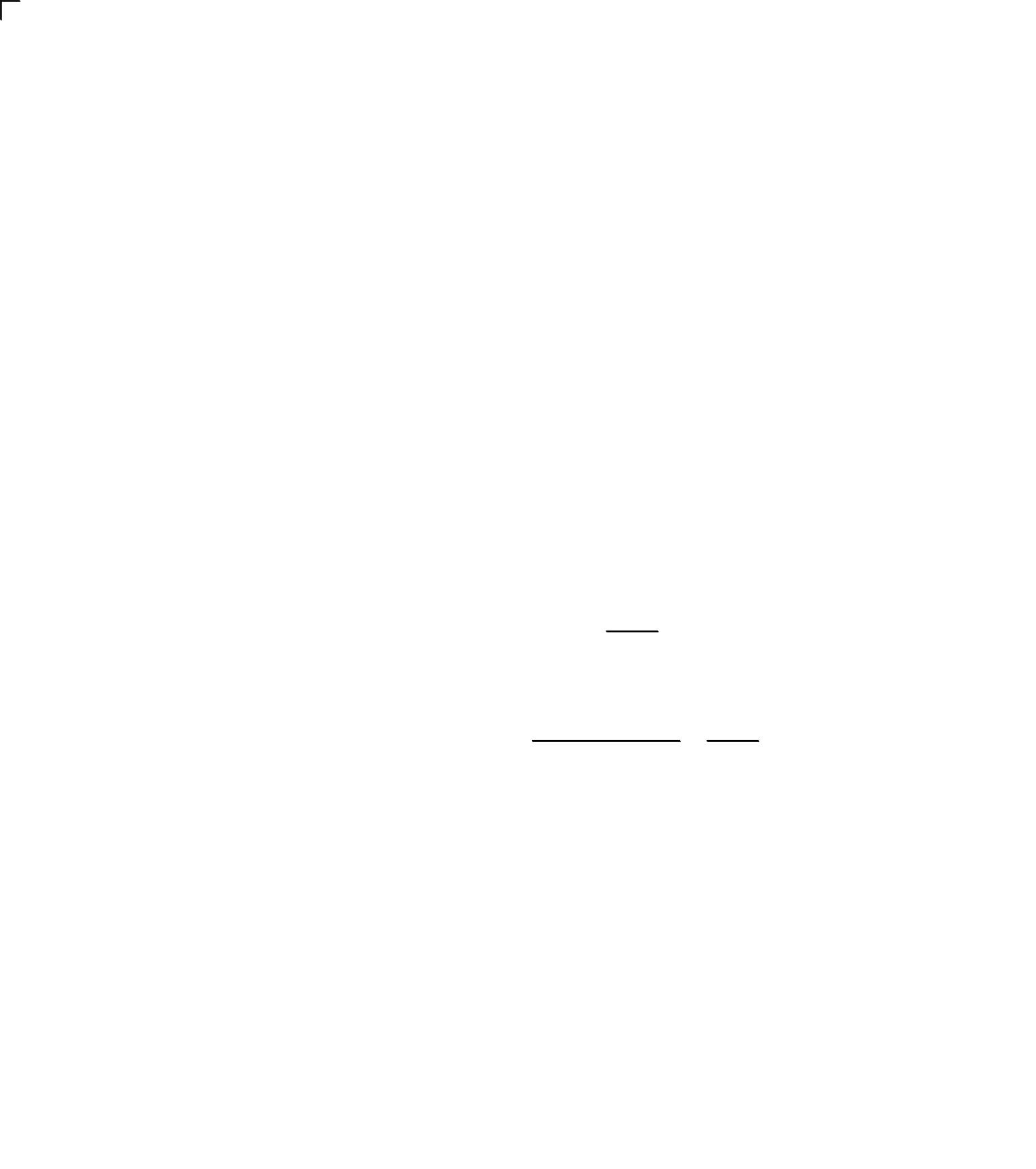


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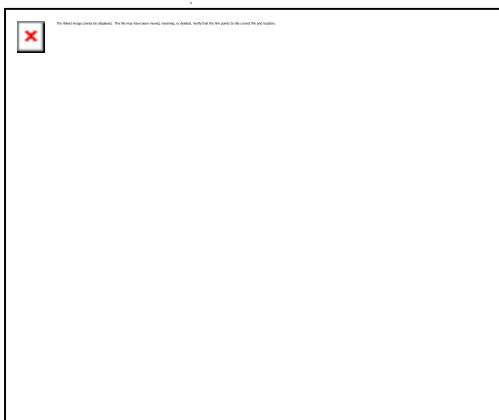
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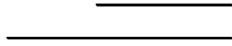


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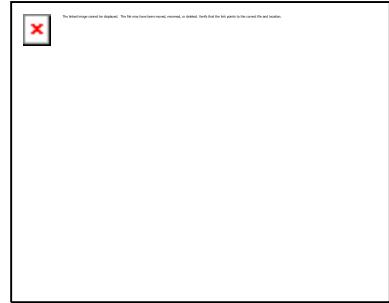
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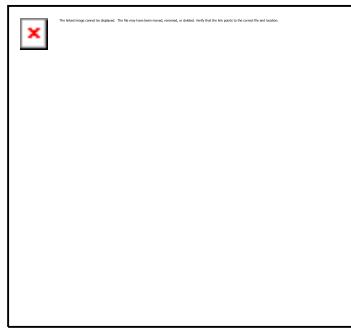
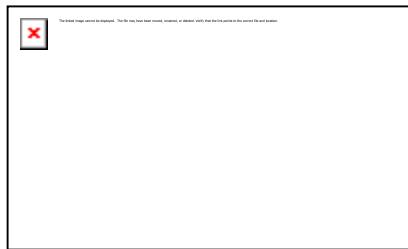


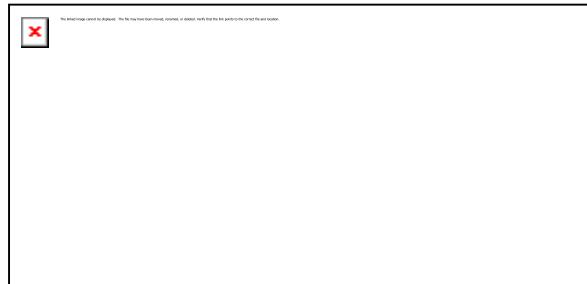
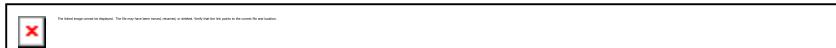
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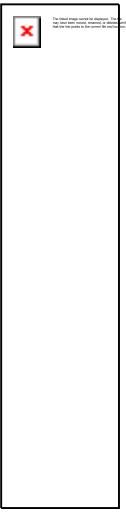


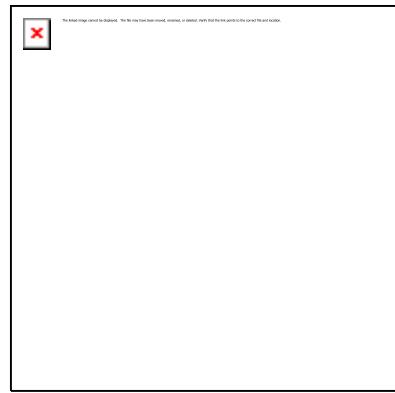






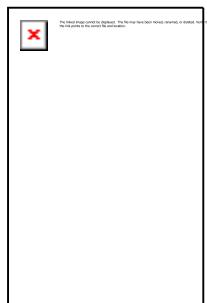
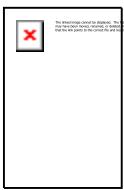


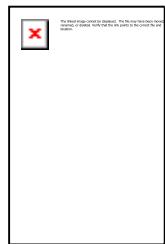
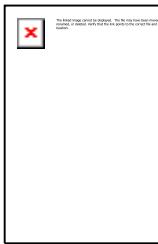
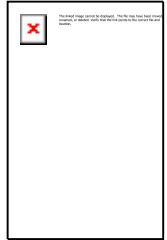


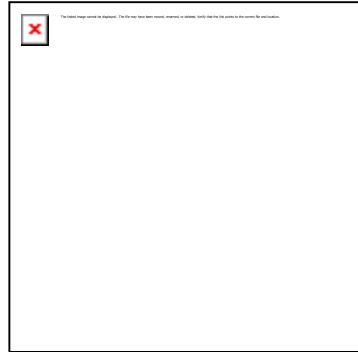


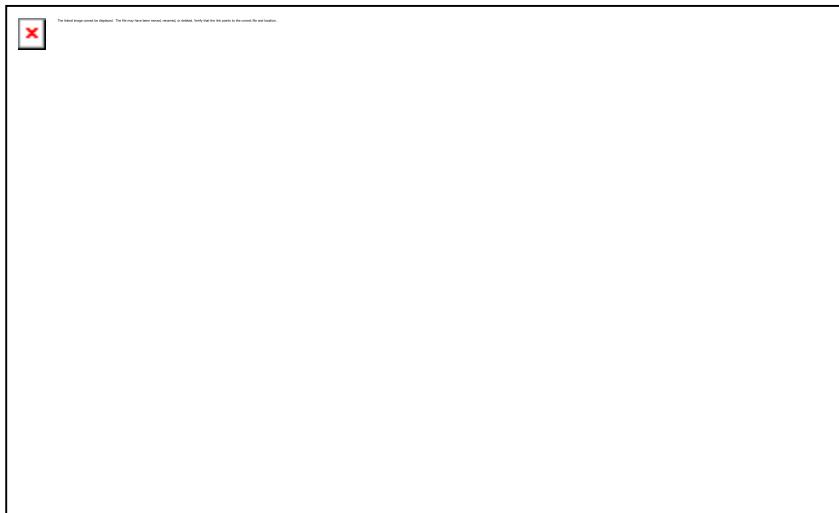
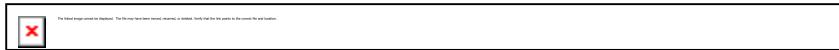
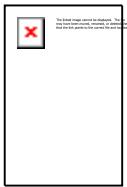
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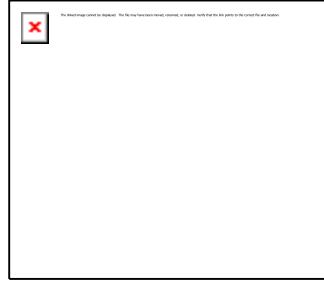


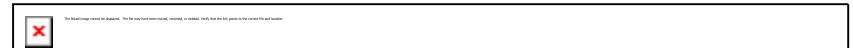
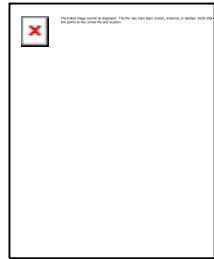
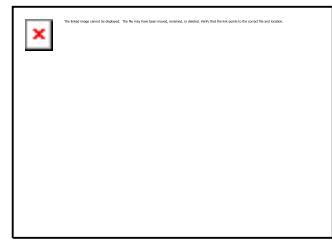






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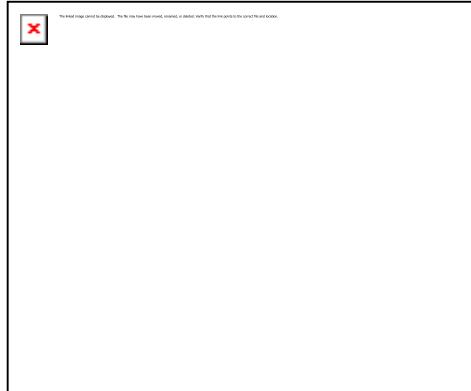


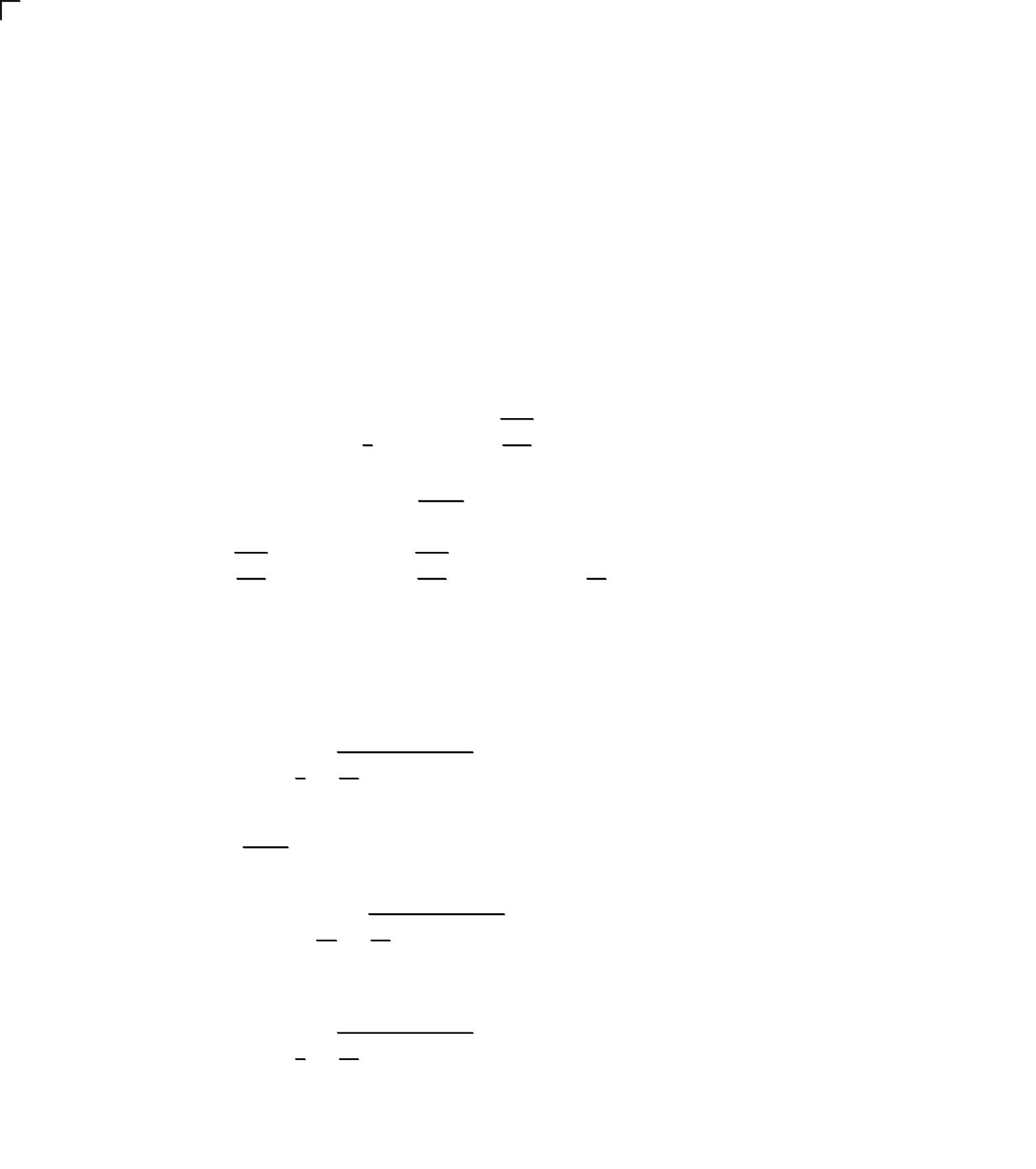
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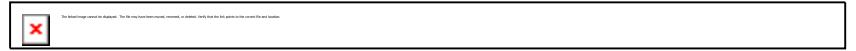


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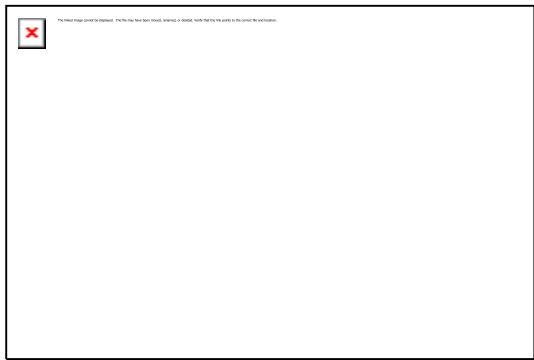
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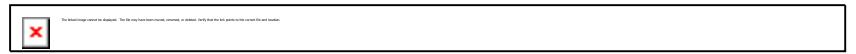


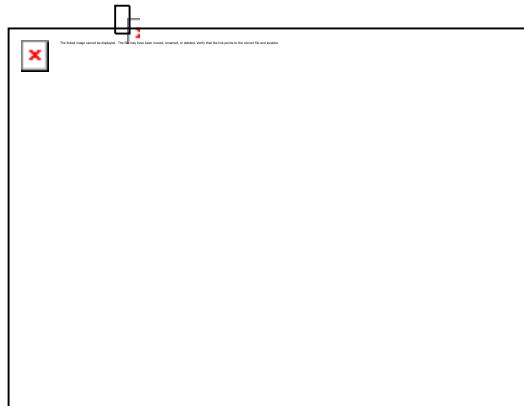
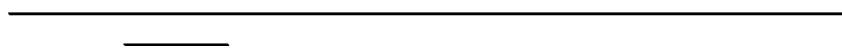


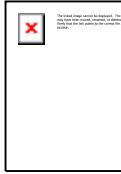
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$$i_D = K \frac{(V_{GS} - V_T)v}{2}^{DS - V_{DS2}} .$$

Substituting $V_{GS} = 2$ V - 1 V, $V_T = 1$ V, $v_{DS} = v_O$, and $K = 64$ mA/V², and simplifying, we get

$$i_D = 64 \times 10^{-3} v_O \frac{-v_O^2}{2} . \quad (7.77)$$

Equating the right-hand sides of Equations 7.76 and 7.77, and simplifying, we get the following equation for v_O :

$$33v_O^2 - 72v_O + 16 = 0,$$

which yields

$$v_O = 0.25V.$$

When v_O is 0.25 V it is easy to see that M1 is indeed in saturation and M2 is in the triode region.

7.9 SUMMARY

The last two chapters have discussed a set of progressively more elaborate models for the MOSFET. This section summarizes the models and discusses when it is appropriate to use each of them.

The simplest model for the MOSFET is the S model. This switch model models the on-off behavior of the MOSFET. Accordingly, the S model is appropriate when the designer cares only about the logical behavior of a circuit containing MOSFETs; in other words, where the voltage values of interest are only highs and lows. Thus, the S model is commonly used to arrive at the topology of a digital circuit to perform some given logical function. The S model is also useful in certain analog situations where the specific properties of the MOSFET beyond its on-off behavior have no effect on circuit behavior. Certain power circuits that use the MOSFET as a switch fall under this category.

The SR model of the MOSFET characterizes the behavior of the MOSFET as a resistor when the MOSFET is in its ON state, and v_{GS} is fixed. The SR model is appropriate for most types of simple analyses involving digital circuits, such as static discipline computations of voltage levels, simple power calculations, and, as will be discussed in later chapters, delay calculations. Although technically the SR model is valid only in the MOSFET's triode region (that is, when $v_{DS} < (v_{GS} - V_T)$), for simplicity, we ignore this limitation and apply it in digital circuit applications irrespective of the value of the drain voltage, since the model is such a gross simplification of the MOSFET's behavior in the first place.

The SCS model characterizes the behavior of the MOSFET in its saturation region. By designing analog circuitsto adhere to the saturation discipline, the SCS model is appropriate for most of our analog applications such as amplifiers and analog filters.

The SU model provides accurate models of the MOSFET in both the triode and the saturation regions, but is more complicated. In its saturation region, it behaves as the SCS model. So, for analog circuits that are designed to adhere to the saturation discipline its use is no different than the use of the SCS model. Thus the SU model is useful when the designer wishes to conduct very accurate analyses of digital or analog circuits in which the MOSFETs are allowed to operate in both their triode and saturation regions. To analyze a circuit containing MOSFETs, the designer first makes an educated guess as to the region — triode, saturated, or cutoff — in which each of the MOSFETs operates. Then, the designer writes node equations for the circuit, selecting appropriate device equations for each of the MOSFETs. After solving this set of equations for the node voltages and edge currents, the designer must confirm that their initial guesses as to the state of the MOSFET is consistent with the final node voltages. We leave a

detailed treatment of the SU model for more advanced courses on circuits. In the rest of this book, we will focus on the S, the SR, and the SCS models.

This chapter also introduced the MOSFET amplifier. The amplifier is an example of an nonlinear circuit. We chose to operate the amplifier under the saturation discipline so that it provided a voltage gain for an input signal and so that the MOSFET operated solely in its saturation region, where the SCS model applied. We also discussed the application of a DC offset voltage at the input of the amplifier to boost the signal of interest sufficiently so that the amplifier operated in saturation for the entire dynamic range of input signal variation. The application of a DC offset established a DC operating point for the amplifier.

We introduced large signal analysis for the amplifier. Large signal analysis summarizes how the amplifier behaves for large swings in the input signal and involves answering the following questions:

1. What is the relationship between the amplifier output v_o and its input v_{in} in the saturation region?
2. What is the range of valid input values for the amplifier under the saturation discipline? What is the corresponding range of valid output values?

The next chapter will discuss small signal analysis of the amplifier. Small signal analysis is appropriate when the input signal perturbations about the operating point are very small.

EXERCISES

exercise 7.1 Determine the voltage v_o across the voltage-dependent current source shown in the circuit in Figure 7.66 when

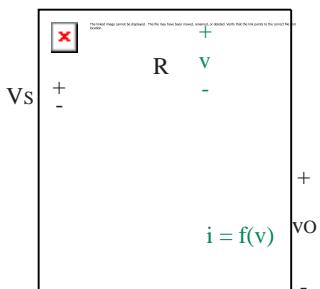


FIGURE 7.66

$$i = f(v) = v K_2$$

exercise 7.2 Consider the circuit containing the dependent current source shown in Figure 7.67.

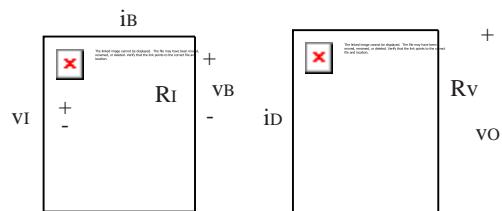


FIGURE 7.67

- Determine v_o in terms of v_i if $i_D = K_1 v_B$. What are the units of K_1 ?
- Determine v_o in terms of v_i if $i_D = K_2 i_B$. What are the units of K_2 ?
- Determine v_o in terms of v_i if $i_D = K_3 v_{B2}$. What are the units of K_3 ?
- Determine v_o in terms of v_i if $i_D = K_4 i_{B2}$. What are the units of K_4 ?

exercise 7.3 The resistance R in the circuit shown in Figure 7.68 depends on the voltage across resistor R_B . Determine v_B if

$$R = \frac{K}{v_B}.$$

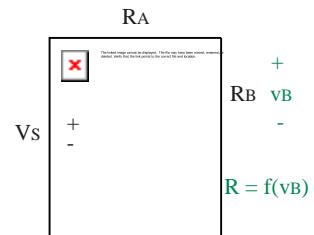


FIGURE 7.68

exercise 7.4 AMOSFET is characterized by the following equation:

$$i_{DS} = K_2(v_{GS} - V_T)^2$$

in its saturation region. AMOSFET operates in the saturation region for

$$v_{DS} \geq v_{GS} - V_T \text{ and } v_{GS} \geq V_T.$$

Express the $v_{DS} \geq v_{GS} - V_T$ constraint in terms of i_{DS} and v_{DS} .

exercise 7.5 The MOSFET in Figure 7.69 is characterized by the equation:

$$i_{DS} = K_2(v_{GS} - V_T)^2$$

in its saturation region according to the SCS model. The MOSFET operates in the saturation region for

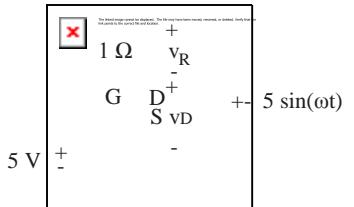


FIGURE 7.69

$$v_{DS} \geq v_{GS} - V_T \text{ and } v_{GS} \geq V_T.$$

The MOSFET operates in its triode region for

$$v_{DS} < v_{GS} - V_T \text{ and } v_{GS} \geq V_T.$$

Suppose the MOSFET is characterized by the SR model in its triode region. In other words,

$$i_{DS} = \frac{V}{R_{DS}}^{\text{ON}}$$

in the triode region. Assume that R_{ON} is a constant with respect to i_{DS} and v_{DS} , but its value is some function of v_{GS} . Further suppose that $i_{DS} = 0$ when $v_{GS} < V_T$:

a) For $v_{GS} = 5\text{V}$, what value of R_{ON} makes the MOSFET i_{DS} versus v_{DS} continuous between its triode and saturation regions of operation? characteristic

b) Plot v_R versus v_D for the circuit shown in Figure 7.69. This circuit is useful in plotting the MOSFET characteristics. Assume that $K = 1\text{mA/V}^2$ and $V_T = 1\text{V}$. Use the value of R_{ON} calculated in (a). Use a volt scale for V_D and a millivolt scale for v_R .

exercise 7.6 Consider the MOSFET amplifier shown in Figure 7.70. Assume that the amplifier is operated under the saturation discipline. In the saturation region, the MOSFET is characterized by the equation:

$$i_{DS} = K_2(v_{GS} - V_T)^2$$

where i_{DS} is the drain-to-source current when a voltage v_{GS} is applied across its gate-to-source terminals.

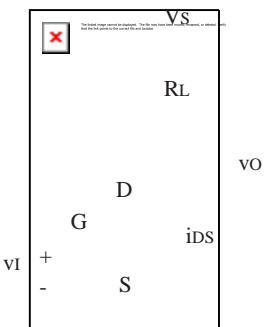


FIGURE 7.70

a) Draw the equivalent circuit for the amplifier based on the SCS model of the MOSFET.

b) Write an expression relating v_O to i_{DS} .

c) Write an expression relating i_{DS} to v_I .

d) Write an expression relating v_O to v_I .

e) Suppose that an input voltage V_I results in an output voltage V_O . By what factor must V_I be increased (or decreased) so that the output voltage is doubled?

f) Suppose, again, that an input voltage V_I results in an output voltage V_O . Suppose, further, that we desire an output voltage that is $2V_O$. Assuming that both the input voltage and the MOSFET do not change, what are all the possible ways of accomplishing the desired doubling of the output voltage?

g) The power consumed by the MOSFET amplifier in Figure 7.70 is given by $V_S i_{DS}$, assuming that no current is drawn out of the V_O terminal. Which of the alternatives for doubling V_O from parts (e) and (f) will result in the lowest power consumption?

exercise 7.7 Consider, again, the MOSFET amplifier shown in Figure 7.70. Assume that the amplifier is operated under the saturation discipline. The MOSFET in the drain is off if its threshold voltage is 0. In other words, the saturation region of the

MOSFET is now characterized by the equation:

$$i_{DS} = \frac{K_2}{2} v_{GS}$$

where i_{DS} is the drain-to-source current when a voltage v_{GS} is applied across its gate-to-source terminals. The following questions relate to the large-signal analysis of the amplifier:

- Derive the relationship between the output voltage v_o and the input voltage v_i .
- Derive the range of valid input voltages. Under the saturation discipline, valid input voltages are those that result in saturation region operation of the amplifier. Determine the corresponding range of output voltages (v_o) and output currents (i_{DS}).
- Suppose we wish to amplify an AC input signal v_i . Assume that v_i has a zero DC offset. Draw a circuit showing how a separate DC input voltage V_i can be used to bias the amplifier in a region where saturation region operation is achieved for both positive and negative excursions of v_i . Assuming the v_{ih} is symmetric positive and negative swings, how would you choose the input operating point for the amplifier that allows a maximum peak-to-peak voltage range for v_i ? What is the corresponding output operating point (v_o and i_{DS})?

exercise 7.8 The three-terminal device shown in Figure 7.71a is called a bipolar junction transistor (BJT). Figure 7.71b shows a piecewise-linear model for the device, in which the parameter β is a constant. When

$$i_B > 0$$

and

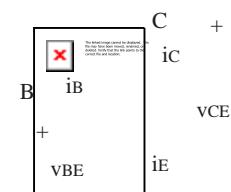
$$V_{CE} > V_{BE} - 0.4 \text{ V},$$

the emitter diode behaves like a short circuit, the collector diode like an open circuit, and the collector current is given by:

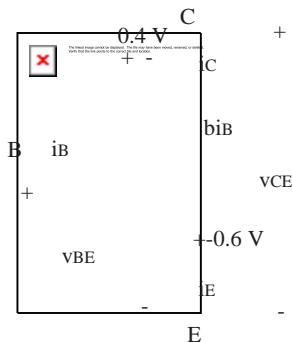
$$i_C = \beta i_B.$$

Under the given constraints, the BJT is said to operate in its active region. For the rest of this exercise, assume that $\beta = 100$:

- Determine the collector current i_C for a base current $i_B = 1 \mu\text{A}$ and $V_{CE} = 2 \text{ V}$ using the model in Figure 7.71b.



(a)



(b)

FIGURE 7.71 (a) A bipolar junction transistor. B stands for base, E for emitter, and C for collector; (b) a piecewise-linear model for the BJT.

b) Sketch a graph of v_{o} versus v_{ce} for $i_b = 1 \mu A$. Using the model in Figure 7.71b. In drawing this graph, assume that the current source turns off for

$$v_{ce} \leq v_{be} - 0.4V.$$

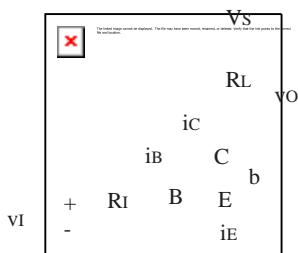


FIGURE 7.72

exercise 7.9 Consider the bipolar junction transistor (BJT) amplifiers shown in Figure 7.72. Assume that the BJT is characterized by the large signal model from Exercise 7.8, and that the BJT operates in its active region. Assume further that $V_s = 5 V$, $R_L = 10 k\Omega$, $R_E = 500 k\Omega$, and $\beta = 100$.

- a) Draw the equivalent circuit for the BJT amplifier based on the large signal BJT model from Exercise 7.8.
- b) Write an expression relating v_o to i_C .
- c) Write an expression relating i_C to v_i .
- d) Write an expression relating i_E to i_B .
- e) Write an expression relating v_o to v_i .
- f) What is the value of v_o for an input voltage $v_i = 0.7 V$? What are the corresponding values of i_B , i_C , and i_E ?

exercise 7.10 In this exercise you will perform a large signal analysis of the BJT amplifiers shown in Figure 7.72. Assume that the BJT is characterized by the large signal model from Exercise 7.8. Assume further that $V_s = 5 V$, $R_L = 10 k\Omega$, $R_E = 500 k\Omega$, and $\beta = 100$.

- a) Write an expression relating v_o to v_i .
- b) What is the lowest value of the input voltage v_i for which the BJT operates in its active region? What are the corresponding values of i_B , i_C , and v_o ?
- c) What is the highest value of the input voltage v_i for which the BJT operates in its active region? What are the corresponding values of i_B , i_C , and v_o ?
- d) Sketch a graph of v_o versus v_i for the four parameter values given.

PROBLEMS

problem 7.1 Consider the MOSFET voltage divider circuit shown in Figure 7.73. Assume that both MOSFETs operate in the saturation region. Determine the output voltage v_o as a function of the supply voltage V_s , the gate voltages V_A and V_B , and the MOSFET geometries L_1 , W_1 , and L_2 , W_2 . Assume that the MOSFET threshold voltage is V_T , and remember, $K = K_n W/L$.

problem 7.2 An inverting MOSFET amplifier is shown in Figure 7.74, together with an i_{DS} characteristic for the MOSFET. This characteristic is simpler than the SCS model presented in this chapter. The characteristic is simply the standard MOSFET characteristic with the triode region compressed onto the y -axis.

Alternatively, this characteristic can be viewed as describing ideal switch behavior that is extended to exhibit a saturating drain-source current. In other words, for $v_{GS} < V_T$, the MOSFET behaves like an open switch with $i_{DS} = 0$. For $v_{GS} \geq V_T$, the MOSFET behaves like a closed switch with $v_{DS} = 0$ provided that $i_{DS} < K/2(v_{GS} - V_T)^2$. However, once i_{DS} reaches $K/2(v_{GS} - V_T)$, which is the maximum current the MOSFET can carry for a given v_{GS} , MOSFET operation enters a saturation region in which the MOSFET behaves as a current source of value $K/2(v_{GS} - V_T)^2$. Saturated operation is as described by the saturation model given in Figure 7.74.

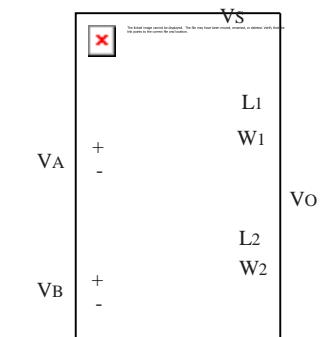


FIGURE 7.73

- Determine v_{OUT} as a function of v_{IN} for $0 \leq v_{IN}$
- What is the lowest value of v_{IN} for which $v_{OUT} = 0$?
- Assume that $V_S = 15V$, $R = 15k\Omega$, $V_T = 1V$, and $K = 2mA/V^2$. Graph v_{OUT} versus v_{IN} for $0V \leq v_{IN} \leq 3V$.
- On the input-output graph, identify the regions over which the MOSFET behaves as an open circuit, behaves as a short circuit, and exhibits saturated behavior.

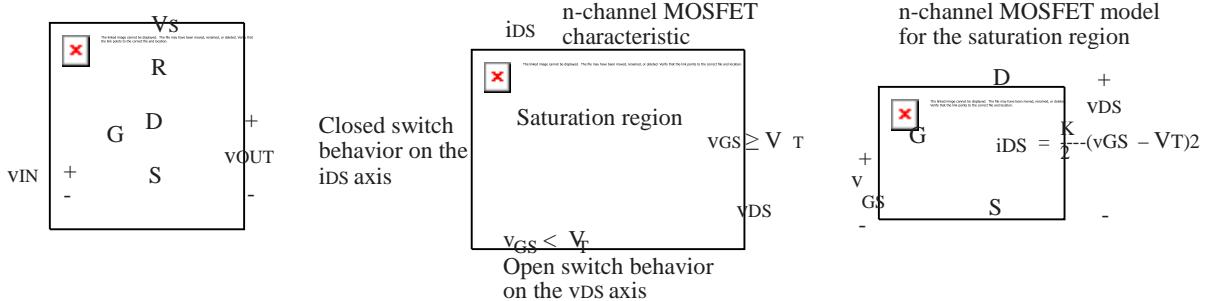
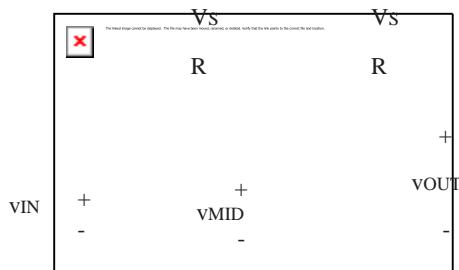


FIGURE 7.74

problem 7.3 A two-stage amplifier is shown in Figure 7.75. It is constructed by cascading two one-stage amplifiers of the type seen in Problem 7.2. In analyzing this amplifier, use the MOSFET model described in Problem 7.2 and illustrated in Figure 7.74.

FIGURE 7.75



a) The fact that a second amplifier stage is connected to the first amplifier stage does not change the operation of the first stage. That is, the relation between v_{MID} and v_{IN} here is the same as the relation between v_{OUT} and v_{IN} in Problem 7.2. Why? What terminal characteristic of the second MOSFET must change in order for this not to be true?

b) Derive the relation between v_{MID} and v_{IN} for $0 \leq v_{IN}$, and the relation between v_{OUT} and v_{MID} for $0 \leq v_{MID} \leq V_s$. (Hint: see Problem 7.2.)

c) Derive the relation between v_{OUT} and v_{IN} for $0 \leq v_{IN}$.

d) Determine the range of input voltages for which both MOSFETs operate under the saturation discipline. What are the corresponding ranges for v_{MID} and v_{OUT} ?

e) Using the numerical parameters given in Problem 7.2, graph v_{OUT} versus v_{IN} for v_{IN} for $0 \leq v_{IN} \leq 3V$. Compare this graph to the input-output graph found in Problem 7.2, and explain the differences.

problem 7.4 Consider again the two-stage amplifier shown in Figure 7.75. Suppose that the MOSFETs are characterized by the following equation in their saturation region:

$$i_{DS} = \frac{K_2}{2} \cdot \frac{v_{GS}}{V_T}$$

In other words, the threshold voltage $V_T = 0$. Furthermore, the MOSFETs operate in their saturation region when

$$v_{DS} \geq v_{GS} \text{ and } v_{GS} \geq 0.$$

Show that there is only one input voltage for which both stages simultaneously operate under the saturation discipline. What is that input voltage?

problem 7.5 Consider the “source-follower” or “buffer” circuit shown in Figure 7.76. Use the SCS MOSFET model (with parameters V_T and K) to perform

alarge-signalanalysisofthiscircuitaccordingtothefollowingsteps:

a) AssumingthattheMOSFEToperatesinitssaturationregion, showthat v_{OUT} is relatedtov IN accordingto

$$v_{OUT} = \frac{(2/RK) + 4(v_{IN} - V_T) - 2/RK}{2}^2.$$

b) Determine the range of V_{IN} over which the assumption of saturated MOSFET operationholds.Whatisthecorrespondingrangefor v_{OUT} ?

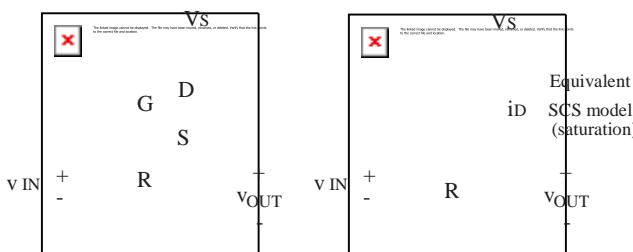


FIGURE 7.76

problem 7.6 ThisproblemstudiestheuseofamythicalMOSFET-likedevice calledaZFETtoconstructanamplifierasshowninFigure7.77.TheZFEToperates initssaturationregionwhen $v_{GS} \geq 0$ and $v_{DS} > 0$. Inthisregion, thedrain-source terminalrelationis $i_{DS} = K v_3^3$, where K isconstanthavingunitsof A/V^3 . When $v_{DS}=0$,theZFETexhibitsashortcircuitbetweenitsdrainandsourcerterminals, andis saidtooperateoutsideitssaturationregion.Similarly, theZFETexhibitanopencircuit for $v_{GS} < 0$ asitoperatesoutsideitssaturationregion.Finally, thegateterminal always exhibits an open circuit. These characteristics are summarized in Figure 7.77, beneaththesymbolfortheZFET.

a) AssumingssaturatedoperationoftheZFET,determine v_{OUT} asafunctionof V_{IN} .

b) Overwhatrangeof V_{IN} willtheZFEToperatesinitssaturationregion?

c) Assumethat $V_S=10V$, $R_L=1k$,and $K=0.001A/V^3$.Sketchandclearlylabel

v_{OUT} asafunctionof v_{IN} for $-1V \leq v_{IN} \leq 3V$.

d) Giventheparametersofpart(c), cantheamplifierbeusedasaninverterthatprovides

avalidoutputhighvoltagethresholdof $V_H=7V$?Whyorwhynot?Assumethat $V_L=2V$.

e) Giventheparametersofpart(c), cantheamplifiercanbeusedasaninverterthat

providesavalidoutputhighvoltagethresholdof $V_H=7V$?Whyorwhynot?This timearound, assumethat $V_L=1V$.

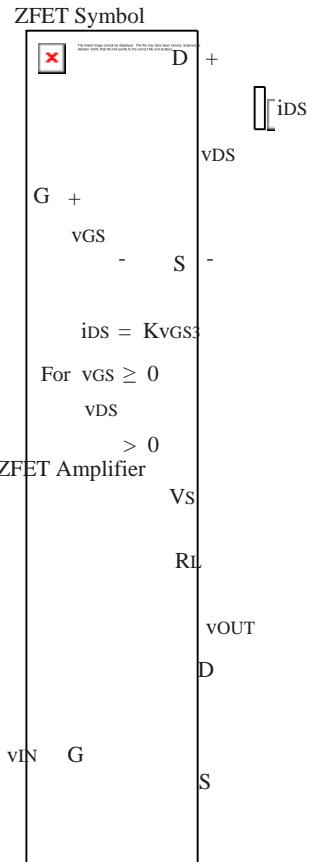


FIGURE 7.77

problem 7.7 Consider the difference amplifier circuit shown in Figure 7.78. Notice that the difference amplifier is powered by $+V_S$ and $-V_S$ power supplies. Assume that all MOSFETs operate under the saturation discipline, and, unless indicated otherwise, are characterized by the parameters K and V_T .

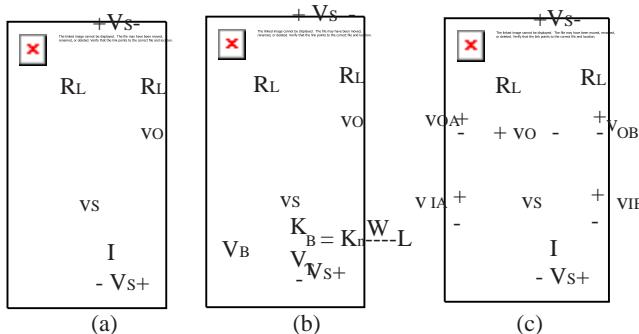


FIGURE 7.78

a) Determine v_o and v_{ds} for the connections shown in Figure 7.78a. In this figure, the gates of the MOSFETs are connected to ground.

b) Consider the difference amplifier version shown in Figure 7.78b. In this figure, a MOSFET implementation of a current source replaces the abstract current source from Figure 7.78a. Determine values for V_B and W/L such that the circuit in (b) is equivalent to that in (a).

c) The difference amplifier in Figure 7.78c is driven by two input voltages v_{IA} and v_{IB} as shown. Assume that the input voltage v_{IA} satisfies the following constraint $v_{IA} = -v_{IB}$ at all times. Determine v_{OA} , v_{OB} , and v_o as a function of v_{IA} .

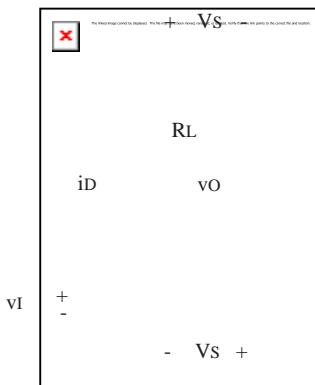


FIGURE 7.79

problem 7.8 Consider the amplifier circuit shown in Figure 7.79. The amplifier is powered by a $+V_S$ and a $-V_S$ power supply.

a) Determine v_o and i_D as a function of v_I under the saturation discipline. Assume that the MOSFET parameters K and V_T are given.

b) Determine the range of valid input voltages for saturation region operation. Determine the corresponding valid range for v_o and i_D .

c) Determine the output voltage when the input is grounded; in other words, for $v_I=0$.

d) Determine the value of v_I for which $v_o=v_I$ in terms of V_S , R_L , and the MOSFET parameters.

problem 7.9 Consider the current mirror circuit in Figure 7.80.

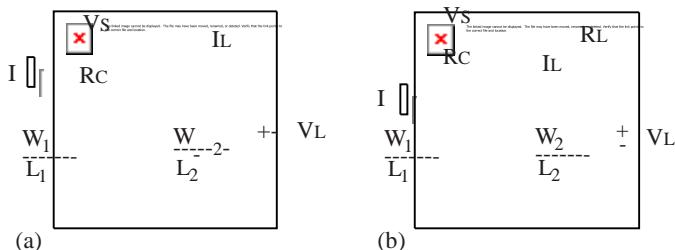


FIGURE 7.80

- Referring to Figure 7.80a, determine I_L as a function of I assuming both MOSFETs operate under the saturation discipline. Both MOSFETs have the same values for K_n and V_T . Does I_L change if V_L changes? What are the conditions under which $I_L = I$?
- Now consider Figure 7.80b. The current I can be increased either by increasing V_S or decreasing R_C . Assuming that either V_S or R_C may be changed, and that $W_1/L_1 = W_2/L_2 \geq W/L$, determine the range of values of I for which both MOSFETs operate under the saturation discipline. Assume both MOSFETs have the same values for K_n and V_T .

problem 7.10 Consider the circuit shown in Figure 7.81. Assume that the MOSFET operates under the saturation discipline.

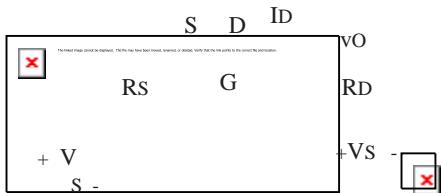


FIGURE 7.81

- Draw the SC equivalent circuit by replacing the MOSFET by its SC model.
- Determine v_o and i_d in terms of R_D , R_S , V_S , and the MOSFET parameters K and V_T .

problem 7.11 Consider the “common-gate amplifier” circuit shown in Figure 7.82. Assume that the MOSFET operates under the saturation discipline.

- Draw the SC equivalent circuit by replacing the MOSFET by its SC model.

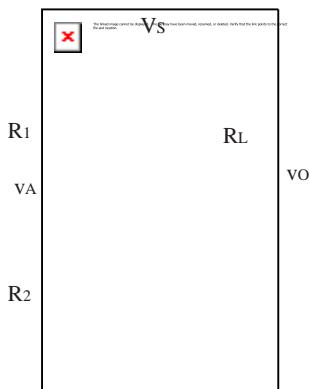


FIGURE 7.83

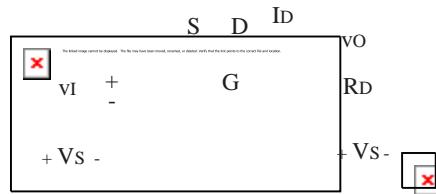


FIGURE 7.82

b) Determine v_o and i_d in terms of v_i , R_D , V_s , and the MOSFET parameters K and V_T .

c) Determine the range of values of v_i for which the MOSFET operates under the saturation discipline. What is the corresponding range of v_o ?

problem 7.12 Consider the MOSFET circuit shown in Figure 7.83. Determine the value of v_o in terms of the other circuit parameters. Assume the MOSFET is in saturation and is characterized by the parameters K and V_T .

problem 7.13 Consider the MOSFET circuit shown in Figure 7.84. Determine the value of v_o in terms of the other circuit parameters. Assume the MOSFET is in saturation and is characterized by the parameters K and V_T .

problem 7.14 Figure 7.85 shows a MOSFET amplifier driving a load resistor R_L . The MOSFET operates in saturation and is characterized by parameters K and V_T . Determine v_{out} versus v_{in} for the circuit shown.

problem 7.15 Determine v_{out} versus v_{in} for the circuit shown in Figure 7.86. Assume that the MOSFET operates in saturation and is characterized by the parameters K and V_T . What is the value of v_{out} when $v_{in}=0$?

problem 7.16 Determine v_o versus v_i for the circuit shown in Figure 7.87. Assume that the MOSFET operates in saturation and is characterized by the parameters K and V_T . What is the value of v_o when $v_i=0$?

problem 7.17 Determine v_o versus v_i for the circuit shown in Figure 7.88. Assume that the MOSFET operates in saturation and is characterized by the parameters K and V_T .

problem 7.18 Consider the BJT circuit called the “common-collector amplifier” shown in Figure 7.89. This BJT amplifier configuration is also called the source follower circuit. For this problem, use the piecewise-linear BJT model from Exercise 7.8. Assume that the BJT operates in its active region.

a) Draw the active-region equivalent circuit of the BJT source follower by replacing the BJT by its piecewise-linear model.

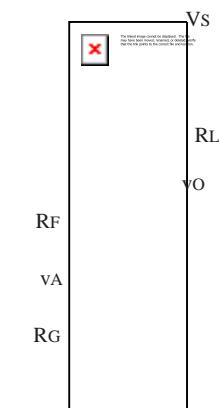


FIGURE 7.84

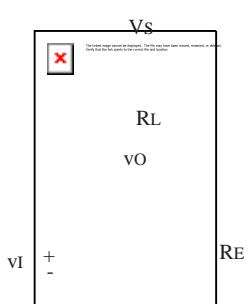


FIGURE 7.85

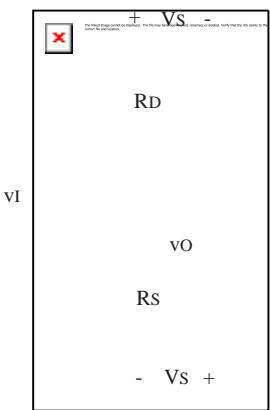


FIGURE 7.86

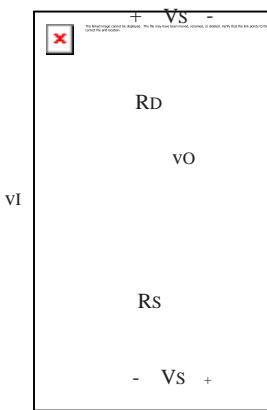


FIGURE 7.87

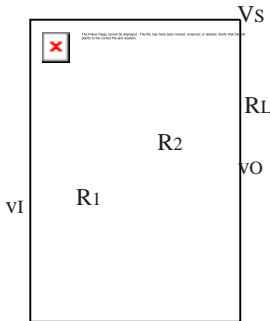


FIGURE 7.88

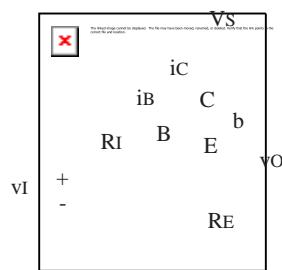


FIGURE 7.89

- b) Assuming active region operation, determine v_o in terms of v_i , R_1 , R_E , and the BJT parameter β .
- c) What is the value of v_o when $\beta R_E \gg R_I$?
- d) Compute the value of v_o given that $v_i = 3V$, $R_I = 10k\Omega$, $R_E = 100k\Omega$, $\beta = 100$, and $V_S = 10V$.
- e) Determine the range of values of v_i for which the BJT operates in its active region for the parameter values given in (d). What is the corresponding range of v_o ?

problem 7.19 Consider the compound three-terminal device formed by connecting two BJTs in the configurations shown in Figure 7.90. The three terminals are

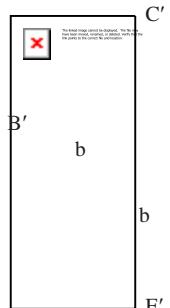


FIGURE 7.90

labeled C, B, and E. The two BJTs are identical, each with $\beta = 100$. Assume that each of the BJTs operates in the active region.

- a) Draw the active-region equivalent circuit of the compound BJT by replacing each of the BJTs by the piecewise-linear model shown in Exercise 7.8. Clearly label the C, B, and E terminals.
- b) In the configuration shown, the compound device behaves like a BJT. Determine the value of the current gain β for this compound BJT.
- c) When the base current $i_B > 0$, determine the voltage between the B and E terminals.

chapter 8

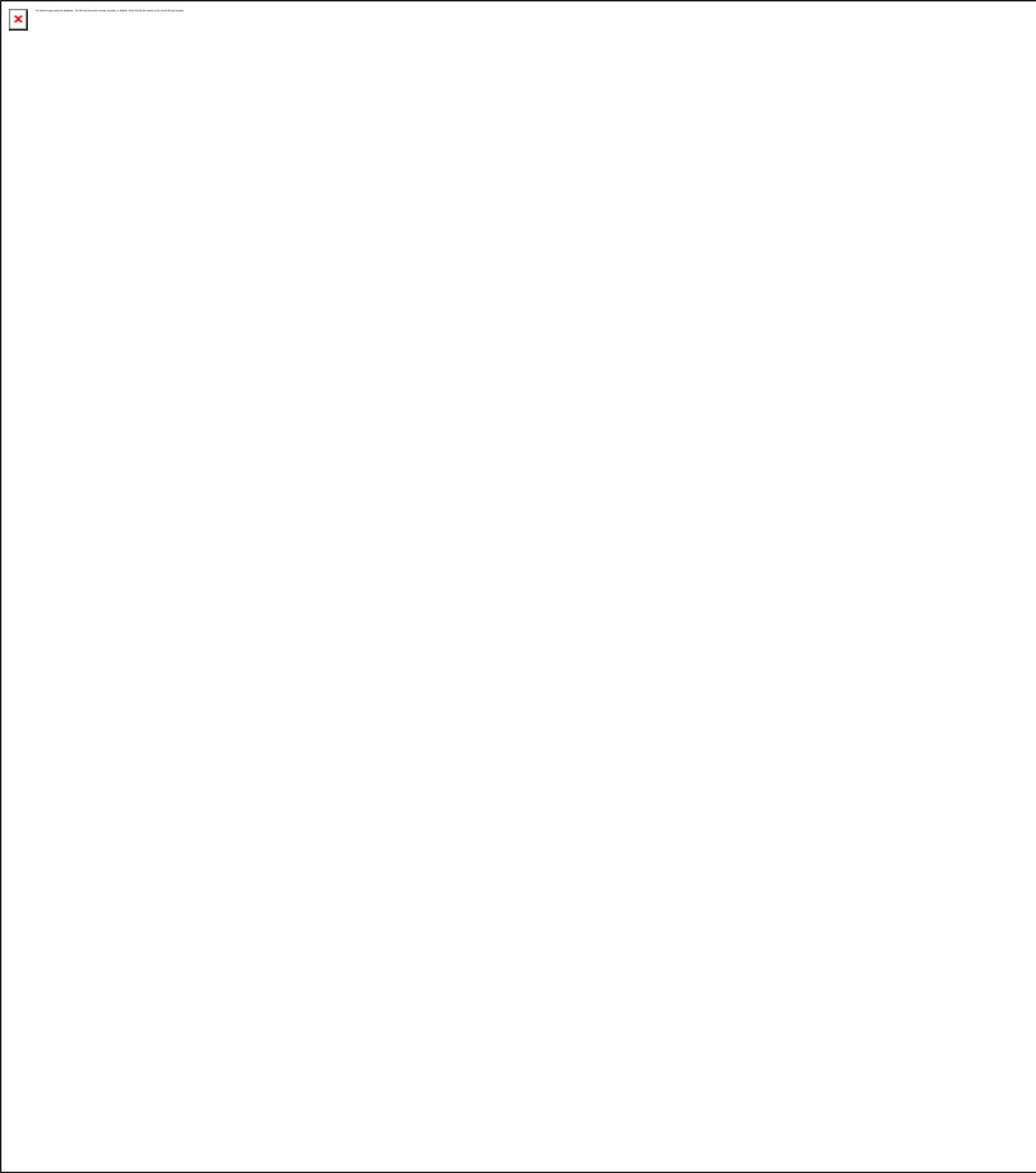
8.1 OVERVIEW OF THE NONLINEAR MOSFET AMPLIFIER

8.2 THE SMALL-SIGNAL MODE

8.3 SUMMARY

EXERCISES

PROBLEMS



8

the small-signal model

8.1 OVERVIEW OF THE NONLINEAR MOSFET AMPLIFIER

An unfortunate feature of the MOSFET amplifier discussed in Chapter 7 was its nonlinear input-output relationship. Shown in Figure 8.1, the MOSFET amplifier has the following input-output relationship:

$$v_o = V_s - i_D R_L \quad (8.1)$$

Substituting for the current i_D in terms of the MOSFET input voltage under the saturation discipline, we get the following nonlinear relationship between v_i and v_o :

$$v_o = V_s - K(v_i - V_T)^2 R_L \quad (8.2)$$

The nonlinear relationship between the input and the output voltage is plotted in Figure 8.2. The nonlinear relationship makes it difficult for us to analyze and to build circuits using the amplifier.

8.2 THE SMALL-SIGNAL MODEL

In many circuit applications, such as audio amplifiers, demand a linear amplifier of the form depicted in Figure 8.3. The amplifier shown in the figure has a constant gain A that is independent of the input voltage. Does that mean we cannot use the MOSFET amplifier in these linear applications? It turns out that total variables representing signalssuch as those input to an audio amplifier commonly consist of two components: a DC offset (or an average value), plus a time-varying component with a zero average. We will show that if the time-varying component is small, then the incremental amplification provided by the MOSFET amplifier to the time-varying component about the operating point defined by the input DC offset will be approximately linear. As we saw in Section 4.5, this observation actually generalizes to arbitrary nonlinear circuits: The response of a circuit to small perturbations about an operating point will be linear. Thus, if the signals of interest to us can be represented as small perturbations about an operating point, then the response of arbitrary nonlinear

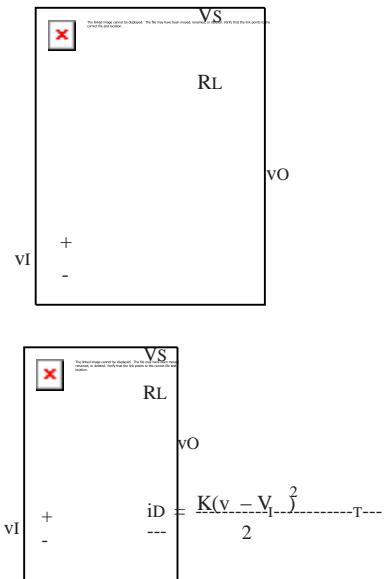


FIGURE 8.1 The MOSFET amplifier and its SCS circuit model.

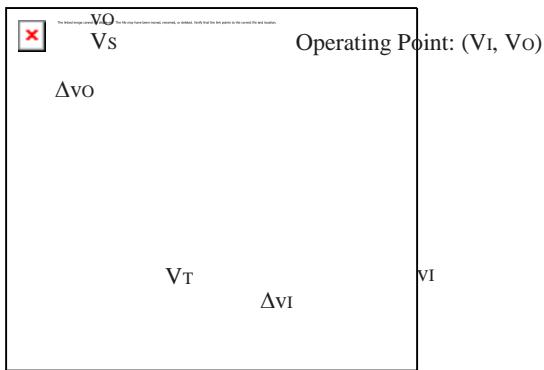


FIGURE 8.2 v_o v_I

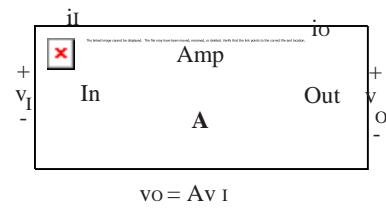


FIGURE 8.3 A

small-signal discipline.

$$v_I = V_I + v_i$$

$$v_o = A v_I$$

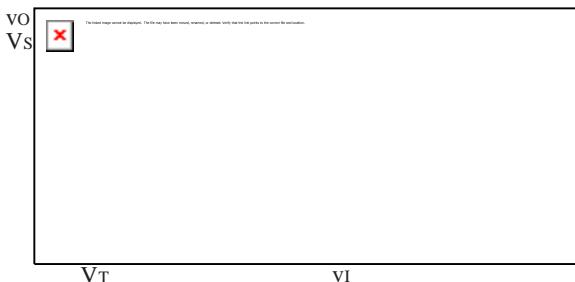


FIGURE 8.4 A small segment of the V_O versus V_I curve.

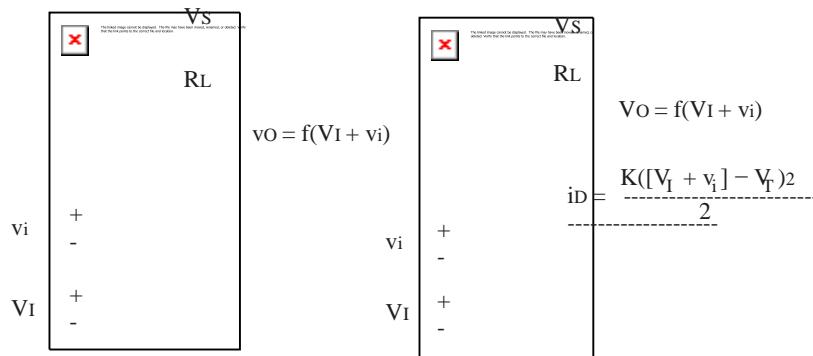


FIGURE 8.5 Superimposing a small (possibly time-varying) signal on the DC bias voltage at the input of the MOSFET amplifier, and the corresponding SC circuit model for the combined input signal.

Let us revisit the transfer curve of the amplifier shown in Figure 8.2. Consider a very small region of the transfer curve in the vicinity of the operating point (V_I, V_O) . The slope of the curve segment is depicted in the figure. As illustrated in Figure 8.4, if we focus our attention on the small curve segment shown, it looks more or less linear. We will use this intuition to develop an abstraction for amplifiers that appears linear for very small variations in the input voltage.

The basic idea is that the amplifier transfer function appears linear for small perturbations in the input voltage about a given bias point. We can arrive at the same result analytically. Suppose that the amplifier is biased at some bias point: (V_I, V_O) . Now suppose that we superimpose a small signal $v_I = v_{in} V_{bias}$ depicted in Figure 8.5. An example of a DC signal with a small superimposed time-varying signal is shown in Figure 8.6.

We know from the SC model of the MOSFET (see Equation 7.8) that the current through the MOSFET is related to its gate voltage as:

$$i_{DS} = \frac{K(v_{GS} - V_f)}{2} \quad (8.3)$$

FIGURE 8.6 A small time-varying signal combined with a DC offset voltage.

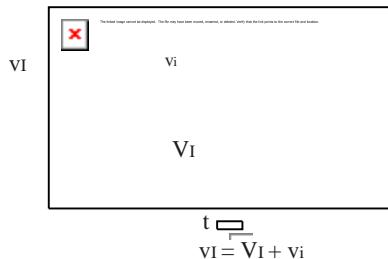
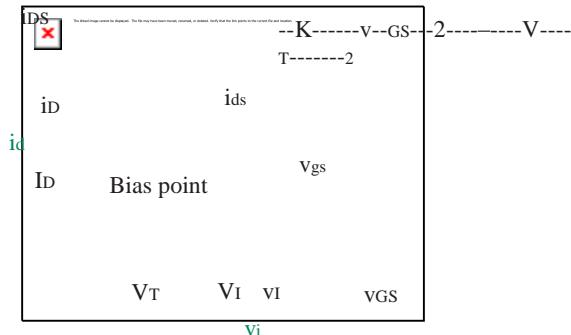


FIGURE 8.7 Output current for the MOSFET for the combined input voltage.



For the combined input signal shown in Figure 8.5, the response current i_d through the MOSFET is the sum of two components: a bias current I_D and a change due to the incremental input signal v_i . As depicted in Figure 8.7, this combined current can be obtained by substituting for V_{GS} as

$$\frac{K(V_I - v_i)}{2} \cdot V_T^2. \quad (8.4)$$

Since we know that v_i is small compared to V_t , we can adopt the following linearization technique to obtain the combined response: Model the MOSFET characteristic curve accurately only in the vicinity of the bias point V_t and disregard the rest of the curve. The Taylor series expansion is the natural tool for this task.

x The Taylor series expansion for the function $y = f(x)$ in the vicinity of x_0 is given by:

$$y \quad f(x) \quad f(X_0) \quad \frac{d}{dx} \Big|_{X_0} (x - X_0) \quad \frac{1}{2} \frac{d^2f}{dx^2} \Big|_{X_0} (x - X_0)^2$$

Our goal is to use the Taylor series method to expand the MOSFET SCS equation for the combined input voltage given in Equation 8.4 about the bias voltage V_I . For our Taylor expansion, V_I corresponds to X_0 , x corresponds to $V_I + v_i$, or $x - X_0$ corresponds to v_i , and y corresponds to $i_D = I_D + i_d$. Applying the Taylor expansion to Equation 8.4 about V_I we get

$$i_D = f(V_I + v_i) = \frac{K[(V_I + v_i) - V_T]^2}{2} \quad (8.5)$$

$$= \frac{K(V_I - V_T)^2}{2} + K(V_I - V_T)v_i + v \frac{K^2}{2} v_i^2 \quad (8.6)$$

If the incremental signal v_i is small enough to permit us to ignore the second order term (and higher terms, when they exist) in the Taylor series expansion, the following simplification results:

$$i_D \approx \frac{K(V_I - V_T)^2}{2} + K(V_I - V_T)v_i. \quad (8.7)$$

We know that the output current is composed of a DC component I_D and a small perturbation i_d . Thus, we can write

$$I_D + i_d = \frac{K(V_I - V_T)^2}{2} + K(V_I - V_T)v_i. \quad (8.8)$$

Equating DC terms and corresponding incremental terms:

$$I_D = \frac{K(V_I - V_T)^2}{2} \quad (8.9)$$

$$i_d = K(V_I - V_T)v_i. \quad (8.10)$$

Note that I_D is simply the DC bias current related to the DC input voltage V_I . Accordingly, the DC terms relating I_D to V_I can be equated as in Equation 8.9 because the operating point values I_D, V_I satisfy Equation 8.3, which is the MOSFET equation. When the DC terms are eliminated from both sides of Equation 8.8, the incremental relationship shown in Equation 8.10 results.

Notice that the change in the output current i is linearly related to the change in the input voltage v_i provided that v_i is small compared to V_I . We note that Equation 8.9 is exact because the small-signal model goes through the exact model at the operating point. However, Equation 8.10 is approximate because of the linearization.

A graphical interpretation of this result provides additional intuition. As shown in Figure 8.8, Equation 8.8 is a straight line passing through the DC operating point V_I, I_D and tangent to the curve at that point. Using the tangent

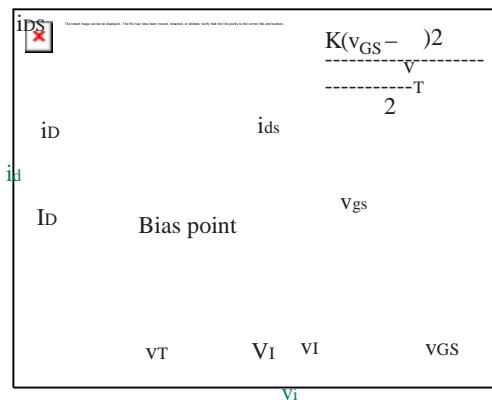


FIGURE 8.8 Incremental change in the output current for the MOSFET for a small change in the input voltage.

To compute the incremental change in the signal about the operating point is tantamount to replacing the actual curve with the tangent. Clearly, the tangent approximation is valid only for points that are close to the operating point. The higher-order term in Equation 8.6 that we neglected would add a quadratic term to the model, thereby making the fit exact for our model.

Let us return to the relationship between the incremental output current and the incremental input voltage for the MOSFET:

$$id = K(VI - VT)vi \quad (8.11)$$

The $K(VI - VT)$ term in Equation 8.11 relates the input voltage to the current through the MOSFET. Notice that for a given DC bias, the $K(VI - VT)$ term is a constant. Since the form of Equation 8.11 is similar to that for a conductance, the $K(VI - VT)$ term is called the incremental transconductance g_m of the MOSFET. Accordingly, we can write

$$id = g_m vi \quad (8.12)$$

where

$$g_m = K(VGS - VT). \quad (8.13)$$

In our example, $VGS = VI$.

Returning to our amplifier, we can express the total output voltage v_o as the sum of the output operating voltage V_o and the incremental change vi as

$$v_o = V_o + vi.$$

From Equation 8.1 we know that

$$v_o = V_s - i_D R_L. \quad (8.14)$$

Replacing v_o and i_D with their corresponding DC and incremental components,

$$V_o + v_o = V_s - (I_D + i_d) R_L \quad (8.15)$$

$$= V_s - I_D R_L - i_d R_L. \quad (8.16)$$

Therefore,

$$V_o = V_s - I_D R_L \quad (8.17)$$

$$v_o = -i_d R_L \quad (8.18)$$

$$= -g_m v_i R_L. \quad (8.19)$$

In other words,

$$\frac{V}{\text{Small signal gain}} = \frac{v_i}{-g_m R_L} = A. \quad (8.20)$$

Notice from Equation 8.20 that the small signal gain is a constant $-g_m R_L$. Note, however, that g_m , and therefore the gain, depends on the choice of bias point for the amplifier. Equation 8.19 demonstrates that for small excursions from a DC operating point, a linear amplifier results! This result forms the basis of the small-signal model.

We can directly arrive at the small signal response — be it voltage or current — using basic calculus for circuit responses that are differentiable, which basically includes all physically realizable analog circuits. Recall that the derivative of a function $y = f(x)$ at the point x is the slope of the function at that point, or $f'(x)$. As depicted in Figure 8.9, given a small change from the

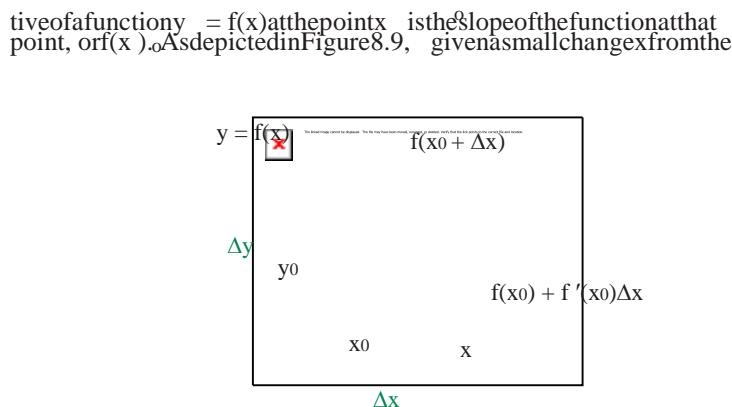


FIGURE 8.9 Incremental response.

point x_0 , we can compute the response to the change as the product of the slope at that point and x . In other words,

$$f(x_0 + x) = f(x_0) + \frac{dx}{dx} \Big|_{x_0} x.$$

Thus the incremental change in the output is given by

$$\underline{y} = \frac{\underline{x}}{\frac{dy}{dx} \Big|_{x_0}} \quad (8.21)$$

In particular, we can obtain the incremental voltage gain directly from the voltage transfer function, without first determining the incremental output current. The input-output voltage relationship for the MOSFET amplifier is given by

$$v_o = f(v_i)$$

$$= V_s \frac{K(v_i - V_T) 2 R_L}{2}$$

As before, let $v_i = v$ denote a small change in the input voltage, and let $v_o = v$ denote the corresponding change in the output voltage. Then,

$$\begin{aligned} v_o &= \frac{\underline{v}_i}{df(\underline{v}_i) \Big|_{v_i=v_i}} \\ &= \frac{\underline{v}_i}{-K(v_i - V_T) R_L} \\ &= -K(V_i - V_T) R_L^T \\ &= -g_m R_L v_i. \end{aligned}$$

Not surprisingly, this result is the same as the one we obtained earlier.

To summarize, the small-signal model is a statement of a particular type of linearized analysis of our circuits, which applies when the desired circuit responds to signals that can be represented as an incremental perturbation over a DC operating value. Put another way, it is a statement of a particular type of constraint on our use of circuits called the small-signal discipline that allows us to obtain linear behavior from nonlinear circuits over small ranges of operation.

Small signal model The responses of circuits to incremental changes from a known DC operating point will be linear about a good approximation.

A systematic procedure for finding incremental signal responses based on the preceding discussion involves two steps:

1. Find the DC operating point of the circuit using DC values and the complete characteristics of the devices. Determine the corresponding large-signal response (possibly nonlinear) to the desired input.
2. Apply the Taylor expansion method to the large-signal response to derive the small-signal response. Alternatively, as discussed in Section 8.2.1, replace the large-signal circuit with its equivalent small-signal model based on the Taylor expansion and obtain the small-signal response.

Small-signal analysis is an extremely useful technique that applies to all physical systems with differentiable characteristics. In essence, it says that if we operate within a small-signal discipline, the response of any physical system to small perturbation will be linear! In turn, the effectively linear system is amenable to linear analysis techniques, such as superposition.

For example, consider a two-terminal sensor S that behaves like a temperature-dependent voltage source with the following nonlinear relationship between its terminal voltage v_s and its temperature t_s :

$$v_s = Bt^3$$

where B is some constant. If the ambient temperature is T_s and the corresponding voltage is V_s , we can relate the incremental change in the terminal voltage Δv_s to an incremental change in the temperature Δt_s using Equation 8.21 as follows:

$$\Delta v_s = B \left(t_s^3 - T_s^3 \right)$$

In other words,

$$\frac{\Delta v_s}{\Delta t_s} = B t_s^2$$

When operating at a given ambient temperature, $3BT^2$ is a constant. Therefore, the voltage response of the sensor to small changes in the temperature around an ambient will be linear.

8.2.1 SMALL-SIGNAL CIRCUIT REPRESENTATION

A model that involves only the small-signal variables of a circuit, and hence describes purely the small-signal behavior of that circuit, would greatly facilitate small-signal analysis. Fortunately, such a small-signal model is relatively straight-

forward to develop by executing the following procedure:

1. Set each source to its operating-point value, and determine the operating-point branch voltages and currents for each component in the circuit. This is most likely the longest step in the procedure.
2. Linearize the behavior of each circuit component about its operating point. That is, determine the linearized small-signal behavior of each component, and select a linear component to represent this behavior.
The parameters of the small-signal components will commonly depend on the operating-point voltages or currents.
3. Replace each original component in the circuit with its linearized equivalent and re-label the circuit with the small-signal branch variables. The resulting circuit is the desired small-signal model.

The circuit that is generated by this procedure is the desired small-signal circuit model, and is analogous to equating the small signal terms on both sides of Equation 8.8 yielding the equalities in Equation 8.10. Further, it is a linear circuit, and hence the analysis tools developed for linear circuits, such as superposition and the Thévenin equivalent model, may be applied to its analysis.

At this point, it is worth discussing why the procedure works. To begin, recognize that the operation of a circuit is described in total by two sets of equations: the circuit connection law of KV L and KCL, and the constitutive laws that describe the behavior of the individual circuit components. With this recognition, the small-signal analysis of a circuit may also be described by the following more direct mathematical procedure:

1. Set each source to its operating-point value, and combine the equations to determine the operating point of the circuit. This is essentially the same step as in the previous procedure.
2. Return to the original set of equations. For each variable in every equation, substitute for the total variable the sum of its operating-point value and its small-signal value. Then, linearize the equations around the operating point assuming that the small-signal terms are small.
3. Cancel the operating-point variables from the linearized equations to yield a set of linear equations that relate the small signals to themselves. This cancellation must always be possible since the linearization is defined to pass through the operating-point. This cancellation is akin to separately equating the operating-point variables and the incremental variables as we did in Equation 8.10.1

1. In other words, we start with a set of equalities defining the operating point using operating-point variables, for example,

4. Complete the small-signal analysis by combining the linearized equations to determine the desired small-signal variables in terms of the small-signal inputs at the sources.

Now, let us examine the last procedure more closely. Notice that in Step 2 it is actually necessary to linearize only the constitutive laws that describe the behavior of the individual circuit components because KVL and KCL are already linear equations. It is for this reason that the first procedure called for the linearization of only the constitutive laws. Further, because KVL and KCL constitute a linear set of equations, they are unchanged by the linearization step. This is important to recognize because KVL and KCL contain the information concerning the topology of the original circuit. That is, they state which branches are connected to which nodes, and which branches connect to form which loops. Since KVL and KCL are unaffected by the linearization step, the topological information is preserved during linearization. It is for this reason that the small-signal circuit model has the same topology as the original circuit. Thus, the linearized set of equations describing the behavior of the small-signal circuit variables that is generated by the more formal mathematical procedure comprises the original KVL and KCL equations, and linearized component constitutive laws. Thus, to develop a small-signal circuit model it is necessary to determine only equivalent linearized circuit components and substitute them into the circuit in place of their corresponding original circuit components.

Small-signal circuit models for various devices are summarized in Figure 8.10.

The small-signal equivalent model for an independent DC voltage source is a short circuit because its output voltage does not change for any perturbation of the current through it. In particular, the power supply connection labeled V_s in most of our circuits gets shorted to ground in the incremental circuit.

The small-signal model for an independent DC current source is an open circuit.

We then linearize, and obtain a new set of equalities in operating-point variables and incremental variables, for example,

$$V_O + v_o = A_V I + A_v i.$$

The equalities that define the operating point in the first place (namely, $V_O = A_V I$ in our example) may always be cancelled out of the linearized equation since they are only additively connected to the small-signal variables. For our example, we thus obtain

$$v_o = A_v i.$$

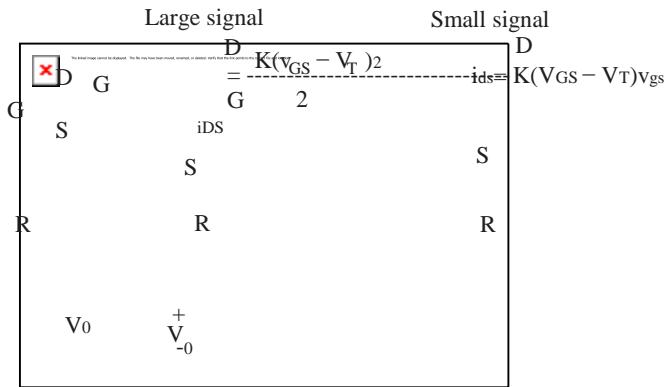
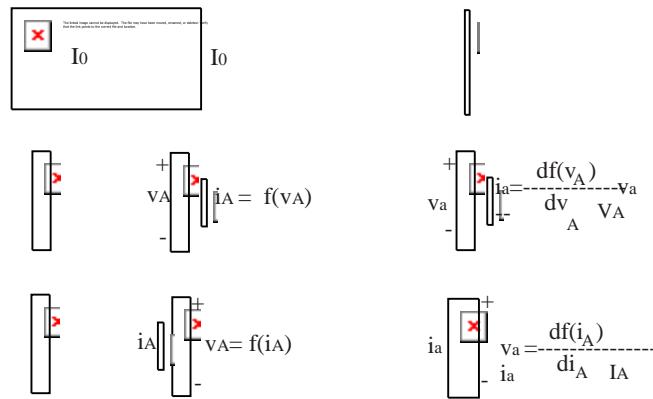


FIGURE 8.10 Small-signal equivalent models.



A resistor behaves identically for a large signal or a small signal. Therefore its small-signal and large-signal models are the same.

For a MOSFET, the derivation resulting in Equation 8.11 shows how to relate the incremental drain-to-source current to the incremental gate-to-source voltage v_{gs} .

By definition, an input signal v_i has an incremental component v_i and a DC component V_i .

In general, if a device variable x_B depends on some other variables x_A as

$$x_B = f(x_A),$$

then the incremental change in x_B due to a small change in x_A is given by

$$\Delta x_B = \frac{df(x_A)}{dx_A} \Delta x_A \quad \text{at } x_A = X_A \quad (8.22)$$

where X_A is the operating point value of x_A .

example 8.1 a mosfet with its gate and drain tied together Let us derive the incremental model for a MOSFET that has its gate and drain terminals tied together as shown in Figure 8.11. When the G and D terminals of the MOSFET are tied together, we get an effective two-terminal device. Let us denote the two terminals as D and S, respectively. Because the gate-to-source voltage of the device is the same as the drain-to-source voltage, the current i_{DS} through the device is related to the voltage v_{DS} across the device as

$$i_{DS} = K(v_{GS} - 2V_T)_2.$$

Since the gate and drain are connected, $v_{GS} = v_{DS}$. Therefore,

$$i_{DS} = K(v_{DS} - V_T)_2.$$

The large-signal model for the mosfet is shown in Figure 8.12.

We can derive the change in i_{DS} for a small change in v_{DS} as follows. Let the DC value of v_{DS} be V_{DS} and let the change be denoted v_{DS} . Let the corresponding DC value of i_{DS} be I_{DS} and let its change be denoted i_{DS} . Then,

$$i_{DS} = \frac{di_{DS}}{dv_{DS}} v_{DS}$$

$$= K(v_{DS} - V_T) \frac{v_{DS}}{v_{DS}} ds$$

$$= K(V_{DS} - V) \frac{v_{DS}}{V_{DS}} ds.$$

In other words,

$$v_{DS} = K \frac{i_{DS}}{V_{DS} - V_T}.$$

Notice that because $1/K(V_{GS} - V_T)$ is a constant, v_{DS} is directly proportional to i_{DS} , which is a resistor relationship. Remarkably, a MOSFET with its gate and drain terminals connected behaves like a resistor with resistance $1/K(V_{GS} - V_T)$ to small signals. The small-signal equivalent circuit for the preceding element is shown in Figure 8.13. Because of its resistive behavior for small signals, and because MOSFETs with a high resistance are easier to fabricate than resistors, MOSFETs are commonly used as the load resistor in amplifiers.

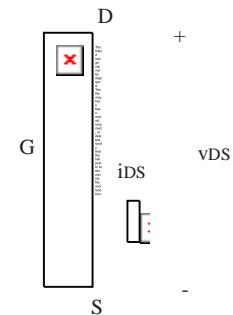


FIGURE 8.11 MOSFET with its G and D terminals connected together.

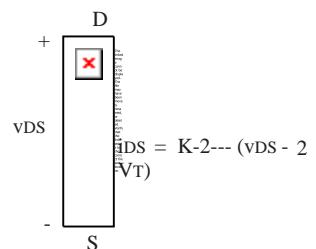


FIGURE 8.12 Large-signal model for a MOSFET with its G and D terminals connected together.

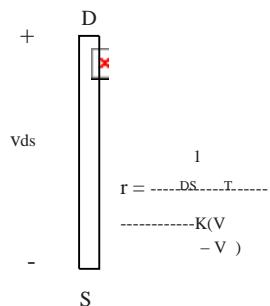


FIGURE 8.13 Small-signal model for a MOSFET with its G and D terminals connected together.

8.2.2 SMALL-SIGNAL CIRCUIT FOR THE MOSFET AMPLIFIER

Let us now develop the small-signal equivalent circuit for the MOS amplifier shown in Figure 8.14. Recall that developing the small-signal model involves the following steps:

1. Set each source to its operating-point value, and determine the operating-point branch voltages and currents for each component in the circuit.
2. Determine the linearized small-signal behavior of each component, and select a linear component to represent this behavior.
3. Replace each original component in the circuit with its linearized equivalent and re-label the circuit with the small-signal branch variables. The resulting circuit is the desired small-signal model.

As the first step, let us determine the operating point of the MOSFET amplifier for its bias voltages using the large-signal SCS circuit model depicted in Figure 8.15. Assuming that the input bias voltage is V_I , we can determine the output operating current I_D and the output operating voltage V_O . We explicitly show the power-supply voltages source V_S to facilitate deriving the small-signal model.

FIGURE 8.14 The MOSFET amplifier.

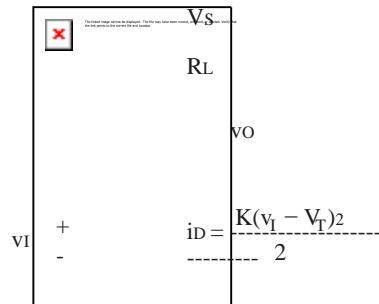
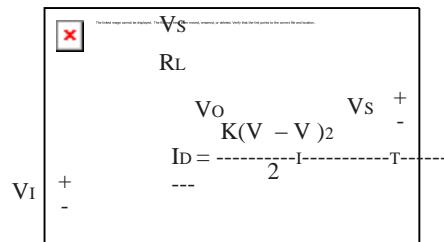


FIGURE 8.15 Computing the operating point of the MOSFET amplifier based on the large-signal SCS model.



The output operating current I_D is directly calculated from the MOSFET characteristic equations:

$$I_D = K_2(V_i - V_T)^2.$$

The output operating voltage is obtained by applying KVL for the loop comprising the power supply, the MOSFET, and R_L as follows:

$$V_o = V_s - I_D R_L \quad (8.23)$$

$$= V_s - K_2(V_i - V_T)^2 R_L. \quad (8.24)$$

At the second step, we determine the linearized small-signal models for each component. Referring to Figure 8.10, we see that the small-signal model for the DC power supply is a short. The small-signal model for the resistor is the same as its large-signal model. Finally, the linearized small-signal model for the MOSFET in saturation is a voltage-dependent current source whose small-signal current is linearly related to the small-signal gate-to-source voltage as:

$$i_{ds} = K(V_{GS} - V_T)v_{gs}.$$

Notice that the biasing of the large-signal circuit determines the parameters of the small-signal circuit (for example, the small-signal current source parameter $K(V_i - V_T)$ depends on the input bias voltage, V_i).

At the third step, we replace each original component in the circuit with its linearized equivalent and re-label the circuit with the small-signal branch variables v_i , v_o , and i_d as depicted in Figure 8.16.

The small-signal circuit model can be analyzed to determine the circuit responses to small signals. For example, we can use Figure 8.16 to determine the small-signal gain of the MOSFET amplifier. Applying KVL at the output, we get

$$v_o = -i_d R_L \quad (8.25)$$

$$= -K(V_i - V_T)v_i R_L \quad (8.26)$$

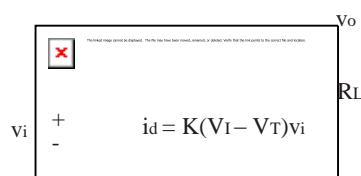


FIGURE 8.16 The small-signal SC circuit model for the MOSFET amplifier.

Thus, the small-signal gain is given by

$$\frac{V_o}{V_i} = -K(V_I - V_T)R_L \quad (8.27)$$

$$= -g_m R_L \quad (8.28)$$

where

$$g_m = K(V_{GS} - V_T) \quad (8.29)$$

K is the transconductance of the MOSFET.

As an example, let us compute the small-signal gain for the following amplifier parameters:

$$V_S = 10V$$

$$K = 1mA/V^2$$

$$R_L = 10k$$

$$V_T = 1V.$$

Also, suppose the input bias voltage is chosen to be $V_I = 2V$. As determined earlier in Equation 8.24,

$$V_o = V_S - K^2(V_I - V_T)^2 R_L.$$

Substituting the given parameters, we get $V_o = 5V$. We can now calculate the magnitude of the voltage gain as

$$\frac{V_o}{V_i} = K(V_I - V_T)R_L$$

$$= 10^{-3}(V_I - 1)10^4$$

$$= 10.$$

8.2.3 SELECTING AN OPERATING POINT

Small-signal operation requires that the total input signal appear as a small perturbation about a DC offset. The input DC offset establishes an operating point for the amplifier. Section 7.7 discussed the issue of operating points in the context of large signals, and proposed a method for selecting the operating point based on maximizing the dynamic input signal range. Specifically, Section 7.7 suggested that the operating point be chosen at the midpoint of the valid input voltage range of amplifier operation under the saturation discipline. This made

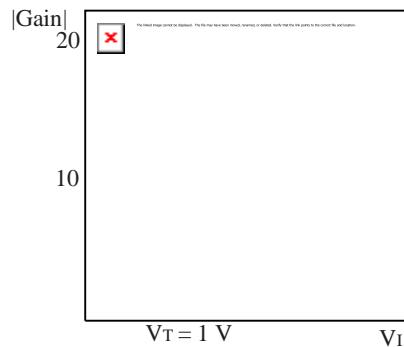


FIGURE 8.17 Magnitude of the small-signal gain of the amplifier for various values of the input operating point voltage V_I .

sense, since the input signals were large and maximizing the input dynamic range enabled the amplifier to deal with the largest possible input signals.

When dealing with small signals, other criteria are often more important in selecting the operating point than just obtaining maximum dynamic range. One criterion is the small-signal gain of the amplifier. As evident from Equation 8.28, the small-signal gain of the amplifier is dependent on the input operating point voltage V_I . The magnitude of the small-signal gain is given by

$$\frac{V_o}{V_i} = K(V_I - V_T)R_L \quad (8.30)$$

Figure 8.17 plots the magnitude of the gain for various values of V_I . The graph indicates that the amplifier gain increases with increasing V_I .

As an example, assuming these parameters for our amplifier,

$$V_s = 10V$$

$$K = 1mA/V^2$$

$$R_L = 10k$$

$$V_T = 1V$$

let us determine a value for the input operating-point voltage V_I that will result in a gain of 12.

Substituting the required gain into Equation 8.30, we have

$$12 = 1 \times 10^{-3}(V_I - 1)10 \times 10^3.$$

Solving, we obtain $V_I = 2.2V$. This means that an input DC offset of 2.2V will result in a small-signal gain magnitude of 12.

Now, assuming that the input signal is a small-signal sinusoid superimposed on the DC offset of 2.2 V, let us determine the maximum valid peak-to-peak swing for the sinusoid. We refer back to Section 7.6.2 to answer this question. From Section 7.6.2, we know that under the saturation discipline, the maximum valid range for the input voltage is $V_T \rightarrow -1 + \sqrt{V_S R_L K / R_L K + V_T}$.

For the given parameters, the valid range for input voltages is $1 \text{ V} \rightarrow 2.32 \text{ V}$. In other words, as discussed in Section 7.6.2, input voltages under 1 V will result in cutoff region operation of the MOSFET, while those over 2.32 V will result in triode region operation. Operation in either the cutoff region or the triode region will result in severe signal distortion.

Since the input offset is 2.2 V, and the maximum valid input voltage is 2.32 V, the maximum positive swing for saturation region operation of the MOSFET is given by $2.32 \text{ V} - 2.2 \text{ V} = 0.12 \text{ V}$. Thus, the maximum peak-to-peak swing for the input sinusoid is $2 \times 0.12 \text{ V} = 0.24 \text{ V}$. Notice the clear tradeoff we have made between gain and dynamic range. To increase the gain, we had to bias the amplifier with a high input bias voltage, which was close to the high end of the valid input signal range. However, the high input bias voltage limited the positive signal swing.

Another criterion that is often important is the output operating-point voltage. This is important when the amplifier must drive another circuit stage and the output operating-point voltage of the amplifier determines the input operating-point voltage of the next stage.

For example, consider the two-stage amplifier shown in Figure 8.18. In this circuit, V_{IA} provides the DC bias for the first stage. Its output, in turn, V_{OA} provides the DC bias for the second stage. Thus, $V_{OA} = V_{IB}$.

Assuming the following parameters for our amplifier,

$$V_S = 10 \text{ V}$$

$$K = 1 \text{ mA/V}_2$$

$$R = 10 \text{ k}\Omega$$

$$V_T = 1 \text{ V}$$

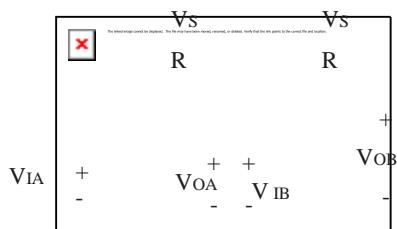


FIGURE 8.18 A two-stage amplifier.

suppose the first stage is biased at $V_{IA} = 2.2\text{V}$ to achieve a small-signal gain magnitude of 12. Let us determine whether the output operating-point voltage of the first stage can provide a valid input bias voltage for the second stage. When the first stage is biased at V_{IA} , V_{OA} is given by Equation 8.24. 2.2V. Substituting the first stage the operating-point parameters for

$$\begin{aligned} V_{OA} &= V_S - \frac{K}{2(V_{IA} - V_T)2R} \\ &= 10 - \frac{1 \times 10^{-3}}{2(2.2 - 1)210 \times 10^3} \\ &= 2.8\text{V}. \end{aligned}$$

From Section 7.6.2, we know that under the saturation discipline, the maximum valid range for the input voltage of the second stage is $V_T \rightarrow -1 +$

$\sqrt{1+2V_{OA}} \frac{R_K}{R_K+V_T}$. Substituting the circuit parameters, the valid input range for the second stage comes out to be $1\text{V} \rightarrow 2.32\text{V}$. Since V_{OA} exceeds the upper bound ($2.8\text{V} > 2.32\text{V}$), we conclude that the first stage cannot provide a valid input bias voltage for the second stage when the first stage input bias is set at 2.2V. We can correct this situation by increasing V_{IA} , or by increasing R for the first stage.

8.2.4 INPUT AND OUTPUT RESISTANCE, CURRENT AND POWER GAIN

The small-signal equivalent circuit also allows us to determine other important circuit parameters, such as the small-signal input resistance, output resistance, current gain, and power gain. Since the amplifier behaves as a linear network for small signals, it can be characterized by a Thévenin equivalent when viewed from any given port. The input and output resistance come in handy in this Thévenin characterization. Let us determine these values for the MOSFET amplifier using its small-signal circuit in Figure 8.16. Since these parameters are externally observed quantities, they are defined with respect to the external ports of the amplifier abstraction. Thus, it is important that we define precisely what constitutes the input and output ports of the small-signal amplifier. Figure 8.19 shows the relationship between the external ports of the amplifier circuit and the small-signal model. Notice that we have internalized the input bias voltage into the small-signal amplifier abstraction so the user of the amplifier does not have to provide the appropriate input bias voltage. Instead, the user can simply provide a small input signal and observe the resulting signal output superimposed on the DC output offset.

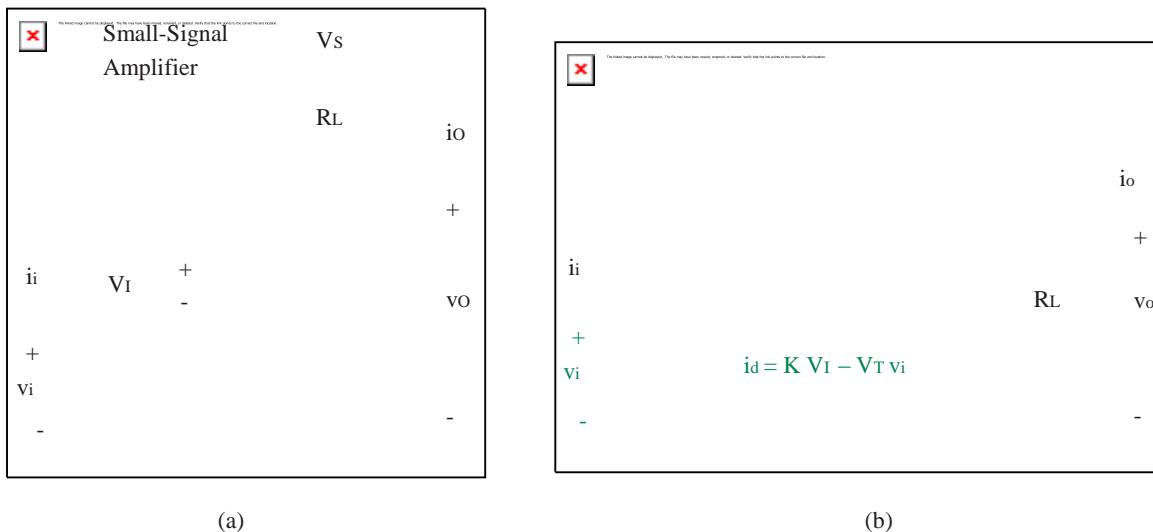


FIGURE 8.19 Amplifier input and output ports: (a) amplifier circuit; (b) small-signal model. As shown in the amplifier circuit, we have internalized the input bias voltage into the small-signal amplifier abstraction.

InputResistanceri

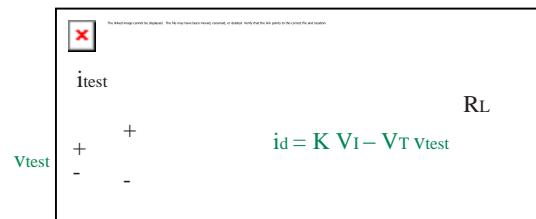
Incremental input resistance The change in the input current for a small change in the input voltage.

Accordingly, as depicted in Figure 8.20 we compute it by applying a small test voltage v_{t3} at the input and measuring the corresponding current i_{t3} . All other independent small-signal voltages or DC voltages sources are shorted. Similarly, all other independent small-signal or DC current sources are returned to open circuits.

The input resistance for the MOSFET amplifier is given by

$$r_i = i \frac{V_{\text{test}}}{V_{\text{test}}} = \frac{V_{\text{test}}}{0} = \infty. \quad (8.31)$$

FIGURE 8.20 Inputresistance measurement



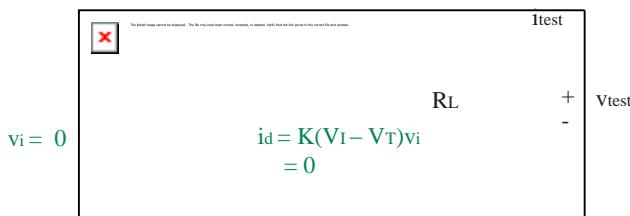


FIGURE 8.21 Outputresistance measurement.

For the SCSMOSFET model, the gate does not draw any current ($i_{test} = 0$), so the input resistance is infinite.

Output Resistance r_{out}

Incremental output resistance The change in the output current for a small change in the output voltage.

We must assume, of course, that the circuit is biased properly. As depicted in Figure 8.21, we compute the output resistance by applying a small test voltage v_{test} at the output and measuring the corresponding current i . As before, all other independent small-signal voltages or DC voltage sources are shorted. Thus the small-signal input voltage v_i is set to 0. Similarly, all other independent small-signal or DC current sources are returned to open circuits.

The output resistance is given by

$$r_{out} = \frac{V}{i_{test}} = R_L. \quad (8.32)$$

Because the input small-signal voltage is set to zero, the current through the MOSFET is 0. In other words, the MOSFET behaves like an open circuit. Thus the output resistance for small signals is R_L .

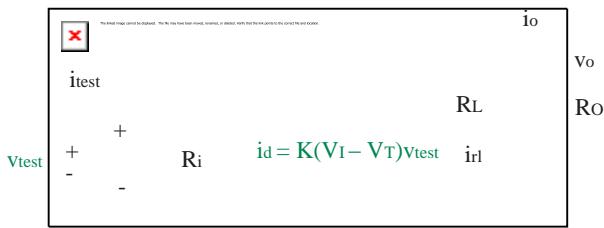
Current Gain

Analogous to the voltage gain, we can define a current gain for an amplifier that supplies an external current.

Incremental current gain The change in the output current divided by the change in the input current, for a given external load resistance.

As depicted in Figure 8.22, we can compute the current gain by applying a small test voltage at the input and measuring both the input current i_{in} and the output current i_o . The ratio i_o/i_{in} is the current gain. Note that the output current is not the current that flows through the dependent current source, rather it is the current that is drawn by an external load resistor R_o . Because it is dependent on the value of the load resistor, the current gain is defined

FIGURE 8.22 Currentgain measurement. As an exercise, we place a resistance R_i between the input terminal and ground. For a MOSFET, $R_i = \infty$.



for a given load resistance. The introduction of an external load resistance also reduces the voltage gain of the amplifier because it appears in parallel with the internal load resistor R_L .

The current gain with an external load resistance R_o is given by

$$\text{Current gain} = \frac{i_{\text{test}}}{i_{\text{test}}} = \frac{V_o}{V_{\text{test}}} \quad (8.33)$$

Let us go through the exercise of determining the value of i_o assuming there is some finite input resistance R_i as shown in Figure 8.22. Substituting for i_o and i_{test} in terms of the respective voltages,

$$\text{Current gain} = \frac{V_o}{V_{\text{test}}} = \frac{R_o}{R_i} \quad (8.34)$$

$$= \frac{V_o}{V_{\text{test}} R_o} \cdot \frac{R_o}{R_i} \quad (8.35)$$

Equation 8.35 says that the current gain is proportional to the product of the voltage gain and the ratio of the input resistance and the output resistance.

We can determine the voltage gain V_o/V_{test} by substituting for V_o in terms of the current i_d and the parallel resistance pair R_L and R_o as

$$\frac{V_o}{V_{\text{test}}} = \frac{i_d}{i_{\text{test}}} = \frac{R_o}{R_i} \quad (8.36)$$

In other words,

$$\frac{V_o}{V_{\text{test}}} = -K(V_i - V_T)(R_L R_o) \quad (8.36)$$

Notice that the voltage gain of the amplifier with an external load is lower than an unloaded amplifier. Substituting the expression for the voltage gain into

Equation 8.35, we get an expression for the current gain:

$$\text{Current gain} = -K(V_i - V_T)(R_L R_o) R_i \quad \text{---} \quad (8.37)$$

Since $R_i = \infty$ for the MOSFET, the corresponding current gain is also infinite.

Power Gain

Incremental power gain The ratio of the power supplied by the amplifier to an external load to that supplied to the amplifier by the input source.

Referring to Figure 8.22, we can compute the power gain as follows: We apply a small test voltage at the input and measure the input current i_{test} . We also measure the corresponding output voltage v_o and output current i_o supplied to the external load resistor. We compute the power supplied by the input source as $v_{\text{test}} i_{\text{test}}$. Similarly, we compute the power supplied to the external load as $v_o i_o$. As we did for the current gain, let us assume that the amplifier has an input resistance R_i . The power gain is given by

$$\text{Power gain} = \frac{v_o i_o}{v_{\text{test}} i_{\text{test}}} = \frac{v_o}{v_{\text{test}}} \frac{i_o}{i_{\text{test}}} \quad \text{---} \quad (8.38)$$

We know both the voltage gain and the current gain from Equations 8.36 and 8.37, respectively. Substituting in the above equation we get,

$$\text{Power gain} = v \frac{v_o}{v_{\text{test}}} \frac{i_o}{i_{\text{test}}} \quad \text{---} \quad (8.39)$$

$$= [-K(V_i - V_T)(R_L R_o)] - K(V_i - V_T)(R_L R_o) \frac{R_i}{R_o} \quad \text{---} \quad (8.40)$$

$$= [K(V_i - V_T)(R_L R_o)] - i \frac{R^2}{R_o} \quad \text{---} \quad (8.41)$$

Since $R_i = \infty$ for the MOSFET amplifier, the power gain is also infinite.

In practical circuits, however, there is always some input resistance, so the power gain is finite.

example 8.2 voltage-controlled current source

Let us perform a small-signal analysis of the voltage-controlled current source circuit shown in Figure 8.23. Referring to Figure 8.23, the current i_o depends on voltage v_i according to

$$i_o = \frac{1}{L(v_i - 1)}$$

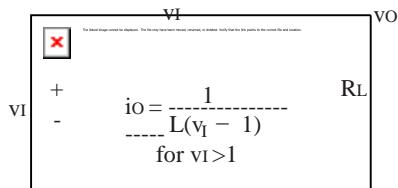


FIGURE 8.23 Dependent current source circuit.

where $V_i > 1$ and L is some constant. What is the change in V_o for an incremental change in V_i , when the operating-point values of V_i and V_o are V_i and V_o , respectively?

To find the incremental change in V_i , we follow the three-step process outlined in Section 8.2.1. We begin by writing the large-signal relationship between V_o and V_i :

$$V_o = i_o R_L \quad (8.42)$$

$$= R_L \frac{1}{L(V_i - 1)} \quad (8.43)$$

Substituting in the operating-point values, we get:

$$V_o = R_L \frac{1}{L(V_i - 1)} \quad (8.44)$$

Next, we linearize the devices. The input voltage source with total voltage V_i is replaced by its small-signal voltage v_i . The resistor remains unchanged. The small-signal equivalent of the dependent current source is derived using:

$$i_o = d\frac{V_i}{V_i} \frac{V_i}{V_i}$$

$$= -\frac{1}{L(V_i - 1)^2} v_i$$

In the third step, we substitute in the small-signal models in place of the large-signal models for each of the devices. The corresponding small-signal circuit is shown in Figure 8.24.

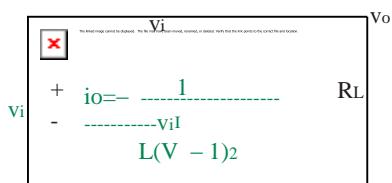


FIGURE 8.24 Small-signal circuit model for the dependent current source.

We can now derive the change in the output voltage for a small change in the input voltage from the small-signal circuit by writing KVL for the output loop:

$$v_o = i_o R_L = -\frac{1}{L(V_i - 1)^2} v_i R_L.$$

We can also derive the change in the output voltage for a small change in the input voltage directly from the v_o versus v_i relationship given by Equation 8.43.

$$v_o = \frac{d v_o}{d v_i} \frac{v_i}{V_i} = -\frac{1}{L(V_i - 1)^2} v_i R_L.$$



example 8.3 small-signal analysis of a difference amplifier The difference amplifier is a building block for high-quality amplification and is useful for processing small signals. When a signal is noisy, straight-forward use of an amplifier would amplify both the signal and the noise. However, under certain conditions that we will see shortly, a difference amplifier (also called a differential amplifier) can be used to amplify the signal by a much larger gain relative to the noise. Difference amplifiers are also used in building operational amplifiers, and suitable difference amplifier circuits are discussed in Examples 7.19 and 8.10.

Suppose the signal is available in differential form. In other words, suppose the signal is available as the relative voltage output ($v_A - v_B$) on a pair of terminals A and B. For example, as the output of the tape-head in a tape-recorder, the output of a instrumentation device or a sensor. Such a sensor often resembles one of four primitive elements for example, a variable resistor. The element might produce a voltage signal across its terminals related to some externally sensed parameter such as temperature, gas concentration, or magnetic field strength. Often, a pair of wires carrying the signal might travel through noisy environments resulting in the coupling of more or less the same amount of noise (v_n) on each of the two wires, as depicted in Figure 8.25.2. In other situations, the two wires might both carry a common DC bias. In such situations, a difference amplifier can help amplify just the differential signal component and discard the common noise component.

The difference amplifier abstraction is shown in Figure 8.26. It is a two-port device with one differential input port and one single-ended output port. The input port has two input terminals. The + input is called the non-inverting input and the - input is called the inverting input. It has an output port across which v_o appears.

2. In fact, the wires are often twisted together to ensure that when there is noise, the same amount of noise infects both wires.

FIGURE 8.25 A differential signal.



FIGURE 8.26 Difference amplifier blackbox representation.

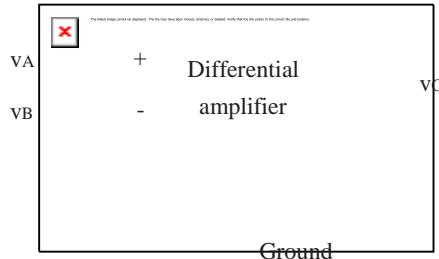
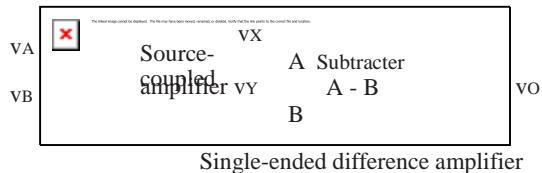


FIGURE 8.27 Single-ended difference amplifier structure.



We can also build a single-ended difference amplifier from a differential output difference amplifier as shown Figure 8.27.

The behavior of the difference amplifier is best explained by considering its effect on the following signals related to the two components, V_A and V_B :

1. A difference-mode component signal,

$$V_D = V_A - V_B \quad (8.45)$$

2. And a common-mode component signal,

$$V_C = \frac{V_A + V_B}{2} \quad (8.46)$$

2

The output of the difference amplifier is a function of these two components of the input,

$$v_o = A_D V_D + A_C V_C \quad (8.47)$$

where A_D is called the difference-mode gain and A_C is called the common-mode gain. The key is using a difference amplifier to encode the useful signal in the difference-mode component and the noise in the common-mode component. Then if we make A_D large and A_C small, we achieve our goal of noise reduction. Usually we use the common-mode rejection ratio (CMRR) to describe the ability of the amplifier to reject the common-mode noise:

$$\text{CMRR} = \frac{A_D}{A_C} \quad (8.48)$$

MOSFET Implementation of the Difference Amplifier

Let us study a MOSFET version of the difference amplifier. The amplifier employs a pair of matching transistors called the source-coupled pair. The source-coupled amplifier is shown in Figure 8.28. v_A and v_B are the inputs, and v_x and v_y are the outputs. Assume v_A and v_B are the input voltages measured with respect to ground. Also assume that v_A and v_B are small variations in the inputs, and that v_x and v_y are the corresponding small-signal variations in the output. The source-coupled pair is connected in series with a DC current source with a high internal resistance R_i . (We can implement the current source using a MOSFET biased to operate in its saturation region, but we do not show it here. For simplicity, we use an abstract non-ideal current source instead. In other words, the current source has a finite resistance, R_i .) Let the current provided by the DC current source be I .

Let us examine the difference amplifier using its small-signal model shown in Figure 8.29. Notice that an ideal current source acts like an open circuit, but a current source with an internal N or tonequivalent resistance R_i behaves like a resistor to incremental changes in its terminal variables. The MOSFETs are replaced by their small-equivalent current sources. The voltages v_{gs1} and v_{gs2} are the small-signal voltages between the gate and source of the two input MOSFETs resulting from a small change in the input voltages v_A and v_B .

The gain parameters g_{m1} and g_{m2} for the MOSFETs depend on the operating-point values of the currents through them. Assuming that the current through R_i is negligible, by symmetry, we find that the current I divides equally between the two MOSFETs. Thus each has an operating-point current equal to $I/2$. From the SCS model for the MOSFETs, given V_t and K , we can thus find the bias input voltages V_{GS1} and V_{GS2} in terms of I . In turn, the respective gains g_{m1} and g_{m2} can be determined in terms of V_{GS1} and V_{GS2} , which are themselves functions of I .

Recall that

the difference-mode component:

$$V_D = V_A - V_B$$

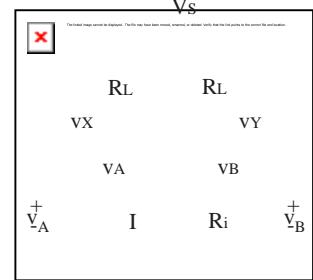


FIGURE 8.28 Source-coupled difference amplifier. All voltages are measured with respect to ground.

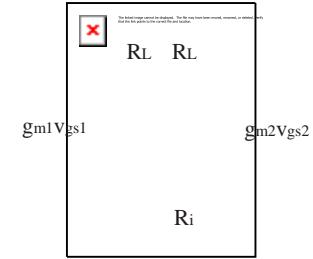


FIGURE 8.29 Source-coupled difference amplifier—small-signal model.

and the common-mode component

$$v_C = \frac{v_A + v_B}{2}$$

2

Therefore, we can decompose the inputs into their difference- and common-mode components as follows:

$$v_A = v_C + v_{2D}$$

$$v_B = v_C - \frac{v_{2D}}{2}$$

We will discuss each mode separately, and then summarize the behavior of the entire amplifier.

Difference-Mode Model

We first examine the circuit with the difference-mode part of the input only. Refer to Figure 8.30 for the circuit and its small-signal model. Assume that the two MOSFET's have identical characteristics, $g_m1 = g_m2 = g_m$. An application of KCL at the source node of the two MOSFETs (in other words, the node with the small-signal voltage v_s) yields

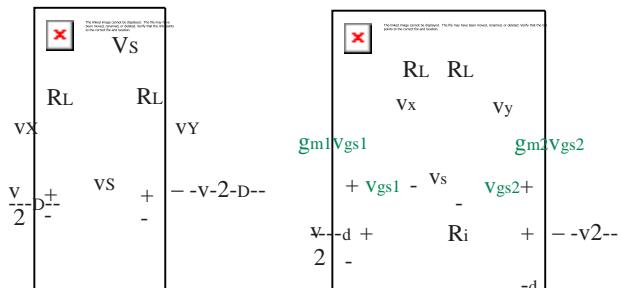
$$g_m v_{gs1} + g_m v_{gs2} = v_s / R_i \quad (8.49)$$

From Figure 8.30 we can also write

$$v_{2D} - v_{gs1} = v_s$$

$$-2v_d - v_{gs2} = v_s$$

FIGURE 8.30 Difference-mode model. All voltages are measured with respect to ground.



(a) Differential mode input only

(b) Small-signal model

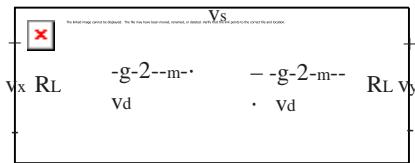


FIGURE 8.31 Difference-mode simplified model.

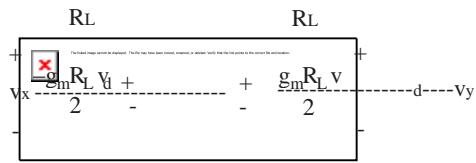


FIGURE 8.32 Difference-mode Thévenin equivalent circuit.

Substituting v_{gs1} and v_{gs2} in terms of v_i into Equation 8.49, we obtain

$$\frac{v}{g_m \frac{2d}{R_L} - v_s + g_m} - v = \frac{v_s}{R_i} \quad (8.50)$$

$$-2g_m v_s = \frac{v_s}{R_i} \quad (8.51)$$

Since g_m and R_i are independent of each other, $v_s = 0$. This result greatly simplifies our circuit to the one in Figure 8.31. Converting it to the Thévenin equivalent model, we obtain the circuit shown in Figure 8.32. We see that

$$v_x = -\frac{g_m R_L v_d}{2}$$

and

$$v_y = \frac{g_m R_i v_d}{2}$$

Thus, the small-signal output voltage across the output terminal pair is given by

$$v_o = v_x - v_y = -g_m R_L v_d.$$

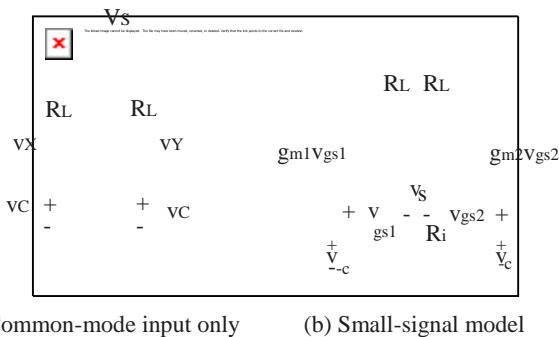
This yields a difference-mode small-signal gain

$$A_d = \frac{v_o}{v_d} = -g_m R_L.$$

Common-Mode Model

We will now examine the behavior of the circuit for the common-mode input. The circuit and small-signal model is shown in Figure 8.33. The small-signal change in the

FIGURE 8.33 Common-mode model.



(a) Common-mode input only

(b) Small-signal model

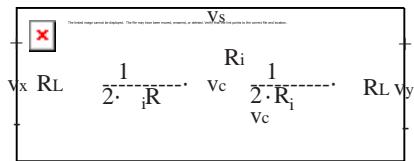


FIGURE 8.34 Common-mode Norton equivalent circuit.

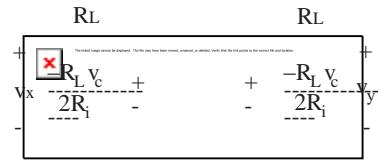


FIGURE 8.35 Common-mode Thévenin equivalent circuit.

common-mode input is denoted v_c . Observe that $v_{gs1} = v_{gs2} = v_{gs}$, and $v_{gs} = v_c - v_s$. Application of KCL at v_s again yields

$$g_m v_{gs} + g_m v_{gs} = \frac{v_s}{R_i} \quad (8.52)$$

$$2g_m v_{gs} = \frac{v_c - v_{gs}}{R_i} \quad (8.53)$$

$$v_{gs} = \frac{1}{2g_m R_i + 1} v_c. \quad (8.54)$$

Assuming R_i is large, so that $2g_m R_i \ll 1$, we can simplify Equation 8.54 to

$$v_{gs} \approx \frac{1}{2g_m R_i} v_c.$$

Therefore, the two dependent current sources will have value

$$\underline{\underline{2g_m R_i v_c.}}$$

The simplified circuit is shown in Figure 8.34. Transforming the circuit into its Thévenin equivalent circuit gives the circuit shown in Figure 8.35.

From the Thévenine equivalent circuit, notice that

$$v_x = v_y = -R_2 L R V_{ic}$$

Remarkably,

$$v_o = v_x - v_y = 0$$

effectively yielding a common-mode small-signal gain of 0.

Overall Behavior

Putting it all together, we combine the small-signal difference-mode circuit from Figures 8.32 with the small-signal common-mode circuit in 8.35 and obtain the circuit shown in Figure 8.36. Notice that we are able to do such a superposition because of the linearity property of our small-signal circuits. The output of the difference amplifier is the difference between v_x and v_y , which gives a difference-mode gain of $-g_m R_L$ and common-mode gain of 0.

Input and Output Resistances

Computing the input and output resistances for the difference amplifier is fairly easy. When we apply the small input signals v_a and v_b , there will not be any current flowing into the MOSFETs, so we have infinite input resistance.

To compute the small-signal output resistance looking in from one of the terminals of the output port, we turn off all independent sources by setting $v_a = 0$ and $v_b = 0$, in effect, turning off v_x and v_y . We introduce a test voltage at the desired output and short the other output to ground. Therefore, the overall circuit is transformed to the one shown in Figure 8.37. Thus the output resistance looking into port v_x or v_y and ground will be R_L .

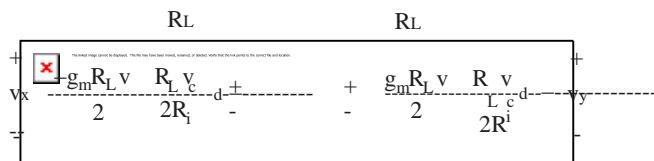


FIGURE 8.36 Difference amplifier Thévenine equivalent circuit.

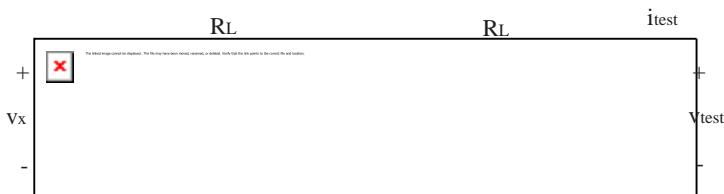


FIGURE 8.37 Difference amplifier output resistance.

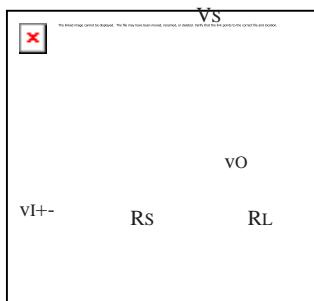


FIGURE 8.38 Source-follower circuit.

example 8.4 source follower A useful circuit we have seen before³ is the source follower shown in Figure 8.38. The source follower in the figure is showing driving an external load resistor R_L . Assume that the total input voltage v_i includes the appropriate DC bias voltage to meet the saturation discipline. The small-signal equivalent circuit for the source follower is shown in Figure 8.39. Let us analyze this circuit by computing its small-signal gain.

The small-signal output v_o can be expressed in terms of the circuit parameters as

$$v_o = g_m v_{gs} (R_L R_S)$$

where v_{gs} is the voltage between the gate and the source of the MOSFET. Using KVL, observe that $v_{gs} = v_i - v_o$. Therefore, we can write

$$v_o = g_m (v_i - v_o) (R_L R_S) \quad (8.55)$$

$$\frac{v_o}{R_L R_S} + g_m = g_m v_i \quad (8.56)$$

$$v_o = \frac{R_L R_S g_m}{R_L + R_S + R_L R_S g_m} v_i \quad (8.57)$$

$$\frac{v_o}{v_i} = \frac{R_L R_S g_m}{R_L + R_S + R_L R_S g_m}. \quad (8.58)$$

Thus the gain is slightly less than 1. An important special case of Equation 8.59 is when R_L is very large. Thus, when $R_L \rightarrow \infty$,

$$\frac{v_o}{v_i} = \frac{R_S g_m}{1 + R_S g_m}. \quad (8.59)$$

FIGURE 8.39 Source-follower small-signal model. g_m is the transconductance of the MOSFET, is given by $K(VGS - VT)$, where VGS is the operating-point value of the gate-to-source voltage for the MOSFET. (See Example 7.8 or Problem 7.5 in Chapter 7 to see how the operating-point parameters of the source follower can be calculated.)



3. See Example 7.8 and Problem 7.5 in Chapter 7.

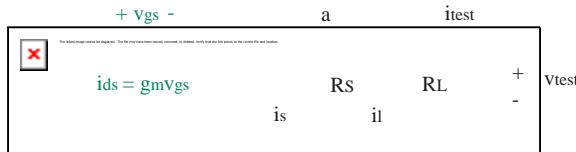


FIGURE 8.40 Source-follower outputresistance.

When g_m is large, irrespective of the values of R_L and R_S , Equation 8.58 can be rewritten as

$$\frac{v_o}{v^i} \approx 1.$$

To find out why such a circuit is useful, let us compute the input and output resistances of the source-follower device.

Small-Signal Input and Output Resistances

The input resistance r_i is easily calculated. Since no current flows into the MOSFET, the input resistance is infinity.

Computing the output resistance needs more work. As depicted in Figure 8.40, let us turn off the independent sources, apply a small test voltage v_{test} at the output terminal and measure the corresponding current i_{test} . The output resistance will be given by

$$r_{out} = v_{test}/i_{test}$$

In order to compute r_{out} , we apply KCL at node a shown in Figure 8.40. The dependent source current i_{ds} depends on V_{gs} , and V_{gs} equals $-v_{test}$. Therefore, we have

$$i_{ds} + i_{test} = i_s + i_l \quad (8.60)$$

$$-gmV_{test} + i_{test} = \frac{v_{test}}{R_L R_S}. \quad (8.61)$$

Rearranging the terms and simplifying the expression, we obtain

$$V_{test} \frac{1}{gm} + \frac{1}{R_L R_S} = i_{test}$$

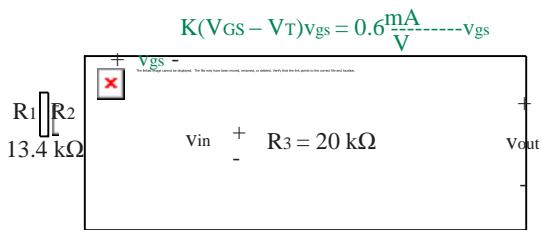
This leads to

$$r_{out} = i \frac{V_{test}}{V_{test}} = \frac{R_L R_S}{gm R_L R_S + R_L + R_S}$$

When g_m , R_L , and R_S are large, $R_L + R_S$ becomes insignificant compared to $g_m R_L R_S$. Therefore, we can simplify,

$$r_{out} \approx g_m R_S$$

FIGURE 8.41 Small-signal model of the MOSFET amplifier in Figure 7.46.



Since g_m can be made very large, the output resistance can be made low. The low output resistance makes the source follower useful as a buffer device, which can provide a large amount of current gain.

example 8.5 small-signal analysis of another mosfet amplifier In this example, we examine the small-signal behavior of the MOSFET amplifier shown in Figure 7.46 and studied in Example 7.12. This amplifier works well for both positive and negative values of V_{IN} , and so we will choose the input bias voltage to be $V_{IN} = 0$ V for the small-signal analysis. Therefore

$$V_{IN} \equiv V_{IN} + v_{in} = v_{in}.$$

To determine the remaining bias voltages in the amplifier, we set $v_{in} = 0$ V, which results in $V_{IN} = 0$ V. From the results of Example 7.12, we can then determine the bias voltages $V_{OUT} = 6.4$ V and $V_g = 0.6$ V.

Next, following the method of Section 8.2, we construct the small-signal circuit model shown in Figure 8.41. Analyzing the small-signal circuit model, we obtain

$$V_{OUT} = R_3 K(V_{GS} - V_T) v_{in} = 12 v_{in}.$$

Therefore, the small-signal gain is 12 at the bias voltage $V_{IN} = 0$. The same result can be obtained by evaluating

$$\frac{dV_{OUT}}{dV_{IN}}|_{V_{IN}=0}$$

using the results of Example 7.12.

example 8.6 small-signal model for the bjt

In

this example, we will develop the small-signal model for the BJT by linearizing the piecewise linear BJT model studied earlier in Figure 7.49c in Example 7.13. Figure 8.42b depicts the large-signal model (from Figure 7.49c) for the BJT under the constraint that

the BJT operates in its active region. When operating in the active region, the base-to-collector diode shown in Figure 7.49c behaves like an open circuit, and so it can be safely ignored in our analysis.

Figure 8.42c depicts the small-signal model of the BJT based on the piecewise-linear model in Figure 8.42b. In the active region, the ideal diode in Figure 8.42b behaves like a short circuit. Furthermore, the 0.6-V voltage source appears as a short circuit for incremental changes. Finally, since the active-region relationship between i_B and i_C is linear, and given by

$$i_C = \beta i_B,$$

the relationship between the incremental signals i_C and i_B is also the same:

$$i_C = \beta i_B.$$

Alternatively, we can derive the incremental change in the collector current for a small change in the base current mathematically from Equation 8.22 as follows:

$$\begin{aligned} i_C &= \frac{\partial i_C}{\partial i_B} i_B \Big|_{i_B=i_B} \\ &= \frac{\partial i_C}{\partial i_B} \Big|_{i_B=i_B} i_B \\ &= \beta i_B. \end{aligned}$$

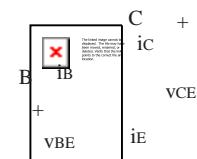
Next, we will use the small-signal model for the BJT in a few examples.



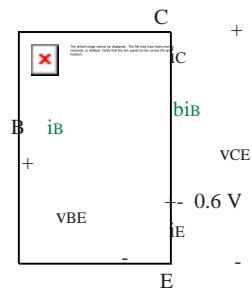
example 8.7 small-signal analysis of the bjt

amplifier In this example, we will study the small-signal behavior of the common-emitter BJT amplifier shown in Figure 7.54, which is redrawn here in Figure 8.43 to show that the total input V_{IN} is the sum of a DC offset voltage V_I and a small-signal voltage v_{in} . In keeping with our usual small-signal notation, the total, operating point, and small-signal voltages at the output are given by V_O , V_o , and v_o respectively. We will compute the small-signal gain of the amplifier assuming that the amplifier operates in its active region, and given that $R_I = 100k$, $R_L = 10k$, and $V_S = 10V$. Assume that the current-gain parameter β for the BJT is 100, and that the input operating voltage is chosen to be $V_{IN} = 1V$.

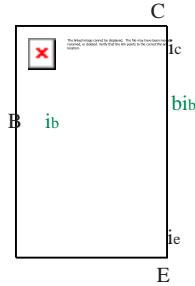
We now begin the small-signal analysis of our BJT amplifier. The first step of small-signal analysis is to determine the operating-point variables in the circuit. Although not strictly



(a) BJT symbol



(b) BJT large-signal model
assuming BJT is in active region



(c) BJT small-signal model

FIGURE 8.42 Small-signal model for the BJT.

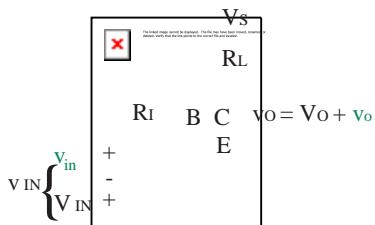


FIGURE 8.43 OurBJT amplifiers showing the small-signal and bias input voltages.

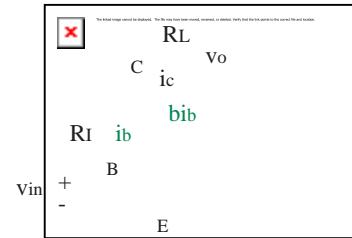


FIGURE 8.44 Small-signal circuit model for the BJT amplifier.

necessary, we will go ahead with the operating-point analysis to verify that the BJT is indeed operating in its active region for the given parameters. From the transfer function relation in Equation 7.51, we know that

$$V_O = V_{IN} \frac{-0.6\beta R_L}{R_I}$$

Substituting our specific parameter values, we obtain

$$V_O = 6V.$$

Since $V_{CE} = V_O = 6V$ and $V_{BE} = V_{IN} = 1V$, it is easy to see that the BJT constraint for active-region operation given by

$$V_{CE} > V_{BE} - 0.4V$$

is satisfied.

At the second step, we must determine linearized small-signal models for each of the circuit components. This step is trivial for our example, since all the elements are linear (including the BJT, since we are given that it always operates in its active region). The small-signal equivalents for the DC sources are short circuits, and those for the linear resistors are the resistors themselves. Finally, we will use the small-signal model for the BJT operating in its active region (developed in Example 8.6) illustrated in Figure 8.42c.

Proceeding with the third step of small-signal analysis, Figure 8.44 shows the small-signal circuit for the amplifier in which the components have been replaced by their respective

4. This step is not strictly necessary in our example because all the elements are linear (including the BJT, since we are given that it always operates in its active region). For linear elements, the small-signal model relationships are independent of their operating points. Compare, for example, the small-signal relations for the BJT and the MOSFET shown in Equations 8.62 and 8.10, respectively.

linearized equivalents, and in which small-signal branch variables have replaced the total variables.

The small-signal gain can now be determined by writing the node equation for the output node

$$R_{V_o L} = -\beta R_I.$$

Substituting $i_B = v_{in}/R_I$, we get

$$\frac{V_o}{R_L} = -\beta R_I \frac{V_{in}}{R_I}.$$

Simplifying, we obtain the small-signal gain of the BJT amplifier

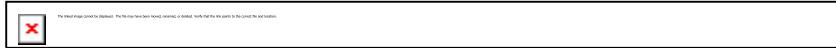
$$\text{Small-signal gain} = \frac{V_o}{V_{in}} = -\beta R \frac{L}{R_I}. \quad (8.62)$$

Notice here that the gain of the BJT amplifier is independent of the operating point, provided the BJT operates in the active region. For a given BJT device (that is, a fixed value for β) the gain can be increased by increasing R_L or decreasing R_I .

Finally, substituting $R_I = 100k$, $R_L = 10k$, $\beta = 100$, we obtain

$$\text{Small-signal gain} = -10.$$

This concludes our analysis.



example 8.8 small-signal input and output resistance of the bjt amplifier Let us first compute the small-signal input and output resistances of the common emitter BJT amplifier. The general approach to doing so is to turn off all independent sources and to apply a test voltage (or current) at the input or output port as appropriate and to measure the resulting current (or voltage). The ratio of the voltage to the current gives the resistance.

The input resistance is easily calculated. For an applied test voltage v_{in} (see Figure 8.45), the resulting current into the input B terminal is given by

$$i_{B\text{ test}} = \frac{V_{in}}{R_I}$$

Thus the input resistance is simply R_I .

As illustrated in Figure 8.46, we compute the output resistance by turning off all independent sources, and applying a small test voltage v_{test} at the output port and measuring the corresponding current i_O . The output resistance will be given by $r_{out} = V_{test}/i_O$.

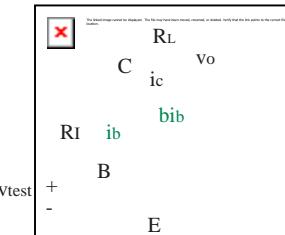


FIGURE 8.45 Applying a small-signal test voltage to the input port of the BJT amplifier to compute the small-signal input resistance.

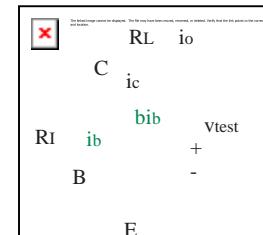


FIGURE 8.46 Applying a small-signal test voltage to the output port of the BJT amplifier to compute the small-signal output resistance.

In order to compute i_{out} , we apply KCL at the node labeled C shown in Figure 8.46. Summing all the currents going into node C, we get

$$i_{out} - \frac{V_{test}}{R_L} - \beta i_b = 0.$$

Since $i_b = 0$ (the voltage across R_i is zero), we get

$$r_{out} = \frac{V_{test}}{i_{out}} = R_L.$$

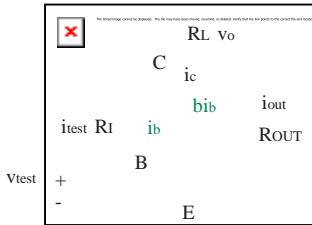


FIGURE 8.47 Incremental circuit for the BJT amplifier including an external load resistor to facilitate current gain and power gain calculations.

example 8.9 small-signal current gain and power gain of the bjt amplifier In this example, let us compute the incremental current and power gain for the common-emitter BJT amplifier. Both the current gain and the power gain are defined as the current or power supplied to an external load divided by the current or power supplied by an input source. Accordingly, as illustrated in Figure 8.47, let us add an external load resistance $ROUT$ to our circuit to facilitate current and power gain measurements.

The incremental current gain is defined as the change in the output current (i_{out}) divided by the change in the input current (i_{test}), for a given external load resistance. We begin by writing the node equation for the node labeled C

$$\frac{V_o}{i_{out} + i_c + \frac{V_{test}}{R_L}} = 0. \quad (8.63)$$

We will obtain the desired relation between i_{out} and i_{test} if we can replace i_c and v_o in terms of i_{test} . From the BJT relation, we know that

$$i_c = \beta i_b = \beta i_{test}. \quad (8.64)$$

To determine v_o in terms of i_{test} , observe that v_o is the voltage drop across the parallel resistor pair comprising R_L and $ROUT$. In other words,

$$v_o = -i_c(R_L + R_{OUT}).$$

Substituting for i_c , we get the desired relation between v_o and i_{test} :

$$v_o = -\beta i_{test}(R_L + R_{OUT}). \quad (8.65)$$

Substituting for i_c and v_o from Equations 8.64 and 8.65 into 8.63 we obtain

$$i_{out} + \beta i_{test} - \frac{\beta i_{test}(R_L + R_{OUT})}{R_L} = 0.$$

Dividing throughout by i_{test} and simplifying, we obtain the current gain as

$$\text{Current gain} = i \frac{i}{i_{\text{test}}} = -\beta \frac{R_L}{R_L + R_{\text{OUT}}}. \quad (8.66)$$

Intuitively, we can also obtain the same current gain result in two short steps as follows: First, notice that the current i is simply i_{test} amplified by a factor β . Second, the fraction of the amplified current βi_{test} that flows into R_{OUT} is given by the current-divider relation from Equation 2.84 as the ratio of the opposite resistor R_L divided by the sum of the two resistors ($R_L + R_{\text{OUT}}$).

Next, the incremental power gain is defined as the ratio of the power supplied into the output resistor ($v_o i$) and the power supplied by the input source ($v_{\text{test}} i_{\text{test}}$), for a given external load resistance. As suggested by Equation 8.38, the power gain is equal to the product of the current gain and the voltage gain for the BJT amplifier.

For the BJT amplifier that includes an output load resistance, the current gain is given by Equation 8.66. For reasons that will be obvious momentarily, we will rewrite the current gain in terms of the parallel combination of R_L and R_{OUT} as

$$\frac{i}{i_{\text{test}}} = -\beta \frac{(R_L R_{\text{OUT}})}{R_{\text{OUT}}} \quad (8.67)$$

We can determine the voltage gain by including the effect of the output load resistance R_{OUT} on the voltage gain equation of the BJT given by Equation 8.62. We do so by replacing the resistance R_I in Equation 8.62 with the equivalent resistance of the parallel resistor pair R_L and R_{OUT} as

$$\frac{v_o}{v_{\text{test}}} = -\beta \frac{R_L R_{\text{OUT}}}{R_I} \quad (8.68)$$

Taking the product of the current gain (Equation 8.67) and the voltage gain (Equation 8.68) and simplifying, we obtain

$$\text{Power gain} = \beta^2 \frac{(R_L R_{\text{OUT}})^2}{R_I R_{\text{OUT}}} \quad$$



example 8.10 small signal of the operational amplifier circuit This example develops a small-signal model of the operational amplifier circuit shown in Figure 7.63 and previously discussed in Example 7.21. It then uses that model to determine the small-signal gain of the amplifier. The small-signal model and gain are determined for the bias conditions established by $V_{\text{IN}1} = V_{\text{IN}2} = 0$. Under these balanced bias conditions, $I_{\text{D}1} = I_{\text{D}2} = I/2$.

FIGURE 8.48 A small-signal model of the operational amplifier circuit.

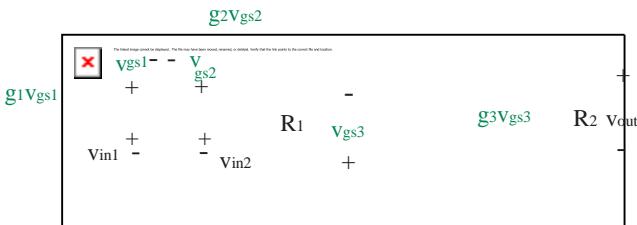


Figure 8.48 shows a small-signal model of the operational amplifier shown in Figure 7.63. The three MOSFET transconductances g_1 , g_2 , and g_3 in Figure 8.48 are not yet determined.

Following the results summarized in Figure 8.10, the small-signal transconductances of the n-channel MOSFETs are given by

$$g_1 = K_n(V_{GS1} - V_T) \quad (8.69)$$

$$g_2 = K_n(V_{GS2} - V_T). \quad (8.70)$$

However, remember that we have chosen to bias the operational amplifiers such that

$$I_{D1} = \frac{I}{2} = \underline{K_n(V_{GS1} - V_T)_2} \quad (8.71)$$

$$I_{D2} = \frac{I}{2} = \underline{K_n(V_{GS2} - V_T)_2} \quad (8.72)$$

Equations 8.71 and 8.72 can be substituted into Equations 8.69 and 8.70, respectively, to yield

$$\underline{g_1 = g_2 = K_n I}. \quad (8.73)$$

A similar small-signal model of the p-channel MOSFET can also be determined following the approach developed in Section 8.2. Specifically, taking the slope of Equation 8.67 at its bias point yields

$$\underline{-id \approx K(V_{SG} + V_T)v_{sg}} \quad (8.74)$$

and so the transconductance from v_{sg} to $-id$ is given by

$$\underline{g = K(V_{SG} + V_T) = 2K(-Id)} \quad (8.75)$$

where the large-signal bias condition for the p-channel MOSFET has been used to derive the last equality. Applying this to the operational amplifiers shown in Figure 8.48 yields

$$\underline{g_3} = \underline{2K_p(-ID_3)}. \quad (8.76)$$

The small-signal model can now be used to determine the small-signal gain of the operational amplifier. Consider first the portion of the small-signal model that corresponds to the differential amplifier alone. KCL applied to the node between the two n-channel MOSFETs yields

$$\underline{i_{d1} + i_{d2}} = \underline{g_1 v_{gs1} + g_2 v_{gs2}} = 0. \quad (8.77)$$

Thus, an increase in one drain current in the differential amplifier is matched by an equal decrease in the other drain currents since both drain currents must sum to I . Next, the application of KVL to the loop around the two MOSFETs through ground yields

$$\underline{v_{in1} - v_{in2}} = \underline{v_{gs1} - v_{gs2}}. \quad (8.78)$$

Finally, combining Equations 8.73, 8.77, and 8.78 with the observation from Figure 8.48 that $v_{sg3} = R_1 g_2 v_{gs2}$ yields

$$\underline{v_{sg3}} = \underline{\frac{-R_1 \sqrt{K_n I(v_{in1})}}{2} (-v_{in2})} \quad (8.79)$$

as the small-signal gain of the differential amplifier.

Consider next the portion of the small-signal circuit that corresponds to the common-source stage built with the p-channel MOSFET. For this stage, the small-signal model shows that

$$\underline{v_{out}} = \underline{R_2 \frac{2K_p(-ID_3)}{2} v_{sg3}} \quad (8.80)$$

where Equation 8.76 has been used to rewrite g_3 . Note that the gain of this stage is positive because that gain is from v_{sg3} to v_{out} .

Finally, Equations 8.79 and 8.80 can be combined to yield

$$\underline{v_{out}} = \underline{\frac{R_1 R_2 2K_n K_p I(-ID_3)(v_{in2})}{2} (-v_{in1})} \quad (8.81)$$

as the small-signal gain of the unloaded operational amplifier.

In operational amplifier parlance (see Chapter 15), from Equation 8.81 we see that V_{IN1} and V_{IN2} play the roles of v_- and v_+ , respectively.

example 8.11 more on the small-signal model of the operational amplifier We will now work a numerical example related to the operational amplifier design described in Example 8.10, assuming that $-I_{D3}=0.5\text{mA}$.

Substitution of this value of $-I_{D3}$ and the parameters from Example 8.10, into Equation 8.81 yields

$$V_{\text{out}}=50\sqrt{2}(V_{\text{in}2}-V_{\text{in}1}) \quad (8.82)$$

Thus, the small-signal gain of the operational amplifier is approximately 71.

8.3 SUMMARY

This chapter expanded on our treatment of small-signal models, focusing on the model for three-terminal devices and amplifiers. As first introduced in Section 4.5, small-signal analysis applies when devices and circuits that are possibly nonlinear are operated over a very narrow range. Small-signal analysis finds a piecewise linear model that ensures maximum accuracy of fits over that narrow operating range. The principal benefit of small-signal models is that the small-signal variables display linear relationships over the narrow operating range, thereby enabling the use of all of our linear analysis techniques such as superposition, Thévenin, and Norton.

This chapter also introduced the small-signal circuit model. The small-signal circuit facilitates small-signal analysis by creating a circuit that is representative of the original large-signal circuit and involves only its small-signal variables. The small-signal circuit can be derived from the original circuit by executing the following procedure:

1. Set each source to its operating-point value, and determine the operating-point branch voltages and currents for each component in the circuit. This step involves a large-signal analysis that is possibly nonlinear.
2. Determine the linearized small-signal behavior of each component about its operating point, and select a linear component to represent this behavior.
3. Replace each original component in the circuit with its linearized equivalent (also called the small-signal equivalent model) and re-label the circuit with the small-signal branch variables. The resulting circuit is the desired small-signal model.

The small-signal equivalent model for an independent DC voltage source is a short circuit, while that for an independent DC current source is an open circuit. The small-signal equivalent model for a resistor is the resistor itself. The small-signal model for a MOSFET is shown in Figure 8.10.

exercise 8.1 Consider the amplifier shown in Figure 8.49. The MOSFET operates in its saturation region and is characterized by the parameters V_T and K . The input voltage v_i comprises the sum of a DC bias voltage V_i and a sinusoid of the form $v_i = A \sin(\omega t)$. Assume that A is very small compared to V_i . Let the output voltage v_o comprise a DC bias term V_o and a small-signal response term $v_o - V_o$.

EXERCISES

- a) Determine the output operating point voltage V_o for the input bias of V_i .
- b) Determine the small-signal gain of the amplifier.

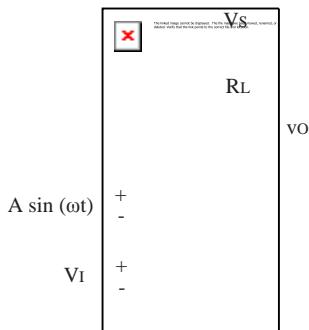


FIGURE 8.49

c) Draw the form of the input and output voltages as a function of time, clearly showing the DC and time-varying small-signal components.

exercise 8.2 Develop the small-signal model for a two-terminal device formed by a MOSFET with its gate tied to its drain, operating under the saturation discipline, with parameters V_T and K .

exercise 8.3 Develop the small-signal model for a two-terminal device formed between the drain and source terminals of a MOSFET with a 2 volt DC source connected between its gate and source terminals ($V_{GS} = 2V$). Assume the MOSFET operates

under the saturation discipline. Assume further that $V_D = 1V$ for the MOSFET.

exercise 8.4 Consider the MOSFET amplifier shown in Figure 8.50. Assume that the amplifier is operated under the saturation discipline. In its saturation region, the MOSFET is characterized by the equation

$$i_{DS} = K_2(v_{GS} - V_T)^2$$

where i_{DS} is the drain-to-source current when a voltage v_{GS} is applied across its gate-to-source terminals.

- a) Write an expression relating v_O to v_I . What is its operating-point output voltage V_O , given an input operating-point voltage of v_I ? What is the corresponding operating-point current i_{DS} ?
- b) Assuming an operating-point input voltage of v_I , derive the expression relating the small-signal output voltage v_O to the small-signal input v_I from the relationship between v_O and v_I . What is the small-signal gain of the amplifier at the input operating point of v_I ?
- c) Draw the small-signal equivalent circuit for the amplifier based on the SCS model of the MOSFET assuming the operating-point input voltage is v_I .
- d) Derive an expression for the small-signal gain of the amplifier from the small-signal equivalent circuit. Verify that the gain computed from the small-signal equivalent circuit is identical to the gain computed in part (b).
- e) By what factor must R_L change to double the small-signal gain of the amplifier? What is the corresponding change in the output bias voltage?
- f) By what factor must V_D change to double the small-signal gain of the amplifier? What is the corresponding change in the output bias voltage?

exercise 8.5 Consider again the MOSFET amplifier shown in Figure 8.50. Assume as before that the MOSFET is operated under the saturation discipline, and that its parameters are V_T and K .

- a) What is the range of valid input voltages for the amplifier? What is the corresponding range of valid output voltages?

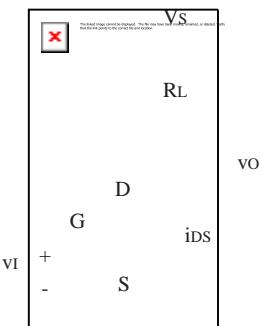


FIGURE 8.50

b) Assuming we desire to use voltages of the form $A \sin(\omega t)$ as AC inputs to the amplifier, determine the input bias point V_I for the amplifier that will allow maximum input swing under the saturation discipline. What is the corresponding output bias point voltage V_O ?

c) What is the largest value of A that will allow saturation region operation for the bias point determined in (b)?

d) What is the small-signal gain of the amplifier for the bias point determined in (b)?

e) Suppose A is small compared to V_I . Write an expression for the small-signal output voltage v_o for the bias point determined in (b).

exercise 8.6 Consider once more the MOSFET amplifier shown in Figure 8.50. Assume as before that the amplifier is operated under the saturation discipline, and that its parameters are V_T and K .

a) Using the small-signal circuit model of the amplifier, and assuming an input bias voltage V_I , determine the small-signal output resistance of the amplifier. That is, determine the equivalent resistance of the amplifier at the output port of its small-signal model with $v_i = 0$.

b) Develop a Thévenin equivalent model for the small-signal amplifier as observed at its output port.

c) What is its input resistance? That is, determine the equivalent resistance of the amplifier at the input port of its small-signal model.

exercise 8.7 Consider the common emitter BJT amplifier shown in Figure 8.51. The input voltage v_{IC} comprises the sum of a DC bias voltage $V_I = 0.7V$ and a sinusoid of the form $v_i = A \sin(\omega t)$, where $A = 0.001V$. For the values shown, you may assume that A is very small compared to V_I . You may further assume that the BJT always operates in its active region. Figure 8.52 shows a small-signal model for the BJT operating in its active region. Let the output voltage v_o comprise a DC bias term V_o and a small-signal response term v_{oA} .

a) Determine the output operating-point voltage V_o for the input bias of $V_I = 0.7V$.

b) Draw the small-signal equivalent circuit for the amplifier.

c) Determine the small-signal gain of the amplifier.

d) What is the value of v_o , the small-signal component of the output, given the small-signal input shown in Figure 8.51?

e) Determine the small-signal input and output resistances of the amplifier.

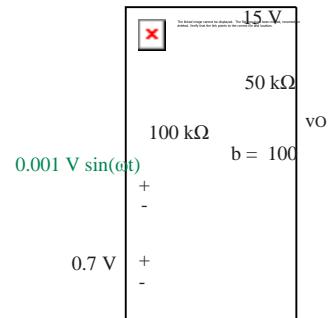
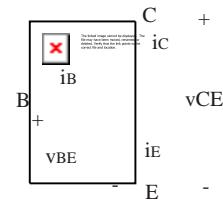
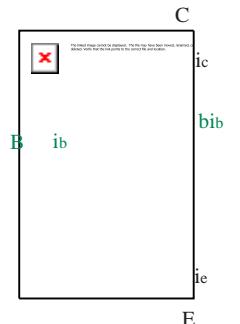


FIGURE 8.51



(a) BJT



(b) BJT small-signal model

FIGURE 8.52

f) Determine the small-signal current and power gain of the amplifier, assuming that the amplifier drives a load $R_o = 50\text{k}\Omega$ that is connected between the output node and ground.

PROBLEMS

problem 8.1 This problem studies the small-signal analysis of the MOSFET amplifier discussed in Problem 7.3 (Figure 7.75).

- First, consider biasing the amplifier. Determine V_{IN} , the bias component of v_{IN} , so that V_{OUT} is biased to V_{OUT} where $0 < V_{OUT} < V_s$. Find V_{MID} , the bias component of v_{MID} in the process.
- Next, let $V_{IN} = V_{IN} + v_{in}$ where v_{in} is considered to be a small perturbation of V_{IN} around V_{IN} . Make the substitution for V_{IN} and linearize the resulting expression for V_{OUT} . Your answers should take the form $V_{OUT} = V_{OUT} + v_{out}$, where v_{out} takes the form $v_{out} = G v_{in}$. Note that v_{out} is the small-signal output and G is the small-signal gain. Derive an expression for G .
- For what value of V_{IN} is V_{OUT} biased to $V_{OUT} = V_s/2$? For this value of V_{IN} , evaluate G using the numerical parameters given in Problem 7.2. You should find that this gain is the slope of the input-output graph from Problem 7.3 evaluated at the bias point.

problem 8.2 Consider again the buffer described in Problem 7.5 (Figure 7.76). Perform a small-signal analysis of this circuit according to the following steps. Assume that the MOSFET operates in its saturation region and continue to use the SCSMOSFET model with parameters V_T and K .

- Draw the small-signal circuit model of the buffer.
- Show that the small-signal transconductance g_m of the MOSFET is given by

$$g_m = K(V_{IN} - V_{OUT} - V_T)$$

where V_{IN} and V_{OUT} are the bias, or operating-point, input and output voltages, respectively.

- Determine the small-signal gain of the buffer. That is, determine the ratio V_{OUT}/v_{in} .
- Determine the small-signal output resistance of the buffer. That is, determine the equivalent resistance of the buffer at the output port of its small-signal model with $v_{in} \equiv 0$.
- Assume that $V_T = 1\text{V}$, $K = 2\text{mA/V}^2$, $R = 1\text{k}\Omega$, and $V_s = 10\text{V}$. Under this assumption, design the input bias voltage to satisfy the following two objectives: First, MOSFET operation must remain within the saturation region for $|v_{in}| \leq 0.25\text{V}$. Second, the output resistance of the small-signal model must be minimized.

f) Again assume that $V_T = 1V$, $K = 2mA/V^2$, $R = 1k$, and $V_S = 10V$. For $V_{IN}=3V$, compute the small-signal gain and output resistance.

g) Determine the small-signal input resistance of the buffer. That is, determine the equivalent resistance of the buffer at the input port of its small-signal model.

problem 8.3 This problem studies the small-signal analysis of the ZFET amplifier from Problem 7.6 (Figure 7.77). Assume that the amplifier is biased at an input voltage V_{IN} such that the ZFET exhibits saturated operation; the corresponding bias output voltage is V_{OUT} . For this case, derive the small-signal voltage gain v_{out}/v_{in} of the amplifier.

problem 8.4 The circuit shown in Figure 8.4 delivers a nearly constant current to its load despite the fact that the power supply is noisy. The noise is modeled by the small signal v_s superimposed on the constant-supply voltage V_S . Thus, V_S and v_s are the large-signal and small-signal components of the total powersupply voltage v_s , respectively. i_L and i are the large-signal and small-signal components of the load

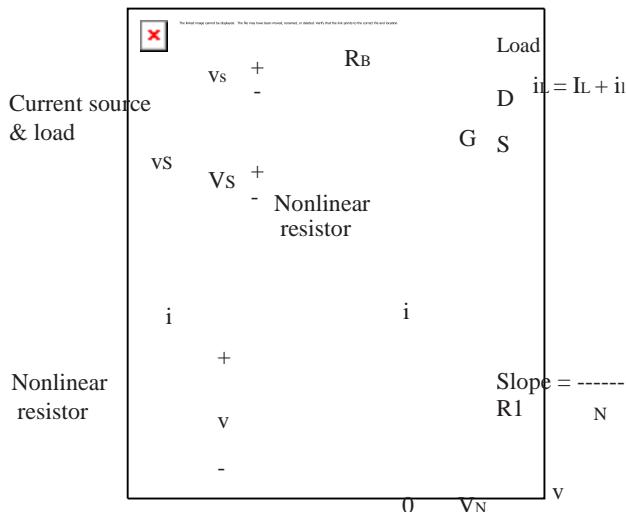


FIGURE 8.53

current i_L , respectively. The noise v_s in the power supply voltage satisfies $v_s \ll V_S$, and is responsible for the presence of i_L .

The current source contains a MOSFET which operates in its saturation region such that $i_{DS} = \frac{K}{2}(V_{GS}-V_T)^2$. The current source also contains a nonlinear resistor whose terminal characteristics are described graphically next. Assume that $V_S > V_G > V_N$.

a) Assume $v_s=0$. Determine V_{GS} , the large-signal component of V_{GS} , in terms of R_B , R_1 , V_S , and V_N .

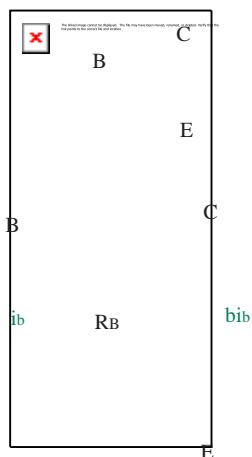


FIGURE 8.54

- b) Following the result of part(a), determine I in terms of R_B , R_N , V_N , V_s , K , and V_T .
- c) Now assume that $v_s = 0$. Draw a small-signal circuit model for the combined circuit comprising the power supply, current source and load, with which i can be found from v_s . Clearly label the value of each component in the circuit model.
- d) Using the small-signal model from part(c), determine the ratio i/v_s .

problem 8.5 Figure 8.54 depicts a bipolar junction transistor (BJT). Recall that a BJT has three terminals called the base (B), the collector (C), and the emitter (E). Figure 8.54 also shows an alternative small-signal model for the BJT operating in its active region. This model is slightly different from the small-signal BJT model discussed in this chapter in that it includes a base resistance R_B . In the model shown in the figure, β is a constant.

- a) Draw the small-signal equivalent circuit for the BJT amplifier shown in Figure 8.55. Use the small-signal equivalent circuit to derive the small-signal gain of the amplifier.
- b) Draw the small-signal equivalent circuit for the BJT amplifier shown in Figure 8.56. Notice that the resistor divider provides the necessary bias voltage. Use the small-signal equivalent circuit to derive the small-signal gain of the amplifier.

problem 8.6 Consider the MOSFET-based amplifier circuit discussed in Problem 7.8 (Figure 7.79). Assuming an input bias point voltage v_I , draw the small-signal circuit equivalent of the amplifier. Determine the small-signal gain of the amplifier. Assume throughout that the MOSFET operates in its saturation region.

problem 8.7 Consider again the amplifier circuit discussed in Problem 7.8 (Figure 7.79). Suppose that the amplifier is biased such that $v_I = v_O$ at the bias point. Draw the small-signal circuit equivalent of the amplifier assuming this bias point. Determine the small-signal gain of the amplifier at this bias point. Assume that the MOSFET operates in its saturation region.

problem 8.8 Consider the common-gate amplifier circuit shown in Figure 7.82, and analyze it earlier in Problem 7.11. Assume that the MOSFET operates in its saturation region, and is characterized by the parameters V_T and K .

- a) Draw the SC equivalent circuit by replacing the MOSFET by its SC model.
- b) Determine the output operating-point voltage V_{OUT} and operating-point current I_D in terms of an input operating-point voltage V_{IN} .
- c) Assuming an input bias point voltage V_{IN} , draw the small-signal model of the amplifier.
- d) Determine the small-signal gain v_{out}/v_{in} of the amplifier.

FIGURE 8.55

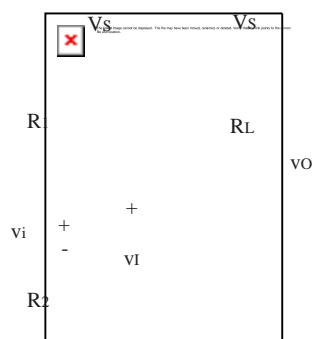


FIGURE 8.56

- e) Determine the small-signal output resistance of the amplifier. That is, determine the equivalent resistance of the amplifier at the output port of its small-signal model with $v_i = 0$. Is the small-signal output resistance greater than, less than, or equal to that of the “commonsource” amplifiers shown in Figure 8.50?
- f) Determine the small-signal input resistance of the amplifier. That is, determine the equivalent resistance of the amplifier at the input port of its small-signal model. Is the small-signal input resistance greater than, less than, or equal to that of the “commonsource” amplifiers shown in Figure 8.50?

problem 8.9 Consider the circuit illustrated in Figure 7.86 and analyzed in Problem 7.15. Assume that the MOSFET operates in its saturation region, and is characterized by the parameters V_T and K .

- a) Draw the SC equivalent circuit by replacing the MOSFET by its SCS model.
- b) Determine the output operating-point voltage V_O and operating-point current I_D in terms of an input operating-point voltage V_I .
- c) Assuming an input bias point voltage V_I , draw the small-signal model.
- d) Determine the small-signal gain v_o/v_i .
- e) Determine the small-signal output resistance.
- f) Determine the small-signal input resistance.

problem 8.10 Consider the circuit illustrated in Figure 7.87 and analyzed in Problem 7.16. Assume that the MOSFET operates in its saturation region, and is characterized by the parameters V_T and K .

- a) Draw the SC equivalent circuit by replacing the MOSFET by its SCS model.
- b) Determine the output operating-point voltage V_O and operating-point current I_D in terms of an input operating-point voltage V_I .
- c) Assuming an input bias point voltage V_I , draw the small-signal model.
- d) Determine the small-signal gain v_o/v_i .
- e) Determine the small-signal output resistance.
- f) Determine the small-signal input resistance.

problem 8.11 This problem studies the small-signal analysis of the amplifier analyzed in Problem 7.14 (see Figure 7.85). Assume that the MOSFET operates in its saturation region, and is characterized by the parameters V_T and K .

- a) Draw the small-signal equivalent circuit of the amplifier driving the load resistor R_E , assuming an input bias voltage V_I .
- b) Determine the small-signal gain of the amplifier when it is driving the load R_E .

problem 8.12 This problem studies the small-signal analysis of the circuit analyzed in Problem 7.17 (see Figure 7.88). Assume that the MOSFET operates in its saturation region, and is characterized by the parameters V_T and K .

- Draw the small-signal equivalent circuit assuming an input bias voltage V_I . What is the value of g_m for the MOSFET under the given biasing conditions?
- Determine the small-signal voltage gain v_o/v_i . What does the v_o/v_i expression simplify to when each of $g_m R_1$, $g_m R_2$, and $g_m R_L$ is much greater than 1?

problem 8.13 This problem studies the small-signal analysis of the source follower (or common collector) BJT circuit analyzed in Problem 7.18 (see Figure 7.89). Assume that the BJT operates in its active region throughout this problem.

- Determine the output operating-point voltage V_O and operating-point current I_E in terms of an input operating-point voltage V_I .
- Assuming an input bias point voltage V_I , draw the small-signal model of the source-follower amplifier.
- Determine the small-signal gain v_o/v_i of the amplifier.
- Determine the small-signal output resistance of the source follower amplifier. Is this resistance greater than, less than, or equal to that of the “common emitter” amplifier analyzed in Exercise 8.7 and shown in Figure 8.51?
- Determine the small-signal input resistance of the amplifier. Is the input resistance greater than, less than, or equal to that of the “common emitter” amplifier shown in Figure 8.51?
- Determine the small-signal current and power gain of the source follower amplifier. Assume for this part that the amplifier is driving an output load of R_O connected between the output node and ground.

problem 8.14 Consider a gain in the compound three-terminal device formed by connecting two BJTs in the configurations shown in Figure 7.90 (Problem 7.19). This problem relates to the small-signal analysis of this device. Assume that the two BJTs are identical, each with $\beta = 100$, and that each of the BJTs operates in the active region.

- Draw the active-region equivalent circuit of the compound BJT by replacing each of the BJTs by the piecewise linear (large signal) model shown in Exercise 7.8. Clearly label the C, B, and E terminals.
- Develop a small-signal model containing a single dependent current source for the compound device by linearizing the circuit model in (a) and simplifying suitably.

chapter 9

9.1 CONSTITUTIVE LAWS

9.2 SERIES AND PARALLEL CONNECTIONS

9.3 SPECIAL EXAMPLES

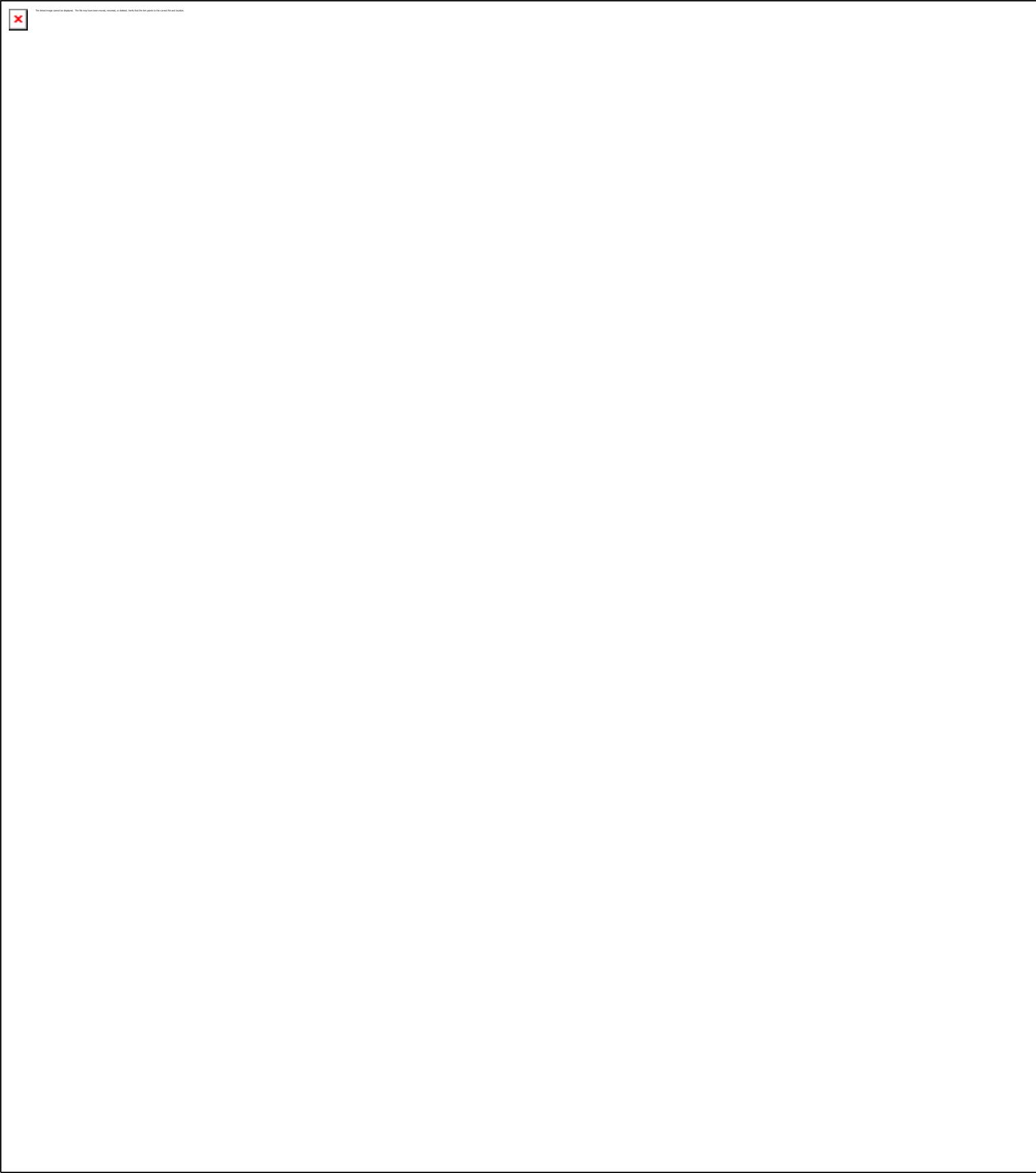
9.4 SIMPLE CIRCUIT EXAMPLES

9.5 ENERGY, CHARGE, AND FLUX CONSERVATION

9.6 SUMMARY

EXERCISES

PROBLEMS



energy storage elements

9

To this point in our study of electronic circuits, time has not been important. The analyses and designs we have performed so far have been static, and all circuit responses at a given time have depended only on the circuit inputs at that time. An important consequence of this is that our circuits have so far responded to input changes infinitely fast. This of course does not happen in reality. Circuits do take time to respond to their inputs, and this delay is often of significant importance.

As an example of circuit delays, and the importance of time in describing the response of a circuit, consider the two cascaded inverters shown in Figure 9.1. The ideal response of the first inverter, based on our analysis of electronic circuits to this point, is shown in Figure 9.2. A square-wave input yields an inverted square-wave output. However, in reality, the output shown in Figure 9.3 is more likely to occur, which is a much more complex function of time. This example is discussed in detail in Section 10.4, where we will show that the complex time behavior shown in Figure 9.3 directly relates to the speed at which circuits can operate. In this chapter, we will lay the foundation for that discussion.

In order to explain the temporal behavior of circuit responses such as that shown in Figure 9.3, we must introduce two new elements, namely capacitors and inductors. For example, we shall see that it is a capacitance internal to the MOSFET that is responsible for the non-ideal inverter responses shown in Figure 9.3. For simplicity, we did not model that characteristic of the MOSFET in earlier chapters, but we will begin to do so now in Section 9.3.1.

There are other ways in which a capacitance or an inductance can inadvertently slow down a circuit. One way is shown in Figure 9.4. This figure

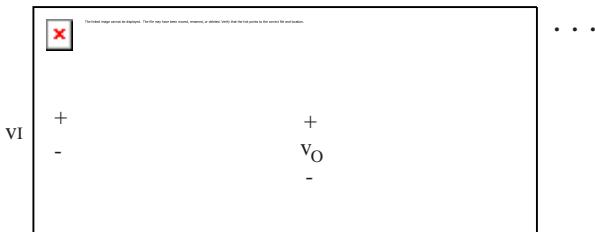


FIGURE 9.1 Two cascaded inverters.

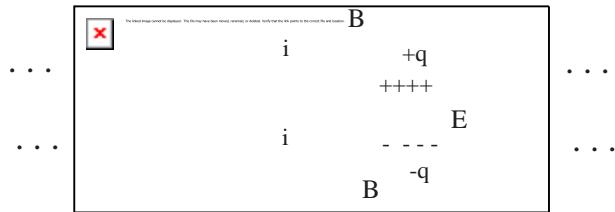


FIGURE 9.2 Ideal response of the first inverter to a square-wave input.



FIGURE 9.3 Observed response of the first inverter to a square-wave input.

FIGURE 9.4 The behavior of a real interconnect between two inverters.



shows two inverters communicating over a long interconnect. As we discussed in Chapter 1, within our lumped-circuit abstraction, the interconnect is perfect. Specifically, by the definition of the lumped circuit abstraction (see Section 1.2), the wires interconnecting the elements have no resistance. Furthermore, by the lumped matter discipline which underlies the lumped circuit abstraction, the wires and other circuit elements store no electric charge and link no magnetic flux outside the elements. Reality, however, is different, and in some cases this difference is important. As Figure 9.4 shows, any interconnect having a potential difference with its surroundings actually stores an electric charge q that sources an electric field E between that charge and its image. Furthermore, in order to supply the charge, a current must flow around the interconnect loop. This current in turn generates a magnetic flux density B that is linked by the loop. So, real interconnects do store electric charge and link external magnetic flux, thereby appearing to violate the lumped matter discipline. They will also exhibit a non-zero resistance. These factors can all contribute to a reduction in the speed of the circuit as a whole, and at times it is important to study these effects.

Reality now presents us with a dilemma. On the one hand, we wish to work within the framework of the lumped circuit abstractions so that the circuits we study all fit within this easily-managed framework. On the other hand, we should not be forced to ignore circuit effects, in this case parasitic resistance, capacitance, and inductance, that significantly affect circuit performance. The resolution of this dilemma is the modeling compromise mentioned in Chapter 1. Figure 1.27 in Chapter 1 used an ideal wire in series with a lumped resistor to model a physical wire with some parasitic resistance. Similarly, we will introduce lumped capacitors and lumped inductors to model the effect of the charge and the flux. As illustrated in Figure 9.5, a capacitor comprising a pair of parallel plates collects the positive and negative charge on its plates and effectively models the distributed charge. Notice that because the capacitor contains equal positive and negative charges the net charge within the capacitor element is zero, thereby satisfying the lumped matter discipline. Thus, the capacitor can be viewed as a lumped element. In like manner, we will introduce a lumped inductor to model the effect of the flux linked with the wires as illustrated in Figure 9.6. The lumped matter discipline is satisfied because the flux is entirely contained inside the lumped inductor, and there is no net flux outside the element.

By using lumped resistors, capacitors, and inductors to model the effect of the resistance, charge, and flux associated with the physical wiring of the

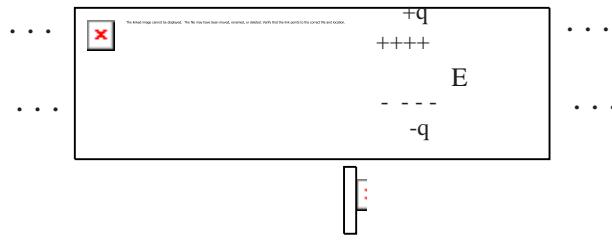


FIGURE 9.5 The capacitor models the effect of the distributed charge.

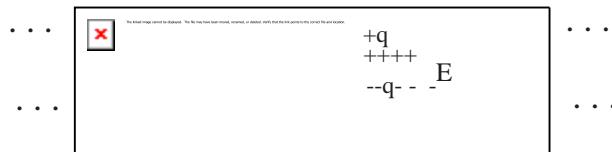


FIGURE 9.6 The inductor models the effect of the flux.



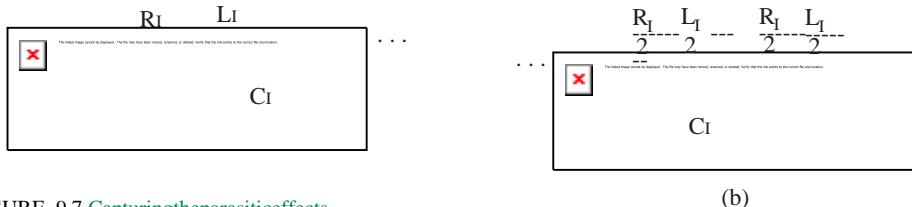
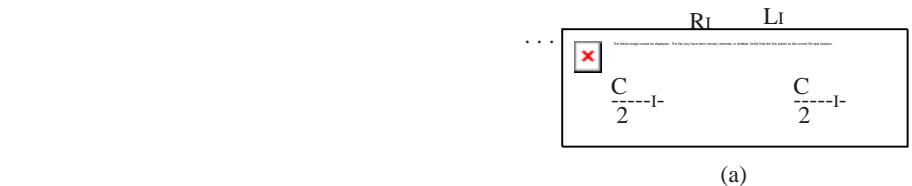


FIGURE 9.7 Capturing the parasitic effects of resistance, charge, and flux through the use of resistors, capacitors, and inductors, respectively. Capacitors and inductors are formally introduced in Section 9.1.

FIGURE 9.8 Two different lumped models for an interconnect that account for interconnect resistance, capacitance, and inductance.

circuit, as shown in Figure 9.7, the wiring within the augmented circuit model remains perfect in keeping with the lumped circuit abstraction. In the figure, the interconnect resistance, capacitance, and inductance are R_I , C_I , and L_I total, respectively.

Figure 9.7 represents one of the simplest models used to model real interconnects. For more accuracy, since we can use as many additional lumped elements as we wish, we can arbitrarily approach the distributed modeling limit, although generally this is not necessary. For example, the two models shown in Figure 9.8 do a better job of modeling reality. The interconnect model in Figure 9.8a is a “π” model in which the resistance and inductance is placed between the split capacitance. The interconnect model in Figure 9.8b is a “T” model in which the capacitance is placed between the split resistance and inductance. As discussed in Section 9.3.1, we will adopt a similar lumped modeling approach to the capacitances at work within the MOSFET.

From the preceding discussion it might appear that capacitors and inductors appear only as parasitics in circuits, causing undesirable delays. This is far from the truth. While they can and do act in that role, they are also often purposefully introduced into circuits, both as discrete devices on breadboards and printed-circuit boards, and as integrated-circuit components on a chip (see Figures 9.9 and 9.10 for examples of capacitors and inductors, respectively). For example, they are the cornerstones of memories, filters, samplers, and energy processing circuits. We shall see many examples of these in future chapters as well. Thus, we have many reasons to study capacitors and inductors.

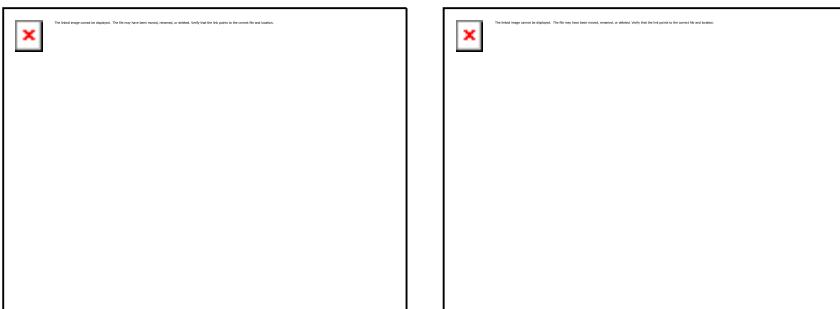


FIGURE 9.9 Examples of discrete capacitors (left) and integrated-circuit capacitors (right). The image on the right shows a small region of the Maxim MAX1062 analog-to-digital converter chip and depicts an array of polysilicon-to-polysilicon capacitors, each measuring $15.9\mu\text{m}$ by $15.9\mu\text{m}$. (Photograph Courtesy of Maxim Integrated Products.)

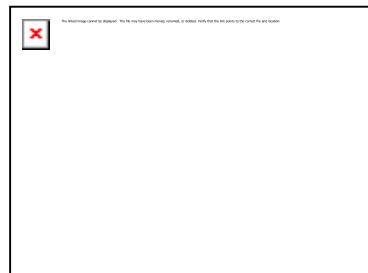


FIGURE 9.10 Examples of discrete inductors. (Photograph Courtesy of Maxim Integrated Products.)

9.1 CONSTITUTIVE LAWS

In this section, we formally introduce the capacitor and inductor in the abstract, and develop the constitutive laws that relate their branch variables. Capacitors and inductors, which are the electric and magnetic duals of each other, differ from resistors in several significant ways. Most importantly, their branch variables do not depend algebraically upon one another. Rather, their relations involve temporal derivatives and integrals. Thus, the analysis of circuits containing capacitors and inductors involves differential equations in time. To emphasize this, we will explicitly show the time dependence of all variables in this chapter.

9.1.1 CAPACITORS

To understand the behavior of a capacitor, and to illustrate the manner in which a lumped model can be developed for it, consider the idealized two-terminal linear capacitor shown in Figure 9.11. In this capacitor, each terminal is connected to a conducting plate. The two plates are parallel and are separated by a gap of length l . Their area of overlap is A . Note that these dimensions will be functions of time if the geometry of the capacitor varies. The gap is filled with an insulating linear dielectric having permittivity ϵ .

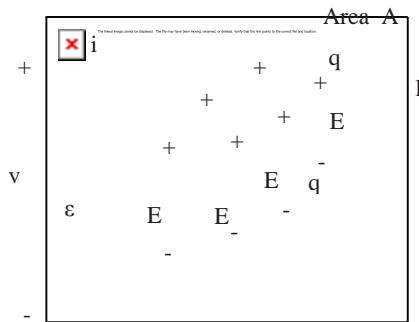


FIGURE 9.11 An idealized parallel-plate capacitor.

As current enters the positive terminal of the capacitor, it transports the electric charge q onto the corresponding plate; the unit of charge is the Coulomb [C]. Simultaneously, an identical current exits the negative terminal and transports an equal charge off the other plate. Thus, although charge is separated within the capacitor, no net charge accumulates within it, as is required for lumped circuit elements by the lumped matter discipline discussed in Chapter 1.

The produce charge an electric on the positive field within plate the and dielectric. its image I

t charge follows $-q$ from the Maxwell's negative

Equations and the properties of linear dielectrics that the strength E of this field is

$$E(t) = \frac{q(t)}{A(t)}, \quad (9.1)$$

and its direction points from the positive plate to the negative plate. The electric field can then be integrated across the dielectric from the positive plate to the negative plate to yield

$$v(t) = l(t)E(t). \quad (9.2)$$

Combining Equations 9.1 and 9.2 then results in

$$q(t) = A(t)v(t). \quad (9.3)$$

$$l(t)$$

We define

$$\underline{\underline{C}(t)} = \frac{A(t)}{l(t)} \quad (9.4)$$

where C is the capacitance of the capacitor having the units of Coulombs/Volt, or Farads [F]. Substituting for the capacitance in Equation 9.3, we get

$$q(t) = C(t)v(t). \quad (9.5)$$

9.1 Constitutive Laws

$$\frac{dq}{dt} = it$$

$$it = \frac{dCvt}{dt}$$

$$qt = Cvt$$

$$it = Cdv \frac{dt}{dt}$$

with the latter being the element law for a linear time-invariant capacitor.

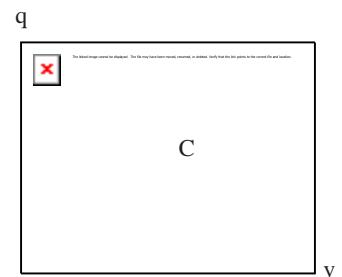
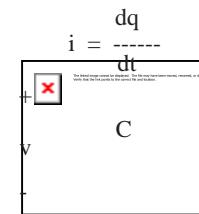


FIGURE 9.12

$$i = Cdv \frac{dt}{dt}$$

d

$$q = K \psi_0 - \psi_0 - v$$

v-

element in all integrated circuits. To see this property, we integrate Equation 9.6 to produce

$$q(t) = \int_{-\infty}^t i(t) dt \quad (9.11)$$

or, with the substitution of Equation 9.8, to produce

$$v(t) = C_1 + \int_{-\infty}^t i(t) dt. \quad (9.12)$$

Equation 9.12 shows that the branch voltage of a capacitor depends on the entire past history of its branch current, which is the essence of memory. This is in marked contrast to a resistor (either linear or nonlinear), which exhibits no such memory property.

At first glance, it might appear that it is necessary to know the entire history of the current in detail in order to carry out the integrals in Equations 9.11 and 9.12. This is actually not the case. For example, consider rewriting Equation 9.11 as

$$\begin{aligned} q(t_2) &= \int_{-\infty}^{t_2} i(t) dt \\ &= \int_{-\infty}^{t_2} i(t) dt + \int_{t_1}^{t_2} i(t) dt \\ &= i(t_1) dt + \int_{-\infty}^{t_1} i(t) dt \\ &= i(t_1) dt + q(t_1). \end{aligned} \quad (9.13)$$

The latter equality shows that $q(t_1)$ perfectly summarizes, or memorizes, the entire accumulated history of $i(t)$ for $t \leq t_1$. Thus, if $q(t_1)$ is known, it is necessary and sufficient to know only over the interval $t_1 \leq t \leq t_2$ in order to determine $q(t_2)$. For this reason, q is referred to as the state of the capacitor. For linear time-invariant capacitors, v can also easily serve as a state because v is proportionally related to q through the constant C . Accordingly, we can rewrite Equation 9.12 as

$$\begin{aligned} v(t_2) &= \frac{1}{C} \int_{-\infty}^{t_2} i(t) dt \\ &= \frac{1}{C} \left[t_1 i(t_1) dt + C_1 - \int_{-\infty}^{t_1} i(t) dt \right] \\ &= \frac{1}{C} \int_{t_1}^{t_2} i(t) dt + v(t_1). \end{aligned} \quad (9.14)$$

Thus, we see that $v(t)$ also memorizes the entire accumulated history of $i(t)$ for $t \leq t_1$ and can serve as the state of the capacitor.

Associated with the ability to exhibit memory is the property of energy storage, which is often exploited by circuits that process energy. To determine the electric energy W_E stored in a capacitor, we recognize that the power v is the rate at which energy is delivered to the capacitor through its port. Thus,

$$\frac{dW_E(t)}{dt} = i(t)v(t). \quad (9.15)$$

Next, substitute for i using Equation 9.6, cancel the time differentials, and omit the parametric time dependence to obtain

$$dW_E = v dq. \quad (9.16)$$

Equation 9.16 is a statement of incremental energy storage within the capacitor. It states that the transport of the incremental charged q from the negative plate of the capacitor to the top plate across the electric potential difference v stores the incremental energy dW_E within the capacitor. To obtain the total stored electric energy, we must integrate Equation 9.16 with v treated as a function of q . This yields

$$W_E = \int_{q_1}^{q_2} v(q) dq \quad (9.17)$$

where x is a dummy variable of integration. Finally, substitution of Equation 9.8 and integration yields

$$\frac{q_2(t)}{2C} - \frac{q_1(t)}{2C} = \frac{Cv(t)}{2} \quad (9.18)$$

as the electric energy stored in a capacitor. The unit of energy is the Joule [J], or Watt-second. Unlike a resistor, a capacitor stores energy rather than dissipates it.

Capacitors come in an enormous range of values. For example, two pieces of insulated wire about an inch long, when twisted together, will have a capacitance of about 1 picofarad (10^{-12} farads). A low-voltage power supply capacitor an inch in diameter and a few inches long could have a capacitance of 100,000 microfarads (0.1 farad; 1 microfarad, abbreviated as μF , is $10^{-6} F$).

A real capacitor can exhibit richer behavior than that described here. For example, leakage current can flow through its dielectric. The practical significance of dielectric leakage is that eventually the charge stored on a capacitor can leak off. Thus, eventually a real capacitor will lose its memory. Fortunately, capacitors can be made with very low leakage (in other words, with very high resistance) in which case they are excellent long-term memory devices. However, if the dielectric leakage is large enough to be significant, then it can be modeled with a resistor in parallel with the capacitor.

Other non-idealities include the distributed series resistance, and even series inductance, that arises in foil-wound capacitors in particular. These characteristics limit the power-handling capability of a real capacitor, and the frequency range over which a real capacitor behaves like an ideal capacitor. They can often be explicitly modeled with a single series resistor and inductor, respectively.

example 9.1 parallel plate capacitor

Suppose the parallel-plate capacitor in Figure 9.11 is 1 m square, has a gap separation of 1 μm , and is filled with a dielectric having permittivity of 2° , where $\approx 8.854 \times 10^{-12} \text{ F/m}$ is the permittivity of free space. What is its capacitance? How much charge and energy does it store if its terminal voltage is 100 V?

The capacitance is determined from Equation 9.4 with $= 1.8 \times 10^{-11} \text{ F/m}$, $A = 1 \text{ m}^2$ and $= 10^{-6} \text{ m}$. It is $18 \mu\text{F}$. The charge is determined from Equation 9.8 with $v = 100 \text{ V}$. It is 1.8 mC . Finally, the stored energy is determined from Equation 9.18. It is 90 mJ .

9.1.2 INDUCTORS

As we saw in Section 9.1.1, from the perspective of modeling electrical systems, the capacitor is a circuit element to model the effect of electric fields. Correspondingly, the inductor models the effect of magnetic fields. To understand the behavior of an inductor, and to illustrate the manner in which a lumped model can be developed for it, consider the idealized two-terminal linear inductor shown in Figure 9.13. In this inductor a coil with N turns alone each end is wound with N turns around a toroidal core made from an insulator having magnetic permeability μ . The length around the core is l and its cross-sectional area is A . Note that these dimensions will be functions of time if the geometry of the inductor varies.

The current in the coil produces a magnetic flux in the inductor. Ideally, this magnetic flux does not stray significantly from the core, so that the flux outside

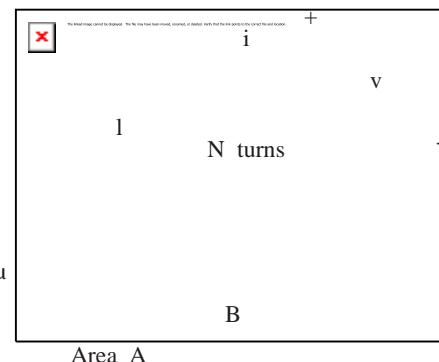


FIGURE 9.13 An idealized toroidal inductor.

the element is negligible. Thus the inductor can be treated as a lumped circuit element that satisfies the lumped matter discipline discussed in Chapter 1. From Maxwell's Equations and the properties of permeable materials, the density B of the flux is

$$B(t) = \frac{\mu N i(t)}{l(t)} \quad (9.19)$$

and its direction is around the core. The magnetic flux density can be integrated across the core to yield

$$(t) = A(t)B(t) \quad (9.20)$$

where λ is the total flux passing through the core, and hence through one turn of the coil. Since the flux is linked N times by the N -turn coil, the total flux linked by the coil is

$$\lambda(t) = N(t) = N A(t) B(t). \quad (9.21)$$

The unit of flux linkage is the Weber [Wb]. Combining Equations 9.19 and 9.21 results in

$$\lambda(t) = \frac{\mu N}{l(t)} A(t) i(t). \quad (9.22)$$

We define L , the inductance of the inductor, as

$$\underline{L(t) = \frac{\mu N^2}{l(t)} A(t)}. \quad (9.23)$$

L has the units of Webers/Ampere, or Henrys [H]. That is, inductance is the number of flux linkages per ampere. Substituting for L in Equation 9.22 we obtain the following relation for the total flux linked by the inductor

$$\lambda(t) = L(t) i(t). \quad (9.24)$$

In contrast to the resistor, which exhibits an algebraic relation between its branch current and voltage, the inductor does not. Rather, like the capacitor, it exhibits an algebraic relation between its branch current and its flux linkage. Had the core not been magnetically linear, this relation would have been nonlinear. While most inductors exhibit such nonlinear behavior for sufficiently high B , we will focus only on linear inductors.

Again from Maxwell's Equations, the rate at which flux linkage builds up in the inductor is

$$\frac{d\lambda(t)}{dt} = v(t). \quad (9.25)$$

From Equation 9.25 we see that the Volt is equivalent to a Weber/second. Equation 9.25 can be combined with Equation 9.24 to yield

$$v(t) = \frac{d(L(t)i(t))}{dt} \quad (9.26)$$

which is the element law for an ideal linear inductor. For time-invariant inductors, Equations 9.24 and 9.26 reduce to

$$\lambda(t) = L i(t) \quad (9.27)$$

$$v(t) = L \frac{di(t)}{dt}, \quad (9.28)$$

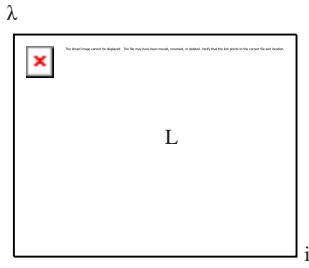


FIGURE 9.14 The symbol and current-flux-linkage relation for an ideal linear inductor. The element law for an inductor is $v = L di/dt$.

respectively, with the latter being the element law for a linear time-invariant inductor. This text will focus primarily on linear time-invariant inductors. Nonetheless, many interesting transducers such as motors, generators, and other magnetic sensors and actuators, are appropriately modeled with time-varying inductors.

The symbol for an ideal linear inductor is shown in Figure 9.14. It is chosen to represent the coil that winds the inductor shown in Figure 9.13. Also shown in Figure 9.14 is a graph of the relation between the branch current and flux linkage of the inductor.

One of the important properties of an inductor is its memory property. To see this property, we integrate Equation 9.25 to produce

$$\lambda(t) = \int_{-\infty}^t v(t) dt \quad (9.29)$$

or, with the substitution of Equation 9.27, to produce

$$i(t) = L \int_{-\infty}^t \frac{v(t) dt}{L} \quad (9.30)$$

Equation 9.30 shows that the branch current of an inductor depends on the entire past history of its branch voltage, which is the essence of memory. As for the capacitor, this is in marked contrast to an ideal resistor, which exhibits no such memory property.

At first glance, it might appear that it is necessary to know the entire history of the voltage in detail in order to carry out the integrals in Equations 9.29 and 9.30. Again as for the capacitor, this is actually not the case. For example,

consider rewriting Equation 9.29 as

$$\begin{aligned}
 \lambda(t_2) &= \int_{-\infty}^{t_2} v(t) dt \\
 &= v(t) dt + \int_{-\infty}^{t_1} v(t) dt \\
 &= v(t) dt + \lambda(t_1).
 \end{aligned} \tag{9.31}$$

The latter equality shows that $\lambda(t)$ perfectly summarizes, or memorizes, the entire accumulated history of $v(t)$ for $t \leq t_1$. Thus, if $\lambda(t_1)$ is known, it is

necessary and sufficient to know v only over the interval $t_1 \leq t \leq t_2$ in order to determine $\lambda(t_2)$. For this reason, λ , the total flux linked by the coil, is referred to as the state of the inductor. For linear time-invariant inductors, i can also easily serve as a state because it is proportionally related to λ through the constant L .

Accordingly, we can rewrite Equation 9.30 as

$$\begin{aligned}
 i(t_2) &= \frac{1}{L} \int_{-\infty}^{t_2} v(t) dt \\
 &= \frac{1}{L} \int_{t_1}^{t_2} v(t) dt + \frac{1}{L} \int_{-\infty}^{t_1} v(t) dt \\
 &= \frac{1}{L} \int_{t_1}^{t_2} v(t) dt + i(t_1).
 \end{aligned} \tag{9.32}$$

Equation 9.32 shows that i can also serve as the state of an inductor.

As with the capacitor, associated with the ability to exhibit memory is the property of energy storage, which is often exploited by circuits that process energy. To determine the magnetic energy stored in an inductor, we recognize that the power is the rate at which energy is delivered to the inductor through its port. Thus,

$$dW_M(t) = i(t)v(t). \tag{9.33}$$

Next, substitute for v using Equation 9.25, cancel the time differentials, and omit the parametric time dependence to obtain

$$dW_M = id\lambda. \tag{9.34}$$

Equation 9.34 is a statement of incremental energy storage within the inductor. To obtain the total stored magnetic energy, we must integrate Equation 9.34

with it treated as a function of λ . This yields

$$w_M = \int_{-L}^{L} i(x) dx \quad (9.35)$$

where x is a dummy variable of integration. Finally, substitution of Equation 9.27 and integration yields

$$\text{Stored energy} = w_M(t) = \frac{\lambda_2(t)}{2L} = \frac{L_i(t)^2}{2} \quad (9.36)$$

as the magnetic energy stored in an inductor. Unlike a resistor, but like a capacitor, an inductor stores energy rather than dissipates it.

A real inductor exhibits richer behavior than that described here. For example, it can exhibit significant coil resistance. The practical significance of this resistance is that it eventually dissipates any energy stored in the inductor. Unfortunately, this resistance is usually significant so that inductors make poor memory devices. When it is necessary to model this energy loss, the coil resistance can be modeled as a resistor in series with the ideal inductor.

Other non-idealities include core loss and inter-turn capacitance. These characteristics limit the power-handling efficiency of a real inductor, and the frequency range over which a real inductor behaves like an ideal inductor. They can often be modeled with a parallel resistor and capacitor, respectively.

example 9.2 toroidal inductor Suppose the toroidal inductor in Figure 9.13 has a cross-sectional area of 1 cm^2 , has a length around its toroid of 10 cm , has a coil with 100 turns, and is filled with free space having permeability $\mu_0 = 4\pi \times 10^{-7}\text{ H/m}$. What is its inductance? How much flux does its coil link, and what energy does it store if its terminal current is 0.1 A ?

The inductance is determined from Equation 9.23 with $\mu = 4\pi \times 10^{-7}\text{ H/m}$, $A = 10^{-4}\text{ m}^2$, $l = 0.1\text{ m}$ and $N = 100$. It is $13\mu\text{H}$. The flux linkage is determined from Equation 9.24 with $i = 0.1\text{ A}$. It is $1.3\mu\text{Wb}$. Finally, the stored energy is determined from Equation 9.36. It is $0.063\mu\text{J}$.

9.2 SERIES AND PARALLEL CONNECTIONS

In Section 2.3.4, we saw that the resistances of resistors in series add, and that the conductances of resistors in parallel add. Thus, series and parallel resistors could be represented as a single resistor with an appropriate resistance. These addition rules later became useful as a means of simplifying circuits and their analyses. As we shall see in this section, similar rules may be derived for both capacitors and inductors, and these rules are equally useful.

9.2.1 CAPACITORS

Consider first the series combination of two capacitors as shown in Figure 9.15; we will assume here that the two capacitors were uncharged at the time of their connection. Since the two capacitors share a common current, it follows from Equation 9.11 that they store a common charge q , as shown in Figure 9.15. Thus, following Equation 9.8,

$$\underline{q(t) = C_1 v_1(t) = C_2 v_2(t)}. \quad (9.37)$$

Next, using KVL we observe that

$$v(t) = v_1(t) + v_2(t). \quad (9.38)$$

Finally, since the effective capacitance C of the two series capacitors is q/v , it follows that

$$\frac{1}{C} = \frac{v(t)}{q(t)} = C_1^{-1} + C_2^{-1},$$

or,

$$\underline{C = \frac{C_1 C_2}{C_1 + C_2}} \quad (9.39)$$

where the second equality results from the substitution of Equation 9.38 and then Equation 9.37. Thus, we see that the reciprocal capacitances of capacitors in series add. This is consistent with the physical derivation of capacitance in Equation 9.4 since placing capacitors in series essentially increases their combined gap length.

Now consider the parallel combination of two capacitors as shown in Figure 9.16. Since the two capacitors share a common voltage v , it follows from 9.8 that

$$v(t) = \frac{q_1(t)}{C_1} = \frac{q_2(t)}{C_2} \quad (9.40)$$

Next, using KCL and Equation 9.11 we observe that

$$q(t) = q_1(t) + q_2(t). \quad (9.41)$$

Finally, since the effective capacitance C of the two parallel capacitors is q/v , it follows that

$$\underline{C = \frac{q(t)}{v(t)} = \frac{1}{C_1} + \frac{1}{C_2}} \quad (9.42)$$

where the second equality results from the substitution of Equation 9.41 and then Equation 9.40. Thus, we see that the capacitances of capacitors

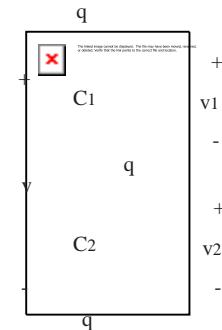


FIGURE 9.15 Two capacitors in series.

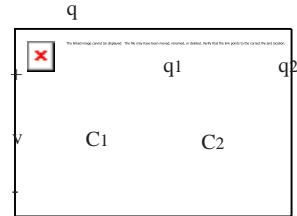


FIGURE 9.16 Two capacitors in parallel.

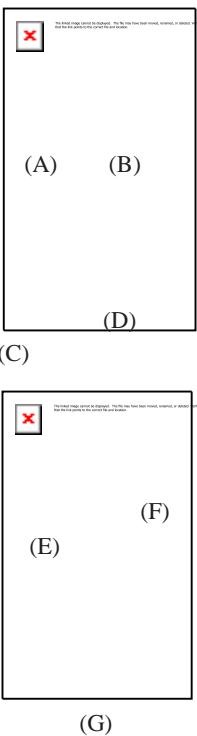


FIGURE 9.17 Various combinations of capacitors involving up to three capacitors.

in parallel add. This is inconsistent with the physical derivation of capacitance in Equation 9.4 since placing capacitors in parallel essentially increases their combined cross-sectional area.

example 9.3 capacitor combinations What equivalent capacitors can be made by combining up to three $1\text{-}\mu\text{F}$ capacitors in series and/or in parallel?

Figure 9.17 shows the possible capacitor combinations that use up to three capacitors. To determine their equivalent capacitances, use the series combination result from Equation 9.39 and/or the parallel combination result from Equation 9.42. This yields the equivalent capacitances of: (A) $1\text{-}\mu\text{F}$, (B) $2\text{-}\mu\text{F}$, (C) $0.5\text{-}\mu\text{F}$, (D) $3\text{-}\mu\text{F}$, (E) $1.5\text{-}\mu\text{F}$, (F) $0.667\text{-}\mu\text{F}$, and (G) $0.333\text{-}\mu\text{F}$.

9.2.2 INDUCTORS

Consider the series combination of two inductors as shown in Figure 9.18; we will assume here that neither inductor carries a current at the time of their connection. Since the two inductors share a common current, it follows from Equation 9.27 that

$$i(t) = \frac{\lambda_1(t)}{L_1} = \frac{\lambda_2(t)}{L_2} \quad (9.43)$$

Next, using KV and Equation 9.29 we observe that

$$\lambda(t) = \lambda_1(t) + \lambda_2(t). \quad (9.44)$$

Finally, since the effective inductance L of the two series inductors is λ/i , it follows that

$$L = \frac{\lambda(t)}{i(t)} = L_1 + L_2 \quad (9.45)$$

where the second equality results from the substitution of Equation 9.44 and then Equation 9.43. Thus, we see that the inductances of inductors in series add. This is consistent with the physical derivation of inductance in Equation 9.23 since placing inductors in series essentially increases the total length of core around which the parallel turns are wound.

Now consider the parallel combination of two inductors as shown in Figure 9.19. Since the two inductors share a common voltage, it follows from Equation 9.29 that they share a common flux linkage λ , as shown in Figure 9.19. Thus, following Equation 9.27,

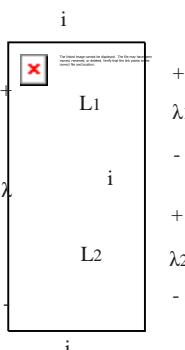


FIGURE 9.18 Two inductors in series.

$$\lambda(t) = L_1 i_1(t) = L_2 i_2(t). \quad (9.46)$$

Next, using KCL we observe that

$$i(t) = i_1(t) + i_2(t). \quad (9.47)$$

Finally, since the effective inductance L of the two parallel inductors is λ/i , it follows that

$$\frac{1}{L} = \frac{i(t)}{\lambda(t)} = \frac{1}{L_1} + \frac{1}{L_2},$$

or,

$$L = \frac{L_1 L_2}{L_1 + L_2} \quad (9.48)$$

where these equality results from the substitution of Equation 9.47 and then Equation 9.46. Thus, we see that the reciprocal inductances of inductors in parallel add. This is consistent with the physical derivation of inductance in Equation 9.23 since placing inductors in parallel essentially increases the cross-sectional area of the core around which the turns are wound.

example 9.4 inductor combinations What equivalent inductors can be made by combining up to three 1- μ H inductors in series and/or in parallel?

Figure 9.20 shows the possible inductor combinations that use up to three inductors. To determine their equivalent inductances, use the series combination result from Equation 9.45 and/or the parallel combination result from Equation 9.48. This yields the equivalent inductances of: (A) 1 μ H, (B) 0.5 μ H, (C) 2 μ H, (D) 0.333 μ H, (E) 0.667 μ H, (F) 1.5 μ H, and (G) 3 μ H.

9.3 SPECIAL EXAMPLES

In this section, we examine several parasitic capacitances and inductances that are commonly encountered inside integrated circuits, and in external wiring connections to them and other circuit elements. There is again the danger that this discussion implies that capacitors and inductors appear most commonly as parasitics in circuits. This is certainly not the case. Rather, we examine the parasitics here primarily for interest sake, and because they will provide interesting and important circuit examples in future chapters.

9.3.1 MOSFET GATE CAPACITANCE

Let us now take a closer look at the structure and operation of the MOSFET in order to better understand its dynamic behavior. Figure 9.21 reviews the

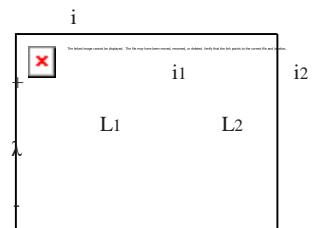


FIGURE 9.19 Two inductors in parallel.

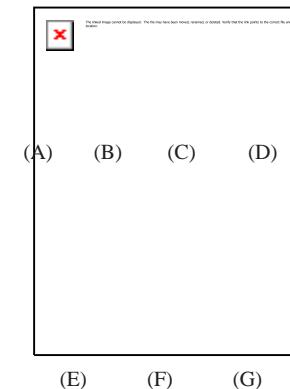


FIGURE 9.20 Various combinations of inductors involving up to three inductors.

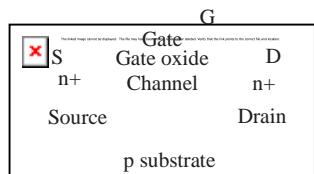


FIGURE 9.21 MOSFET structure.

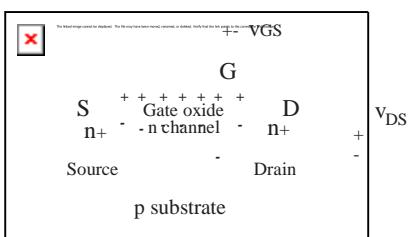


FIGURE 9.22 MOSFET with a positive voltage applied at the gate relative to the source and substrate.

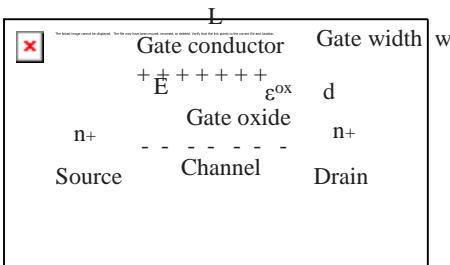


FIGURE 9.23 Electric charge and field within the MOSFET with a positive voltage applied at the gate relative to the source and substrate.

structure of the n-channel MOSFET. The figure identifies its n+-type source and drain, its p-type substrate, its channel region, its gate conductor, and the silicon dioxide dielectric that separates its gate and channel.

Figure 9.22 shows the same n-channel MOSFET with its source and substrate grounded, and positive voltages applied to its gate and drain. As the positive gate voltage is applied, electrons flow from the source into the channel and accumulate beneath the gate. When the gate voltage exceeds the threshold voltage of the MOSFET, the electron density beneath the gate becomes sufficiently high to invert the channel from p-type silicon to n-type silicon. Thus, a continuous n-type channel forms between the source and drain, thereby allowing electrons to flow from the source to the drain, and hence current to flow from the drain to the source, in response to the positive drain voltage.

The important observation here from Figure 9.22 is that in the process of inverting its channel, and turning it self on, the MOSFET actually forms a parallel-plate capacitor between its gate and channel. This is emphasized in Figure 9.23, which shows the electric field E in the silicon dioxide emanating from the positive charge on the gate and terminating on the negative charge in the channel. Comparing this figure to Figure 9.11 leads to the realization (from Equation 9.4) that the gate-to-channel capacitance is approximately

$$\frac{\epsilon_0 L W}{d}$$

where $\epsilon_0 \approx 3.9$ is the permittivity of the silicon dioxide, d is the thickness of the silicon dioxide, L is the channel length, and W is the channel width. The product LW is the gate area.

Since the electrons that fill the channel originate from the source, and since their image charges reside on the gate, the gate-to-channel capacitance that we identified in Figures 9.22 and 9.23 appears between the gate and source

of the MOSFET when viewed from the MOSFET terminals. For this reason the capacitance is usually referred to as the gate-to-source capacitance of the MOSFET, or C_{GS} . In other words,

$$\frac{C_{GS}}{d} = \frac{\text{oxLW.}}{d} \quad (9.49)$$

Often, the ratio ox/d is referred to as C_{ox} , the gate-to-channel capacitance per unit area of the MOSFET gate. In other words,

$$C_{ox} = \frac{\text{ox}}{d}$$

This realization also leads to the augmented switch-resistor-capacitor (SRC) model of the MOSFET shown in Figure 9.24. Here, a lumped capacitor is added to the SR model to account for the charge that must be supplied to the gate conductor and channel in order to turn on the MOSFET. Thus, we develop a model that describes the behavior of the MOSFET yet satisfies the lumped matter discipline.

Because the SRC model contains a capacitor between the gate and source terminals of the MOSFET, a current will flow into the gate terminal and out from the source terminal of that model as the gate-to-source voltage of the MOSFET varies. This current transports the charge that accumulates within the MOSFET as seen in Figures 9.22 and 9.23. Following Equation 9.9, the current is given by

$$i_G = C_{GS} \frac{dv_{GS}}{dt} \quad (9.50)$$

where

$$C_{GS} = C_{ox} L W. \quad (9.51)$$

From Equation 9.50 we can now begin to see the reason for the inverter behavior observed in Figure 9.3. It will take time for the gate current to transport charge onto the gate, and hence it will take time for the gate voltage to rise. Thus, it will take time for the inverter to pass a signal from its input to its output. We will have more to say about this in Section 10.4.

Finally, it is important to realize that the dynamic behavior of a real MOSFET is actually much more complex than described here. In reality a MOSFET actually has many internal capacitances of importance, including capacitances between its gate and drain, its gate and source, its gate and substrate, its drain and source, its drain and substrate, and its source and substrate. Further, most of these capacitances are actually functions of v_{GS} and v_{DS} . For our purposes, we will work primarily with C_{GS} and assume that it is a constant capacitance.

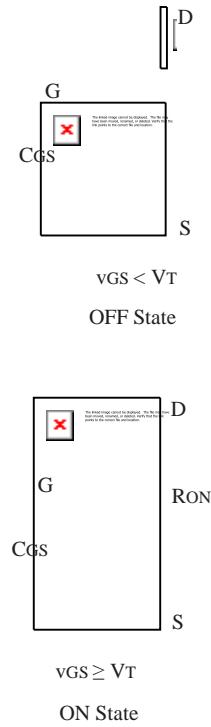
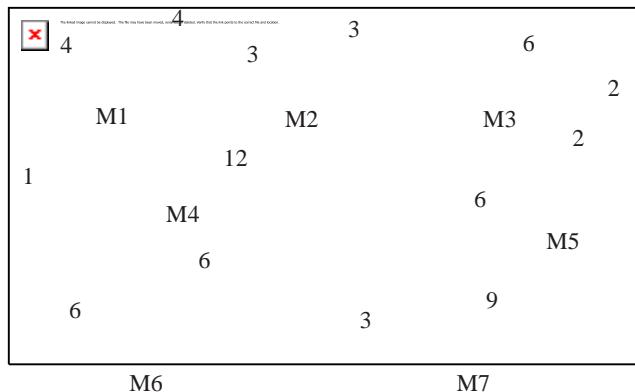


FIGURE 9.24 The switch-resistor-capacitor (SRC) model of the MOSFET.

FIGURE 9.25 MOSFETgates withdifferentdimensions;all dimensionsinthefigurearein μm .



example 9.5 gate capacitances of mosfets Figure9.25

shows the top view of several rectangular MOSFET gates fabricated within an integrated circuit. Let us assume that the silicon-dioxide dielectric is characterized by $C_{ox} \approx 4\text{fF}/\mu\text{m}^2$, and find the gate capacitances C_{gs} for each MOSFET.

To do so, we use Equation 9.51. To begin, notice that MOSFETs M3, M4, and M5 must have the same capacitance because they have the same area of $12\ \mu\text{m}^2$. Their capacitance is therefore 48fF . MOSFET M5 has the biggest area of $36\mu\text{m}^2$, and so it has the biggest capacitance of 144fF , while MOSFET M2 has the smallest area of $9\mu\text{m}^2$, and so it has the smallest capacitance of 36fF . MOSFETs M1 and M7 have capacitances 64fF and 108fF , respectively.

9.3.2 WIRING LOOP INDUCTANCE

The most common parasitic inductance is the inductance associated with a wiring loop. In the lumped circuit abstraction, this inductance is ignored unless it is explicitly modeled in a circuit using an additional lumped inductor. To estimate the inductance of a wiring loop, consider the circular loop of wire in free space shown in Figure 9.26. The loop has a loop radius R and a wire radius A . Its inductance L is given approximately by²

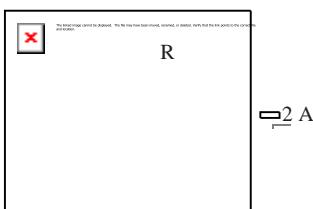


FIGURE 9.26 Awiringloop.

$$L = \mu_0 R \ln(8R/A) - 2 . \quad (9.52)$$

This expression can also be used to successfully approximate the inductance of many noncircular wiring loops.

²See Ramo, Whinnery, and Van Duzer, *Fields and Waves in Communication Electronics*, P.311, John Wiley, 1965.

example 9.6 inductance of a wiring loop

Suppose a wiring loop in free space has a 5-mm diameter and is made from 200- μm -thick wire. What is its inductance?

Using Equation 9.52 with $R = 2.5 \times 10^{-3}\text{ m}$, $A = 10^{-4}\text{ m}^2$, and $\mu_0 = 4\pi \times 10^{-7}\text{ H/m}$, the inductance is found to be 10 nH.

9.3.3 IC WIRING CAPACITANCE AND INDUCTANCE

Let us now return to Figure 9.4, and develop a model for the capacitance and inductance of the conductors inside an integrated circuit (IC) that are implied by the figure. Many conductors inside integrated circuits can be modeled as a flat conductor above a conducting substrate, or ground plane, as shown in Figure 9.27.

The conductor in the figure has a width W , and it is located the distance G above the ground plane. Such conductors are typically surrounded by an insulating dielectric having a permittivity of ϵ and a permeability of μ_0 .

Under the assumption that $W \ll G$, we can ignore the fringing electric and magnetic fields at the edges of the conductor. In this case, the capacitance $C \sim \epsilon / G$ and inductance $L \sim \mu_0 W G$ of the conductor per unit length along its length is approximately

$$C \sim \frac{W}{G} \quad (9.53)$$

$$L \sim \mu_0 W G. \quad (9.54)$$

In other cases, however, the width of the conductor is not large compared to its elevation above the ground plane. An example of this is an arrow printed circuit board trace. In such cases the conductor might alternatively be modeled as a cylindrical conductor above a ground plane as shown in Figure 9.28.

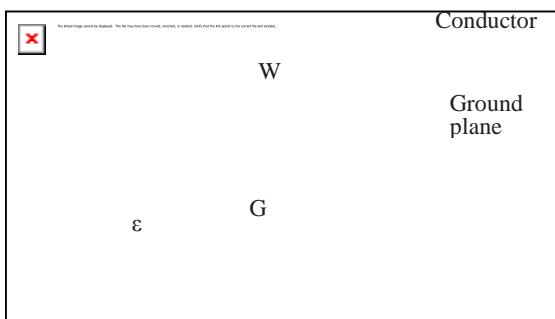


FIGURE 9.27 A flat conductor above a conducting ground plane.

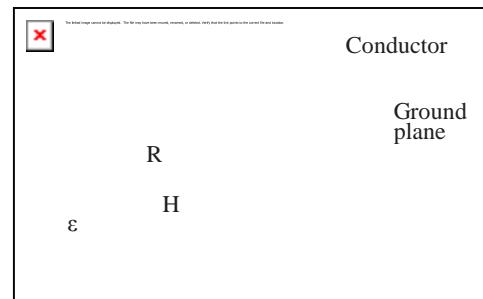


FIGURE 9.28 A cylindrical conductor above a conducting ground plane.

The conductor in Figure 9.28 has a radius R and is centered at the distance H above the ground plane. It has a capacitance C^\sim and inductance L^\sim per unit length of approximately

$$C^\sim = \frac{2\pi}{\ln \frac{H}{R} + \frac{H^2}{R^2} - 1} \quad (9.55)$$

$$L^\sim = \frac{\mu_0}{2\pi} \frac{H}{\ln \frac{H}{R} + \frac{H^2}{R^2} - 1} \quad (9.56)$$

along its length. Together, the conductors shown in Figures 9.27 and 9.28 can be used to model a wide variety of interconnects.

Finally, notice that for both interconnects,

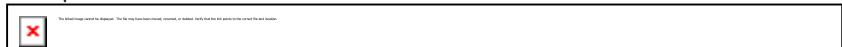
$$CL^\sim = \mu_0.$$

It follows from Maxwell's Equations that this will always be the case for any two-wire interconnect having constant cross section along its length. Thus, any effort to reduce either C or L will result in an increase of the other.

example 9.7 capacitance of integrated-circuit

interconnect Consider an integrated-circuit interconnect, such as the one shown in Figure 9.27, with $W = 2 \mu\text{m}$, $G = 0.1 \mu\text{m}$, and $\theta = 3.9^\circ$. What is its capacitance and inductance per unit length?

Using Equations 9.53 and 9.54, $C^\sim = 690 \text{ pF/m} = 0.69 \text{ fF}/\mu\text{m}$, and $L^\sim = 63 \text{ nH/m} = 63 \text{ fH}/\mu\text{m}$.



example 9.8 printed-circuit-board trace

Consider modeling a printed-circuit-board trace as a cylindrical conductor above a ground plane, as shown in Figure 9.28. Let $R = 0.5 \text{ mm}$, $H = 2 \text{ mm}$, and $\theta = 0^\circ$. What is its capacitance and inductance per unit length?

Using Equations 9.55 and 9.56, $C^\sim = 27 \text{ pF/m}$, and $L^\sim = 410 \text{ nH/m}$.

9.3.4 TRANSFORMERS

A transformer is a two-port device made by winding a second coil around the inductor, for example, that shown in Figure 9.13. Let the first (or primary) coil have N_1 turns and the second (or secondary) coil have N_2 turns. The symbol for an ideal transformer having this construction is shown in Figure 9.29. The two dots indicate the ends of the two coils that are wound in the same direction.

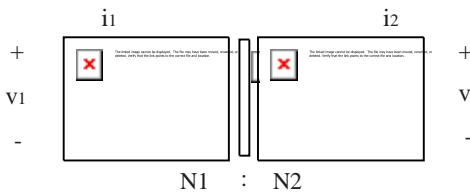


FIGURE 9.29 The symbol for an ideal transformer.

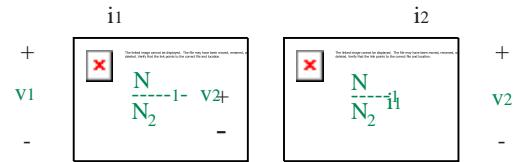


FIGURE 9.30 A useful model for an ideal transformer.

In an ideal transformer, the coils are wound so tightly against each other that each of their turns links the same flux (λ). It then follows from Equations 9.25 and 9.21 that

$$v_1 = N_1 \frac{d(\lambda)}{dt} \quad (9.57)$$

$$v_2 = N_2 \frac{d(\lambda)}{dt} \quad (9.58)$$

so that

$$\frac{v_1(t)}{N_1} = \frac{v_2(t)}{N_2} \quad (9.59)$$

In an ideal transformer, the core is also infinitely permeable, that is, $\mu = \infty$. For a single-coil inductor carrying a finite flux $\lambda(t) = \lambda(t)/N$, Equation 9.22 shows that the total ampere-turns $N_i(t)$ flowing around the core through the coil must vanish as t becomes infinite. In an ideal transformer, the total ampere-turns must similarly vanish, and so

$$N_1 i_1(t) + N_2 i_2(t) = 0 \quad (9.60)$$

or

$$N_1 i_1(t) = -N_2 i_2(t). \quad (9.61)$$

Equations 9.59 and 9.61 are the constitutive equations for an ideal transformer.

By combining Equations 9.59 and 9.61, it can be observed that

$$v_1(t) i_1(t) = -v_2(t) i_2(t). \quad (9.62)$$

Thus, the power flowing into one port of an ideal transformer must instantaneously flow out from the second port. Said differently, an ideal transformer cannot store energy. This is consistent with having an infinitely permeable core.

A very useful model for an ideal transformer is shown in Figure 9.30. This model uses two dependent voltage sources to enforce Equations 9.59 and 9.61. The voltage-dependent voltage source enforces Equation 9.59 and the current-dependent current source enforces Equation 9.61.

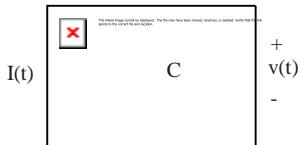


FIGURE 9.31 A current source driving a capacitor.

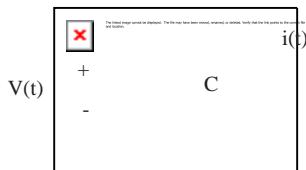


FIGURE 9.32 A voltage source driving a capacitor.

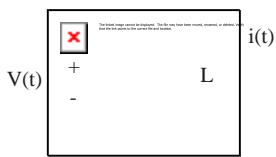


FIGURE 9.33 A voltage source driving an inductor.



FIGURE 9.34 A current source driving an inductor.

example 9.9 a transformer A transformer can be used to transform the 120-Volt rms utility voltage to a voltage that can power a 5-V DC load. To do so, what must be the approximate turns ratio of the transformer?

If the primary of the transformer is connected to the utility, then

$$v_1 = 120\sqrt{2}\sin(2\pi \cdot 60t),$$

where the frequency of the utility voltage is 60 Hz (or 60 cycles per second), or $2\pi \cdot 60$ radians per second. Thus, the primary has a peak voltage of 170 V. At the secondary, it is desired that v_2 have a peak of 5 V, and so the turns ratios should be approximately

$$N_1/N_2 = 34.$$

A real transformer designed for this application would actually have a slightly smaller turns ratio so that v_2 would ideally be somewhat larger than 5 volts. This allows for voltage drops across coil resistances and leakage inductances found in practical devices.

9.4 SIMPLE CIRCUIT EXAMPLES

To complete our introduction to capacitors and inductors, let us now examine their behavior in the simple circuits shown in Figures 9.31 through 9.34. These circuits are the same as those shown in Figures 2.25 and 2.26, except for the replacement of the resistor in the latter figures by the capacitor or inductor in the former figures. Because the two sets of circuits are so similar, we could analyze the circuits shown in Figures 9.31 through 9.34 using the same approach applied in Chapter 2 to the circuits shown in Figures 2.25 and 2.26. Alternatively, we could carry out anode analysis as developed in Section 3.3. However, since the circuit here is simple, we will follow the more intuitive approach outlined at the end of Section 2.4, and save the formalities for the analysis of more complex circuits in future chapters.

Consider first the circuit shown in Figure 9.31. In this circuit, the current from the source must circulate through the capacitor. Thus, the current through both elements is known. Next, following Equation 9.12, the voltage across the capacitor, and hence across the current source, is given by

$$v(t) = C \overline{\int_{-\infty}^t I(t) dt}. \quad (9.63)$$

All branch variables are now known.

Consider next the circuit shown in Figure 9.32. In this circuit, the voltage V from the source must also appear across the capacitor. Thus, the voltage across

both elements is known. Next, following Equation 9.9, the current i circulating through both the capacitor and the voltage source is given by

$$i(t) = C \frac{dV(t)}{dt} \quad (9.64)$$

Again, all branch variables are now known.

Now consider the circuit shown in Figure 9.33. In this circuit, the voltage V from the source must also appear across the inductor, just as it appeared across the capacitor in Figure 9.32. Thus, following Equation 9.30, the current circulating through both the inductor and the voltage source is given by

$$i(t) = L \frac{1}{t} \int_{-\infty}^t V(t) dt. \quad (9.65)$$

All branch variables are now known.

Finally, consider the circuit shown in Figure 9.34. In this circuit, the current I from the source must circulate through the inductor, just as it did through the capacitor shown in Figure 9.31. Thus, following Equation 9.28, the voltage v appearing across both the inductor and the current source is given by

$$v(t) = L dI/dt. \quad (9.66)$$

Once again, all branch variables are now known.

In the following subsections, we will consider specific examples of the source current I and source voltage V . However, before doing so, it is worth noting the similarity between the analyses of the four circuits we have just studied. Because capacitors and inductors are duals of each other, we find that the circuits are as well. For example, the circuits shown in Figures 9.31 and 9.33 are duals. Capacitance interchanges with inductance, and current interchanges with voltage, as can be seen by comparing Equations 9.63 and 9.65. Similarly, the circuits shown in Figures 9.32 and 9.34 are duals. Again, capacitance interchanges with inductance and current interchanges with voltage, as can be seen by comparing Equations 9.64 and 9.66.

It is also interesting to note that the circuits shown in Figures 9.31 through 9.34 perform either integration or differentiation of the source current or voltage as it produces the branch voltages or currents, respectively. Thus, if viewed in this way each circuit is an integrator or differentiator. We will make use of this capability of capacitors and inductors in future chapters as we build filters and other signal processing circuits.

9.4.1 SINUSOIDAL INPUTS*

9.4.2 STEP INPUTS

Step functions, and their integrals and derivatives, constitute another important class of input signals to electronic circuits. So, as an example of a step input to the circuit shown in Figure 9.31 (redrawn here as Figure 9.36 for convenience), consider the source step function:

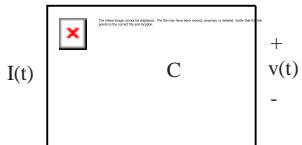


FIGURE 9.36 A current source driving a capacitor.

$$I(t)=I_0 \begin{cases} 0 & t \leq 0 \\ t & t > 0 \end{cases} \quad (9.75)$$

Note that the source is zero for $t \leq 0$, but nonzero for $t > 0$, so that it effectively turns on at $t = 0$. A sketch of the current step input is shown in Figure 9.37a.

To complete the analysis of the circuit, we substitute the corresponding source function from Equation 9.75 into Equation 9.63 and carry out the indicated integration.³ The substitution of Equation 9.75 into Equation 9.63 yields

$$v(t)=\begin{cases} 0 & t \leq 0 \\ \frac{1}{C}t & t > 0 \end{cases} \quad (9.76)$$

for the circuit shown in Figure 9.36. This result is shown in Figure 9.37b.

Let us now examine the operation of the circuit shown in Figure 9.36 more closely. Once the current source steps its value to I_0 , it begins to deliver charge to the capacitor at that constant rate. The charge then accumulates linearly in the capacitor, much like water would accumulate in a glass from a faucet set to deliver that water at a constant rate. Since charge and voltage are proportional through the constant capacitance C of the linear time-invariant capacitor, the voltage across the capacitor also increases linearly. This is as shown in Figure 9.37.

Figure 9.37 also illustrates another very important point, namely that the charge stored in, and hence the voltage appearing across, a capacitor is a continuous function of time. Even though I steps discontinuously at $t = 0$, v does not; the state q , and hence v , is continuous. The only way for v to take a discontinuous step would be for the current source to deliver a non-zero charge in zero time, which requires an infinite current. This is of course not a practical possibility, although we will see that such a mathematical construction can be used very effectively to model certain physical phenomena.

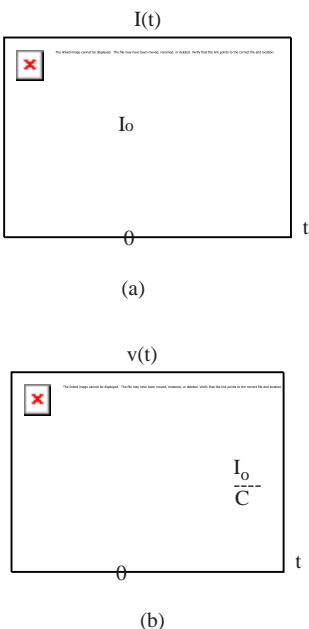


FIGURE 9.37 The current and voltage in the circuit shown in Figure 9.36.

³This is relatively easy for the integration, but as we will see shortly, it requires some thought when the circuit involves a differentiation.

The behavior seen in Figure 9.37 also begins to explain the delays seen in Figure 9.3, although as we shall see in Chapter 10 the details are slightly different. As we see in Figure 9.37, it takes time for a finite current source to charge a capacitor, and hence it raises its voltage. In the case of the two inverters shown in Figure 9.1, it takes time for the first inverter to change the voltage at the input to the second inverter. This is because it takes time for the first inverter to charge and discharge the gate-to-source capacitance of the MOSFET in the second inverter. The time it takes for this voltage to cross the threshold voltage of the MOSFET is also ultimately responsible for a delay at the output of the second inverter.

example 9.10 mosfet gate-to-source capacitance

Suppose that the gate-to-source capacitance C_{GS} for a particular MOSFET is 100 fF . What constant gate current would be required to raise the gate-to-source voltage of that MOSFET from 0 V to 5 V in 10 ns ?

This problem is well modeled by Figure 9.31 with I being a current step. Hence, Equation 9.76 and Figure 9.37 apply. Since the voltage slope is to be 5 V in 10 ns , or $5 \times 10^8\text{ V/s}$, and since the capacitance is 100 fF , the current must be $50\mu\text{A}$.

A second way to solve this problem is to use Equation 9.8 with $C = 100\text{ fF}$ and $v = 5\text{ V}$ to determine that the gate current must deliver a charge of 500 fC . Since this charge flows at a constant rate over a 10-ns period, the current must be $50\mu\text{A}$.

example 9.11 voltage step input to an inductor

As our next example, let us consider a voltage step input of the following form:

$$V(t) = V_0 \begin{cases} 0 & t \leq 0 \\ t & t > 0 \end{cases} \quad . \quad (9.77)$$

to the circuit shown in Figure 9.33 (redrawn here as Figure 9.38). The voltage step input is sketched in Figure 9.39a.

Since they are duals, the operation of the circuit in Figure 9.38 is much the same as that of the circuit in Figure 9.36. Once the voltage source steps its value to V , the current through the inductor begins to increase linearly. More formally, the substitution of Equation 9.77 into Equation 9.65 yields

$$i(t) = \begin{cases} 0 & t \leq 0 \\ \frac{V_0}{L}t & t > 0. \end{cases} \quad (9.78)$$

This is shown in Figure 9.39b.

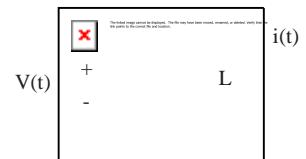
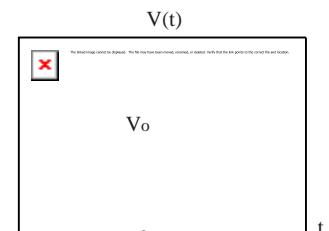
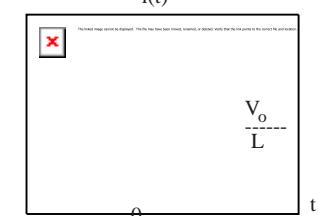


FIGURE 9.38 A voltage source driving an inductor.



(a)



(b)

FIGURE 9.39 The current and voltage in the circuit shown in Figure 9.38.

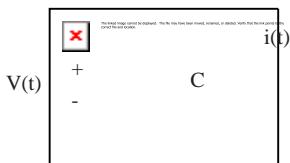


FIGURE 9.40 A voltage source driving a capacitor.

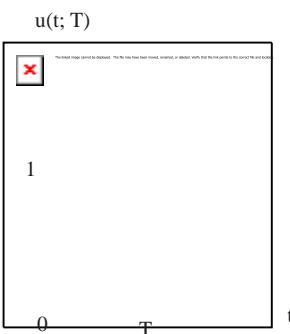


FIGURE 9.41 The ramping unit step function $u(t; T)$.

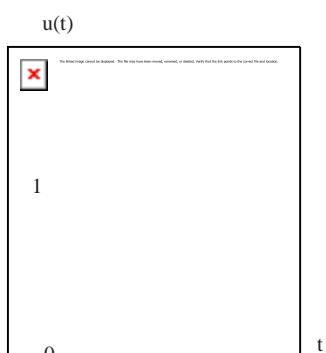


FIGURE 9.42 The unit step function $u(t)$.

Figure 9.39 also illustrates an important point, namely that the flux linked by, and hence the current through, an inductor is a continuous function of time. Even though V steps discontinuously at $t = 0$, i does not; the state λ , and hence i , is continuous. The only way for it to take a discontinuous step would be before the voltage source V deliver a non-zero flux linkage in zero time, which requires an infinite voltage. This is of course a non-physical possibility, although we will see that such a mathematical construction can also be used very effectively to model certain physical phenomena.

example 9.12 relay A relay is constructed as an electromagnet that opens and closes a mechanical switch. Suppose that the electromagnet can be modeled as an inductor having a 10-mH inductance. Suppose further that it will close the mechanical switch once its current reaches 10 mA. What voltage step must be applied to the electromagnet to close the switch in $100\mu s$?

This problem is well modeled by Figure 9.33 with V being a voltage step. Hence, Equation 9.78 and Figure 9.39 apply. Since the current's slope is to be $10\text{mA}/100\mu s$, or 100A/s , and since the inductance is 10mH , the voltage must be 1V .

A second way to solve this problem is to use Equation 9.27 with $L = 10\text{ mH}$ and $i = 10\text{ mA}$ to determine that the voltage source must deliver a flux linkage of 10^{-4}Wb . Since this flux linkage is to be delivered at a constant rate over a $100-\mu\text{s}$ period, the voltage must be 1V .

Let us now turn to the circuit shown in Figure 9.32 (redrawn here as Figure 9.40). Let us analyze its operation with a voltage source that takes a discontinuous step expressed in the following equation

$$V(t) = \begin{cases} 0 & t \leq 0 \\ V_0 & t > 0 \end{cases}. \quad (9.79)$$

and sketched in Figure 9.45a.

To analyze its operation with a source that takes a discontinuous step, we refer to Equation 9.64, and notice that we must contend with the differentiation of the step at $t = 0$. We can develop an understanding of this differentiation with the help of the ramping unit step function $u(t; T)$ defined in Figure 9.41. Here, $u(t; T)$ is a function of time, having the ramp duration T as a parameter.

Note that the ramp in $u(t; T)$, which occurs over the period $0 \leq t \leq T$, becomes increasingly steeper as the ramp width T approaches 0. In fact, it is $u(t; T)$ in the limit $T \rightarrow 0$, or simply $u(t)$, as illustrated in Figure 9.42. Notice that the ideal unit step is the function at work in Equation 9.79. Recognizing this limiting behavior, our approach to dealing with the differentiation of a step will be to take a more roundabout, but easier route: We will compute the response of the circuit to a ramping unit step function, and then take the limit as $T \rightarrow 0$.

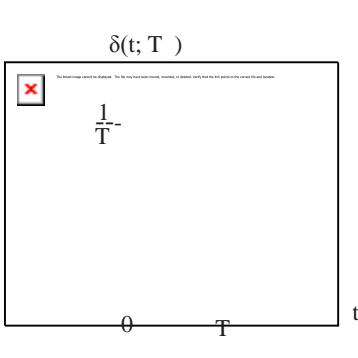


FIGURE 9.43 The unit-area pulse function $\delta(t; T)$ obtained by differentiating the ramping unit-step function $u(t; T)$.

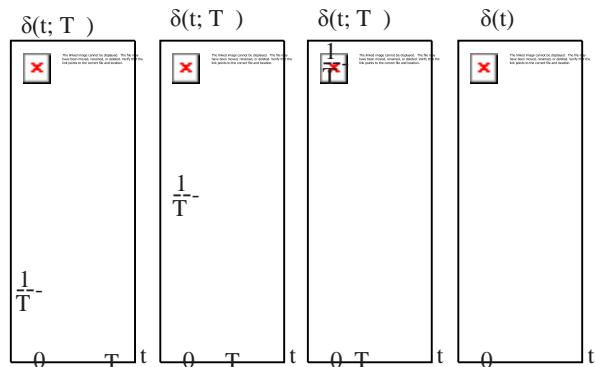


FIGURE 9.44 The unit-area pulse function becomes the unit impulse in the limit as $T \rightarrow 0$.

Thus, we can rewrite Equation 9.79 in terms of the unit step function as

$$V(t) = V \circ \lim_{T \rightarrow 0} u(t; T) \equiv V \circ u(t). \quad (9.80)$$

The ramping unit-step function $u(t; T)$ can be differentiated to yield the unit-area pulse function $\delta(t; T)$ shown in Figure 9.43. This function becomes increasingly narrow and tall as T approaches 0, but in doing so it maintains unit area, as depicted in Figure 9.44. In the limit $T \rightarrow 0$, $\delta(t; T)$ becomes the unit impulse (see the right-most graph in Figure 9.44, which we will simply denote by $\delta(t)$).

The unit impulse δ has several important properties for our purposes. These properties are

$$\delta(t) = 0 \text{ for } t = 0 \quad (9.81)$$

$$\frac{\int_{-\infty}^t \delta(t) dt = u(t)}{\delta(t) dt = u(t)} \Leftrightarrow \delta(t) = \frac{du(t)}{dt} \quad (9.82)$$

$$\int_{-\infty}^{\infty} \delta(t) dt = 1. \quad (9.83)$$

4. $u(t)$ and $\delta(t)$ are commonly used to represent the unit step function and the unit impulse function, respectively. Sometimes, the following notation is also used: $u_0(t)$ represents a unit impulse at time $t=0$. The notation $u_n(t)$ is used to represent the function that results from differentiating the impulse n times, and the notation $u^{-n}(t)$ represents the function that results from integrating the impulse n times. Thus $u^{-1}(t)$ represents the unit step at time $t=0$, $u^{-2}(t)$ the ramp, and $u^1(t)$ the doublet at time $t=0$.

Each of these properties can be deduced from the properties of $\delta(t;T)$ in the limit at reciprocal $T \rightarrow 0$. Finally, time. note that in accordance with Figure 9.43, the units of $\delta(t;T)$

Now that we have the definitions and limiting interpretations of $u(t;T)$ and $\delta(t;T)$ in hand, we can complete the analysis of the circuit shown in Figure 9.40 with a source that steps discontinuously. Suppose that the voltage source in the figure produces the ramping voltage step given by

$$V(t) = V_0 u(t;T). \quad (9.84)$$

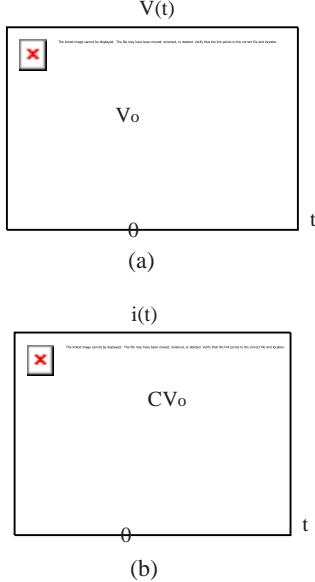


FIGURE 9.45 The voltage and current in the circuit shown in Figure 9.32 for a step voltage input.

Substitution of Equation 9.84 into Equation 9.64 then yields

$$i(t) = CV \cdot \delta(t;T). \quad (9.85)$$

Equation 9.85 shows that the voltage source supplies the current CV / T during the period $0 \leq t \leq T$ as it ramps up the capacitor voltage from $0V$ to V_0 ; note that $\delta(t;T) = 1/T$ during that period. In ramping up the capacitor voltage to V_0 , the source delivers the charge CV in accordance with Equation 9.8. This can be verified by integrating $i(t)$ over $0 \leq t \leq T$.

Now consider the circuit behavior described by Equations 9.84 and 9.85 in the limit $T \rightarrow 0$. In this case, V becomes the discontinuous voltage step described by Equations 9.79 and 9.80, and i becomes

$$i(t) = CV \cdot \delta(t) \quad (9.86)$$

which is the desired response to the discontinuous step in the source voltage. The forms of the input voltage step and the current impulse response for the circuit in Figure 9.32 are depicted in Figure 9.45.

This response can also be obtained directly by substituting Equation 9.80 into Equation 9.64, and then making use of Equation 9.82. At first glance, it might not appear that $CV \cdot \delta(t)$ has the units of current, but it does because CV has the units of charge, and $\delta(t)$ has the units of reciprocal time. In fact, $CV \cdot \delta(t)$ is the total charge delivered by the impulse current.

From our limiting interpretation of the impulse, we see that in Equation 9.86 i is a current that instantaneously delivers the charge CV to the capacitor at $t=0$. Thus, the charge stored in the capacitor takes a step at $t=0$, and so the voltage steps too as driven by the source. This illustrates an important point made earlier, namely that it takes an infinite current to cause the charge stored by, and hence the voltage appearing across, a capacitor to take a discontinuous step. Thus, except under unusual circumstances involving infinite currents, the state of a capacitor is a continuous function of time.

example 9.13 current step input to a inductor

Our next example considers a current step input of the following form (and sketched

in Figure 9.47a):

$$I(t) = \begin{cases} 0 & t \leq 0 \\ I^\circ & t > 0 \end{cases} \quad (9.87)$$

to the circuit shown in Figure 9.34 (redrawn here as Figure 9.46).

Since they are duals, the behavior of the circuit shown in Figure 9.46 parallels that of the circuit shown in Figure 9.40. Suppose that the current source in the figure produces the ramping current step given by

$$I(t) = I^\circ u(t; T). \quad (9.88)$$

Substitution of Equation 9.88 into Equation 9.66 then yields

$$v(t) = LI^\circ \delta(t; T). \quad (9.89)$$

Equation 9.89 shows that the current source supplies the voltage LI° / T during the period $0 \leq t \leq T$ as it ramps up the inductor current from 0 A to I° ; note again that $\delta(t; T) = 1/T$ during that period. In ramping up the inductor current to I° , the source delivers the flux linkage LI° in accordance with Equation 9.27. This can be verified by integrating $v(t)$ over $0 \leq t \leq T$.

Now consider the circuit behavior described by Equations 9.88 and 9.89 in the limit $T \rightarrow 0$. In this case, I becomes the discontinuous current step described by Equation 9.87 and

$$I(t) = I^\circ \lim_{T \rightarrow 0} u(t; T) \equiv I^\circ u(t) \quad (9.90)$$

and v becomes

$$\underline{v(t) = LI^\circ \delta(t)} \quad (9.91)$$

which is the desired response to the discontinuous step in the source current. The forms of the input current step and the voltage impulse response for the circuit in Figure 9.46 are depicted in Figure 9.47.

This response can also be obtained directly by substituting Equation 9.90 into Equation 9.66, and then making use of Equation 9.82. At first glance it might not appear that $LI^\circ \delta(t)$ has the units of voltage, but it does because LI° has the units of flux linkage, and $\delta(t)$ has the units of reciprocal time. In fact, LI° is the total flux linkage delivered by the impulse voltage.

From our limiting interpretation of the impulse we now see that v in Equation 9.91 is a voltage that instantaneously delivers the flux linkage LI° to the inductor at $t=0$. Thus, the flux linked by the inductor takes a step at $t=0$, and so the current steps too as driven by the source. This illustrates an important point made earlier, namely that it takes an infinite voltage to cause the flux linked by, and hence the current passing through, an inductor to take a discontinuous step. Thus, except under unusual circumstances involving infinite voltages, the state of an inductor is a continuous function of time.



FIGURE 9.46 A current source driving an inductor.

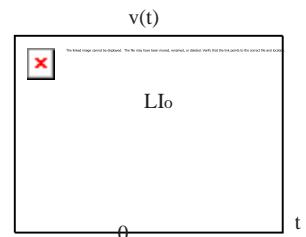
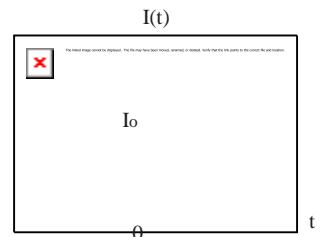


FIGURE 9.47 The current and voltage in the circuit shown in Figure 9.46 for a step current input.

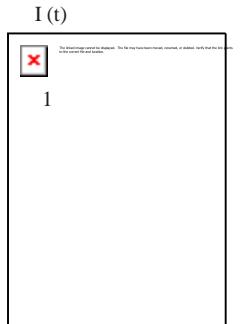
9.4.3 IMPULSE INPUTS

We introduced impulse functions in the previous section. Recall that a unit impulse denoted by $\delta(t)$ has the following properties.

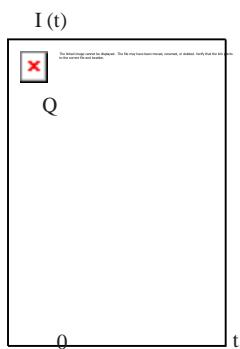
$$\delta(t)=0 \text{ for } t=0 \quad (9.92)$$

$$\int_{-\infty}^t \delta(t)dt = u(t) \Leftrightarrow \delta(t) = \frac{du(t)}{dt} \quad (9.93)$$

$$\int_{-\infty}^{\infty} \delta(t)dt = 1. \quad (9.94)$$



(a)



(b)

FIGURE 9.48 (a) The unit impulse $\delta(t)$; (b) a unit impulse with area Q .

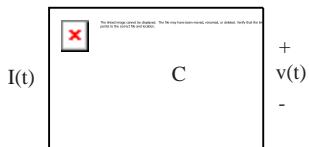


FIGURE 9.49 A current source driving a capacitor.

In other words, the impulse $\delta(t)$ is non-zero only for $t=0$. Its integral produces the unit step function, and the area under it is 1.

Recall further that the unit-area pulse function in Figure 9.44 becomes the unit impulse in the limit as $T \rightarrow 0$.

Figure 9.48a shows a unit current impulse and Figure 9.48b shows a current impulse with area under the impulse Q . In other words,

$$\int_{-\infty}^{\infty} i(t)dt = \int_{-\infty}^{\infty} \delta(t)dt = 1 \quad (9.95)$$

for the current in Figure 9.48a, and

$$\int_{-\infty}^{\infty} i(t)dt = \int_{-\infty}^{\infty} Q\delta(t)dt = Q \quad (9.96)$$

for the current in Figure 9.48b.

Let us analyze the circuit in Figure 9.31 (redrawn in Figure 9.49 for convenience) for an impulse input current with strength Q . In other words, an input current of the form:

$$I(t) = Q\delta(t).$$

Recall that solving the circuit implies finding the values of all the branch variables. The one branch variable that is unknown in the circuit is the voltage $v(t)$. We can obtain $v(t)$ by integrating the current through the capacitor as

$$\begin{aligned} v(t) &= C \int_{-\infty}^t I(t)dt \\ &= \frac{1}{C} \int_{-\infty}^t Q\delta(t)dt \\ &= \frac{1}{C} Qu(t). \end{aligned} \quad (9.97)$$

Thus, a current impulse of strength Q that occurs at time t deposits a charge Q on the capacitor. This charge results in the capacitor voltage jumping to $C_1 Q$ at time t , as illustrated in Figure 9.50.

Before ending this subsection, it is worthwhile to comment on impulse sources. Since impulses are a mathematical invention, and not a physical occurrence, it might appear that they have limited practical value. However, this is not the case. We often encounter sources that produce very narrow pulses of voltage or current. When these pulses are narrow, that we do not really care about the details of their shape, then we can model them very simply by an impulse with an equivalent area. From a mathematical viewpoint, this offers a significant saving since an impulse source is much easier to deal with than a source that produces a pulse with a complex shape. Thus, impulses are actually very useful modeling tools.

9.4.4 ROLE REVERSAL*

9.5 ENERGY, CHARGE, AND FLUX CONSERVATION

In Section 9.2, we studied the parallel combination of capacitors that stored no charge at the time of their connection, and the series combination of inductors that linked no flux at the time of their connection. In this section, we extend that study to consider connections in the presence of initial charge and flux linkage.

Consider the parallel connection of the two initially-charged capacitors shown in Figure 9.51; the connection occurs when the switch closes. We wish to determine the state of the capacitors after the switch is closed. KCL applied to the bottom node of the circuit dictates that

$$\frac{dq_1(t) + dq_2(t)}{dt} = \frac{d}{dt}(q_1(t) + q_2(t)) = 0. \quad (9.98)$$

Equation 9.98 states that the total charge $q_1 + q_2$ on both capacitors is constant, and hence conserved for all time, even as the switch closes. Now, let the switch close at $t = 0$. After the switch closes, that is, for $t > 0$, KVL applied to the loop in Figure 9.51 dictates that

$$v_1(t) = v_2(t), \quad (9.99)$$

and, with the help of Equation 9.8, that

$$\frac{q_1(t)}{C_1} = \frac{q_2(t)}{C_2} \quad (9.100)$$

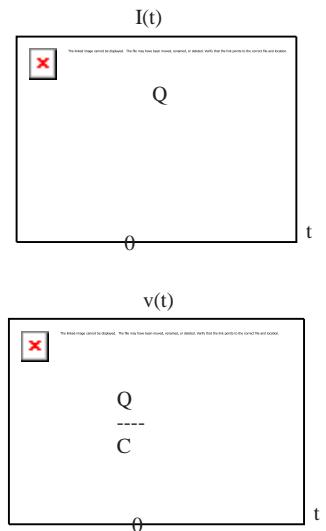


FIGURE 9.50 The current and voltage in the circuit shown in Figure 9.32 for an impulse current input.

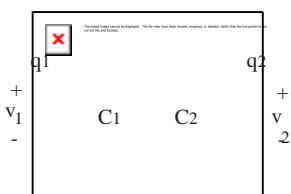


FIGURE 9.51 Two capacitors connected in parallel through a switch.

We can now use Equations 9.98 and 9.100 to determine the capacitor charges, and, with the help of Equation 9.8, the common voltage after the switch is closed. To begin, let us denote the charges on the two capacitors prior to switch closure as Q_1 and Q_2 . Then, from Equation 9.98,

$$q_1(t) + q_2(t) = Q_1 + Q_2. \quad (9.101)$$

Next, Equations 9.100 and 9.101 can be jointly solved to yield

$$q_1(t) = \frac{C_1}{C_1 + C_2(Q_1 + Q_2)} \quad (9.102)$$

$$q_2(t) = \frac{C_2}{C_1 + C_2(Q_1 + Q_2)} \quad (9.103)$$

for $t > 0$. Finally, Equations 9.102 and 9.103 can be substituted in Equation 9.8 to yield

$$v_1(t) = \frac{q_1(t)}{C_1} = \frac{Q_1 + Q_2}{C_1 + C_2^2} \quad (9.104)$$

$$v_2(t) = \frac{q_2(t)}{C_2} = \frac{Q_1 + Q_2}{C_1 + C_2^2}, \quad (9.105)$$

again for $t > 0$. According to Equations 9.102 and 9.103, the capacitors share the total charge in proportion to their capacitance.

While charge is conserved during the closure of the switch, it is interesting to note that energy is not. Using Equation 9.18, the total energy stored between the two capacitors before the switch is closed is found to be

$$w_E(t=0) = \frac{Q_1^2}{2C_1} + \frac{Q_2^2}{2C_2}. \quad (9.106)$$

Using Equations 9.102, 9.103, and 9.18, the total energy stored after the switch is closed is found to be

$$\begin{aligned} w_E(t>0) &= \frac{1}{C_1(Q_1+Q_2)^2} - \frac{1}{2C_1} + \frac{1}{C_2(Q_1+Q_2)^2} - \frac{1}{2C_2} \\ &= \frac{C_1 + C_2}{(Q_1 + Q_2)^2} \cdot \frac{C_1 + C_2}{2(C_1 + C_2)^2}. \end{aligned} \quad (9.107)$$

The two energies are not equal. Further, with a little algebraic manipulation, it can be seen that

$$WE(t<0) - WE(t>0) = \frac{1}{2} C_1 C_2 \frac{Q}{C_1} - \frac{Q_2^2}{C_2} \geq 0, \quad (9.108)$$

and so energy is always lost during the closure of the switch, except for the special case in which v_1 and v_2 are equal before the switch closes. Where the lost energy goes is not apparent from Figure 9.51 because it is an idealized figure. Perhaps the energy is dissipated in the wires used to connect the two capacitors and the switch. Or, perhaps it is dissipated in a spark as the switch closes. It might even be lost as radiated electromagnetic energy. In any case, it is lost. One of the problems at the end of this chapter explores this loss further.

Finally, we note that arguments similar to those presented here can be made for inductors connected in series. The corresponding circuit is shown in Figure 9.52. Initially, the switch is closed, allowing each inductor to carry an arbitrary current. Then, the switch opens. In this way, two inductors with different initial currents are connected in series. Using arguments similar to those presented earlier it is possible to determine the inductor currents and flux linkages after the switch opens. Then, it is straightforward to show that energy is lost during the opening of the switch.

example 9.14 charge sharing in capacitors

In

Figure 9.51, suppose that $C_1 = 1\ \mu\text{F}$ and $C_2 = 10\ \mu\text{F}$. Further, suppose that $v_1 = 10\text{ V}$ and $v_2 = 1\text{ V}$ before the switch is closed. How much energy is stored in the two capacitors before the switch is closed? Also, how much energy is lost during the switch closure, and what is the common voltage across the capacitors after the switch closes?

To begin, we find the charge on each capacitor before the switch closes. Using Equation 9.8, $Q_1 = 10\ \mu\text{C}$ and $Q_2 = 10\ \mu\text{C}$. Next, use Equations 9.102 and 9.103 to determine that $q_1 = 20/11\ \mu\text{C}$ and $q_2 = 200/11\ \mu\text{C}$ after the switch closes. Equation 9.103 or 9.104 can then be used to determine that $v = v_1 - 20/11\text{ V}$ after the switch closes. Finally, Equations 9.106 and 9.108 are used to determine that the initial stored energy is $55\ \mu\text{J}$, and that the energy lost is approximately $36.8\ \mu\text{J}$.

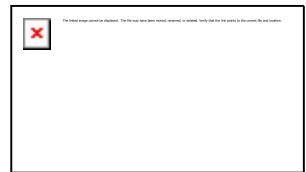


FIGURE 9.52 Two inductors connected in series through a switch.

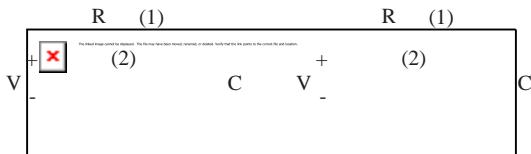
9.6 SUMMARY

In this chapter, we introduced capacitors and inductors, and derived their lumped element laws from more fundamental distributed physics. Since those element laws involved time derivatives, or alternatively time integrals, time became an important variable in this chapter. This was not the case in previous chapters because the circuits we studied there contained only sources, resistors, and idealized MOSFETs, all of which have purely algebraic element laws. Because time was an important variable in this chapter, we also began to consider a richer class of functions for the sources that would input signals into a circuit. These functions included sinusoids, steps, and impulses. The circuit responses to these inputs became our first examples of transients in electronic circuits.

When we first introduced capacitors and inductors, we did so through the effects that parasitic capacitance and inductance can have on the performance of an electronic circuit. This in turn caused us to evaluate our lumped matter discipline, under which such parasitics do not, by definition, exist. In the end we made a modeling compromise to preserve the lumped matter discipline while admitting the existence of important parasitics. That compromise was to augment an original circuit with lumped elements to model the important parasitics, with the understanding that the augmented model obeys the lumped matter discipline. While this is certainly an important issue, it is also important to realize that capacitors and inductors are useful well beyond the modeling of parasitics. As we shall see in future chapters they are frequently used on purpose.

Through our analysis of capacitors and inductors, and several simple circuits that contained them, we have seen that these elements exhibit memory and are capable of reversible energy storage. A simple experiment will illustrate. As illustrated in Figure 9.53, charge up a capacitor by connecting it to a power supply (position 1), then disconnect the supply (position 2). The capacitor will “remember” the voltage of the supply for hours if a high-quality capacitor is used. A similar experiment performed with a resistor produces no memory; when the power supply is disconnected, the resistor voltage instantly falls to zero.

FIGURE 9.53 The capacitor holds its voltage for a long period of time.



The corresponding experiment on an inductor yields less exciting results, however. Establish an inductor current by the circuit in Figure 9.54, with the switch in position 1. Then move the switch to position 2 (make before break). The current will decay to zero in fractions of a second, because the energy stored in the magnetic field is rapidly dissipated in the internal resistance of the coil.

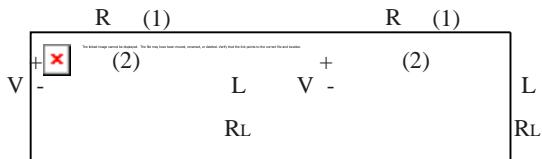


FIGURE 9.54 The inductor holds its current for a very short period of time.

Memory and reversible energy storage are characteristics associated with the state of the elements: charge in the case of the capacitor and flux linkage in the case of the inductor. This behavior is quite different from the behavior of ideal resistors. Ideal resistors do not exhibit memory, and they irreversibly dissipate energy.

The element law for a capacitor is

$$i = C \frac{dv}{dt}$$

and that for an inductor is

$$v = L \frac{di}{dt}.$$

The energy stored in a capacitor is

$$WE(t) = \frac{q_2(t)}{2C} = \frac{Cv(t)^2}{2}$$

The energy stored in an inductor is

$$WM(t) = \frac{\lambda_2(t)}{2L} = \frac{2}{Li(t)^2}$$

Finally, in the process of introducing capacitors and inductors, we defined the symbols and units for various physical quantities. These definitions are summarized in Table 9.1. The units can be further modified with the engineering multipliers listed in Table 1.3.

TABLE 9.1 Electrical engineering quantities, their units, and symbols for both.

Time	t	Second	s
Charge	q	Coulomb	C
Capacitance	C	Farad	F
Flux Linkage	λ	Weber	Wb
Inductance	L	Henry	H
Energy	w	Joule	J

EXERCISES

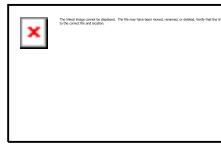
(a)

1 μF 3 μF



(b)

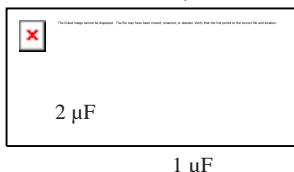
1 μF



3 μF

(c)

3 μF



2 μF

1 μF

FIGURE 9.55

exercise 9.1 Find the equivalent capacitance between the two terminals in each of the networks in Figure 9.55.

exercise 9.2 Find the equivalent capacitance or inductance for each case in Figure 9.56.

exercise 9.3 Consider a powerline on a computer backplane that is 2.5 mm wide, and separated from its underlying ground plane by 25 μm . Let the permittivity and permeability of the separating insulator be $2 \times 10^{-12} \text{ F/m}$ and $2 \times 10^{-6} \text{ Vs/A}$, respectively. What is the capacitance and inductance of the line per 10 cm of length?

If the voltage on the line is 5 V, how much energy is stored in its capacitance per 10 cm of length? If the current through the line is 1 A, how much energy is stored in its inductance per 10 cm of length?

exercise 9.4 A current source drives a capacitor as shown in Figure 9.57. The source current is as shown in Figure 9.58 for $0 \leq t \leq T$. If the capacitor voltage is V at $t = T$, what was it at $t = 0$?

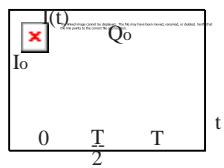
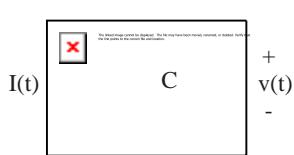
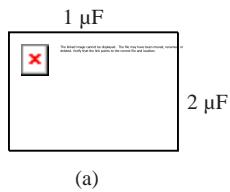


FIGURE 9.57 A currentsourcedrivingacapacitor.

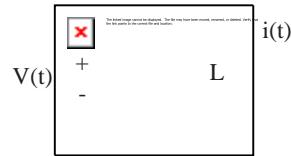
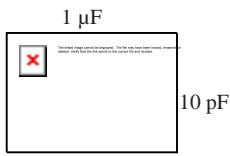
FIGURE 9.58 Sourcecurrent.

exercise 9.5 A voltage source drives an inductor as shown in Figure 9.59. The source voltage is as shown in Figure 9.60 for $0 \leq t \leq T$. If the inductor current is $I = at + b$ at $t = T$, what was it at $t = 0$?

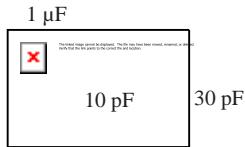
exercise 9.6 Figure 9.61 shows four circuits, labeled “1” through “4,” together with the waveform for the source in each circuit. The figure also shows four branch-variable waveforms, labeled “a” through “d,” that could correspond to the branch current or branch voltage labeled in the circuits. Match the branch variable waveforms to the appropriate circuit and source waveform.



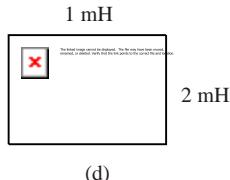
(a)

 $i(t)$ $V(t)$ L 

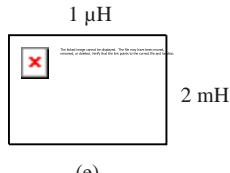
(b)



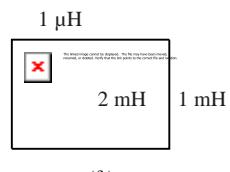
(c)



(d)



(e)



(f)

FIGURE 9.59 Acurrentsourcedrivinganinductor.

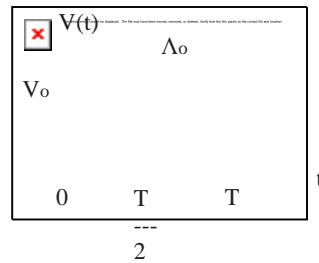
V_o

FIGURE 9.60 Sourcecurrent.

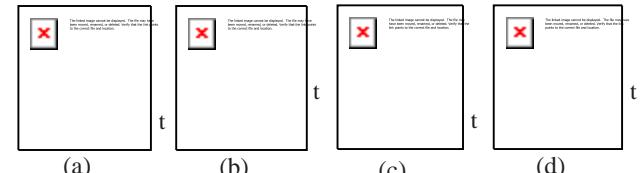
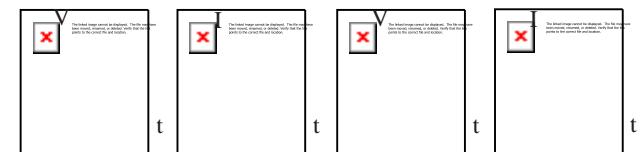
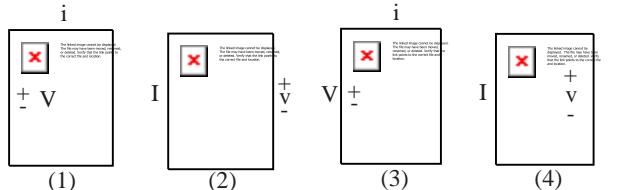


FIGURE 9.56

FIGURE 9.61

PROBLEMS

problem 9.1 A voltage source is connected in series with two capacitors as shown in Figure 9.62. The source voltage is $V(t) = 5V u(t)$, as shown. If the current i and voltage v are given by $i(t) = 4\mu C \delta(t)$ and $v(t) = 1V u(t)$, again as shown, what are C_1 and C_2 ?

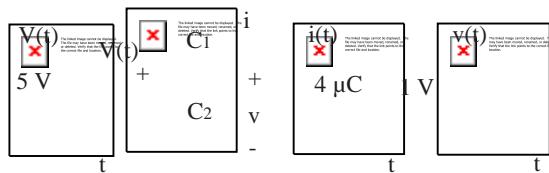


FIGURE 9.62

problem 9.2 A current source is connected in parallel with two inductors as shown in Figure 9.63. The source current is $i(t) = 400A/s u(t)$, as shown. If the current i and voltage v are given by $i(t) = 100A/s u(t)$ and $v(t) = 0.3V u(t)$, again as shown, what are L_1 and L_2 ?

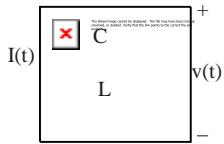


FIGURE 9.63

problem 9.3 A current source drives a series-connected capacitor and inductor as shown in Figure 9.64. Let $I(t) = I \sin(\omega t) u(t)$, and assume that the inductor and capacitor both stored no energy prior to $t=0$.

Determine the voltage v for $t \geq 0$.

Is there any relation between I , ω , C , and L for which v is constant for $t \geq 0$? If so, state the relation and determine v .

problem 9.4 A voltage source drives a parallel-connected capacitor and inductor as shown in Figure 9.65. Let $V(t) = V \sin(\omega t) u(t)$, and assume that the inductor and capacitor both stored no energy prior to $t=0$.

Determine the current i for $t \geq 0$.

Is there any relation between V , ω , C , and L for which i is constant for $t \geq 0$? If so, state the relation and determine i .

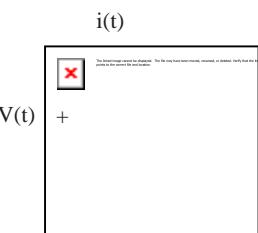


FIGURE 9.65

problem 9.5 A constant voltage source having value V drives a time-varying capacitor as shown in Figure 9.66. The time-varying capacitance is given by $C(t) = C_0 + C \sin(\omega t)$. Determine the capacitor current $i(t)$.

problem 9.6 A constant current source having value I drives a time-varying inductor as shown in Figure 9.67. The time-varying inductance is given by $L(t) = L_0 + L \sin(\omega t)$. Determine the inductor voltage $v(t)$.

problem 9.7 Consider the parallel plate capacitor shown in Figure 9.68. Assume that the dielectric is free space so that $\epsilon = \epsilon_0$.

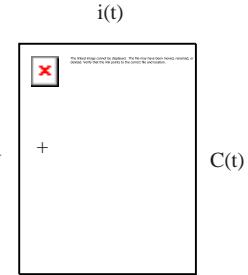


FIGURE 9.66

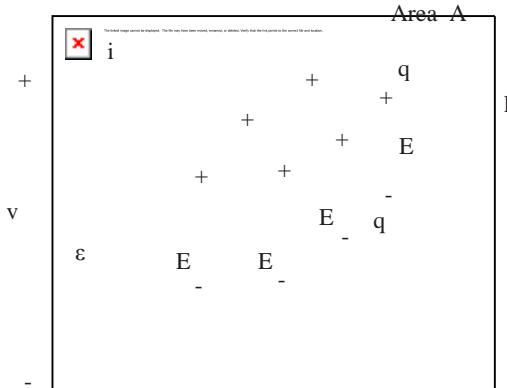


FIGURE 9.68

Suppose the capacitor is charged to the voltage V . Determine the charge and the electric energy stored in the capacitor in this case.

The capacitor is disconnected from the charging sources so that its stored charge remains constant. Following that, its plates are pulled apart so as to double the distance between them; that is, the gap separation is now $2l$. For this new configuration, determine the voltage across the terminals of the capacitor and the energy stored in the capacitor. Explain how the stored energy changes.

problem 9.8 Figure 9.69 shows two capacitive two-port networks. One is a “ π ” network, and one is a “T” network. For the π network, find $i_1 P$ and $i_2 P$ as functions of $v_1 P$ and $v_2 P$. For the T network, find $i_1 T$ and $i_2 T$ as functions of $v_1 T$ and $v_2 T$.

How must C_{1P}, C_{2P} , and C_{3P} be related to C_{1T}, C_{2T} , and C_{3T} for both networks to have the same terminal relations?

problem 9.9 Figure 9.70 shows two inductive two-port networks. One is a “ π ” network, and one is a “T” network. For the π network, find $v_1 P$ and $v_2 P$ as functions of $i_1 P$ and $i_2 P$. For the T network, find $v_1 T$ and $v_2 T$ as functions of $i_1 T$ and $i_2 T$.

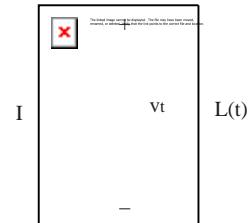
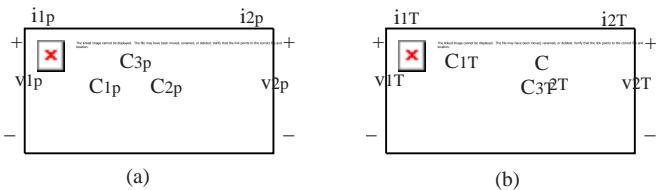


FIGURE 9.67

FIGURE 9.69 (a) A capacitive two-port network; and (b) a capacitive two-port network.



How must L_{1P} , L_{2P} , and L_{3P} be related to L_{1T} , L_{2T} , and L_{3T} for both networks to have the same terminal relations?

FIGURE 9.70 (a) An inductive two-port network; and (b) an inductive two-port network.

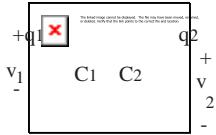
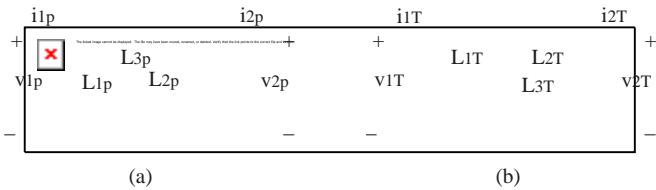


FIGURE 9.71

problem 9.10 This problem examines in more detail why energy is lost when the switch in Figure 9.71 closes. To do so, we examine the transient that occurs during the closure of the switch. In preparation for this, let $t = 0$ be the time at which the switch first begins to close, and let $t = T$ be the time at which the circuit reaches steady state. The charges on the two capacitors prior to switch closure are given to be Q_1 and Q_2 .

Further, let $q_1(t)$ be any function defined over the interval $0 \leq t \leq T$ such that

$$q_1(0) = Q_1$$

and $q_1(T)$ is the steady-state charge on the capacitor given by

$$q_1(T) = \frac{C_1}{C_1 + C_2(Q_1 + Q_2)}.$$

In this way, the function q_1 is an arbitrary transient connecting the initial and final chargeduring the switch closure.

(a) Use the charge conservation relation:

$$q_1(t) + q_2(t) = Q_1 + Q_2$$

to find q_2 in terms of q_1 for $0 \leq t \leq T$. Then, use the equation:

$$\frac{dq(t)}{dt} = i(t)$$

to determine i_1 and i_2 , again in terms of q_1 for $0 \leq t \leq T$. Finally, use the equation:

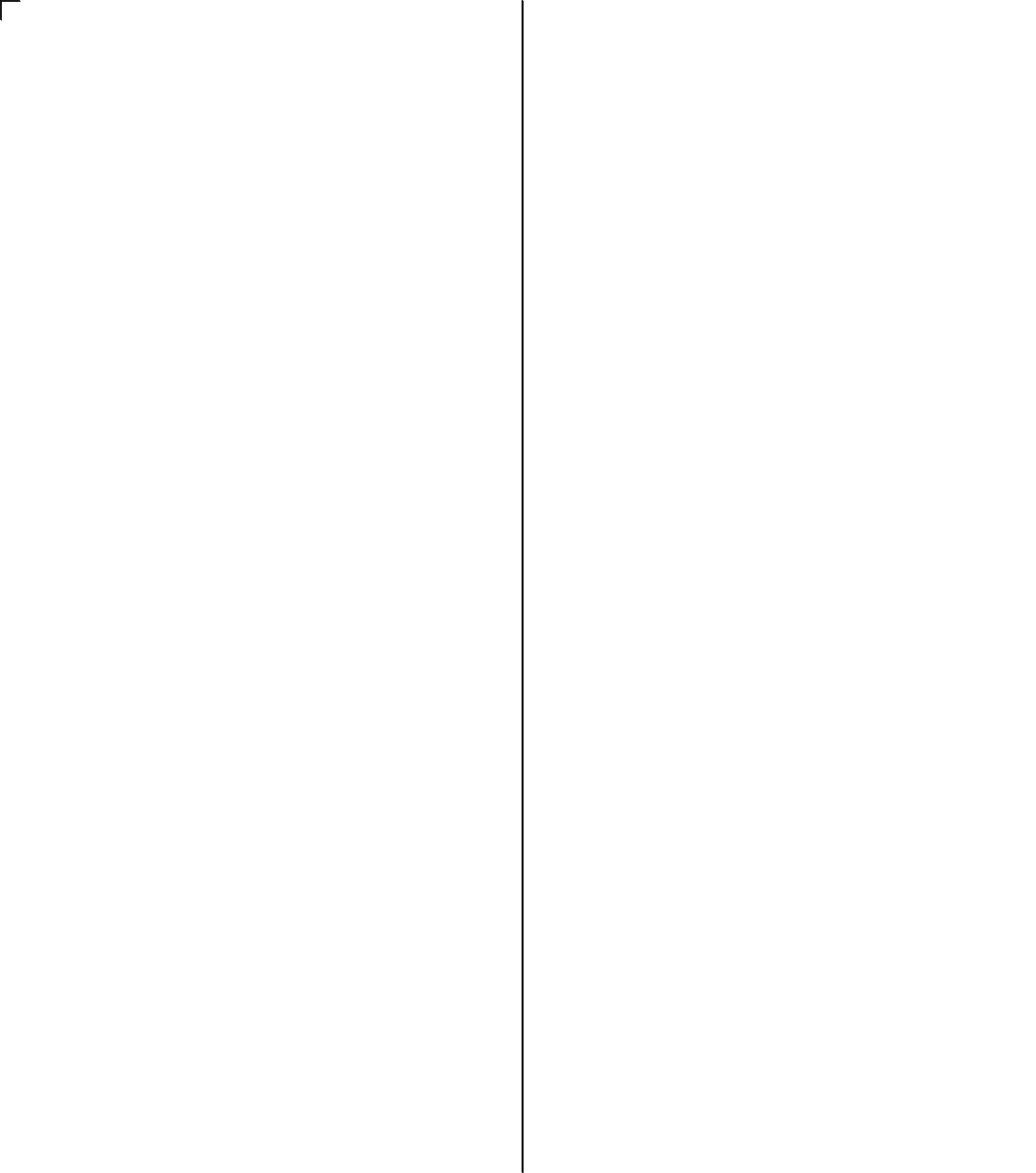
$$q(t) = Cv(t)$$

to find v_1 and v_2 , also in terms of q_1 for $0 \leq t \leq T$. The entire transient is now described in terms of the arbitrary function q_1 .

- (b) During the transient, the difference between v_1 and v_2 must appear across some element or elements within the circuit. KVL requires this. For example, it could appear across the wiring resistance or the switch, or a combination of both. In any case, energy is lost as current passes through this voltage difference. If we consider the voltage difference to be $(v_1 - v_2)$, as opposed to its opposite, then it is i_2 that passes into the positive terminal of this difference. Why?
- (c) The product $i_2(v_1 - v_2)$ is the power dissipated during the transient. Determine this power in terms of q_1 for $0 \leq t \leq T$.
- (d) Integrate the power found in the part (c) over the interval $0 \leq t \leq T$ to find the energy lost during the transient. Also, show that the energy lost is equal to the energy difference in

$$WE(t < 0) - WE(t > 0) = \frac{1}{2C_1 + C_2} \left(\frac{Q_1}{C_1} - \frac{Q_2}{C_2} \right)^2.$$

Remarkably, the energy lost is independent of the interior details of the function chosen for q_1 . Since these details are equivalent to the details of the loss mechanism, it is apparent that the amount of energy lost is independent of how it is lost.



chapter 10

10.1 ANALYSIS OF RC CIRCUITS

10.2 ANALYSIS OF RL CIRCUITS

10.3 INTUITIVE ANALYSIS

10.4 PROPAGATION DELAY AND THE DIGITAL ABSTRACTION

10.5 STATE AND STATE VARIABLES

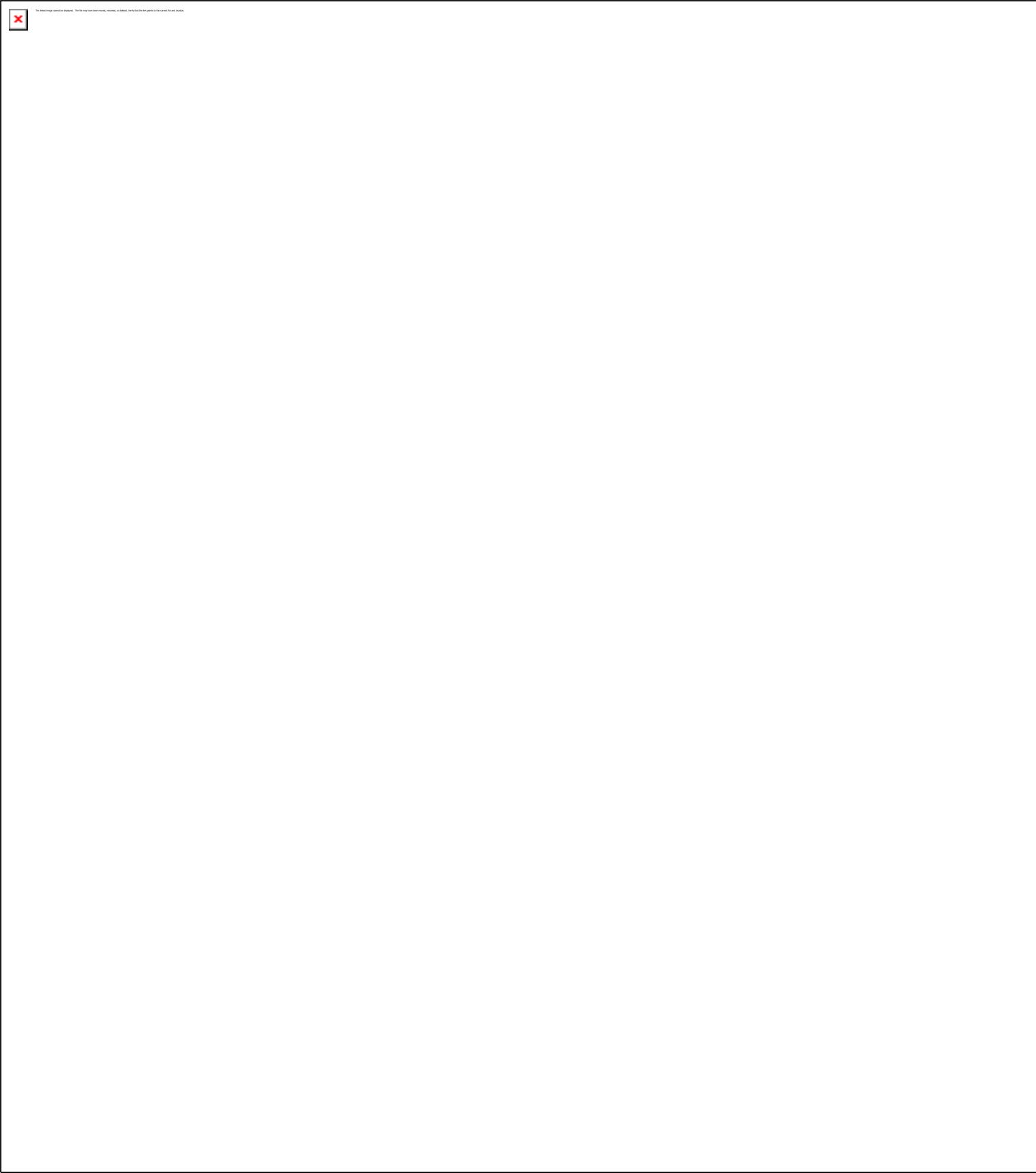
10.6 ADDITIONAL EXAMPLES

10.7 DIGITAL MEMORY

10.8 SUMMARY

EXERCISES

PROBLEMS



10

first-order transients in linear electrical networks

As illustrated in Chapter 9, capacitances and inductances impact circuit behavior. The effect of capacitances and inductances is so acute in high-speed digital circuits, for example, that our simple digital abstractions developed in Chapter 6 based on a static discipline become insufficient for signals that undergo transitions. Therefore, understanding the behavior of circuits containing capacitors and inductors is important. In particular, this chapter will augment our digital abstraction with the concept of delay to include the effects of capacitors and inductors.

Looked at positively, because they can store energy, capacitors and inductors display the memory property, and offer signal-processing possibilities not available in circuits containing only resistors. Apply a square-wave voltage to a multi-resistor linear circuit, and all of the voltages and currents in the network will have the same square-wave shape. But include one capacitor in the circuit and very different waveforms will appear — sections of exponentials, spikes, and sawtooth waves. Figure 10.1 shows an example of such waveforms for the two-inverter system of Figure 9.1 in Chapter 9. The linear analysis techniques already developed — node equations, superposition, etc. — are adequate for finding appropriate network equations to analyze these kinds of circuits. However, the formulations turn out to be differential equations rather than algebraic equations, so additional skills are needed to complete the analyses.

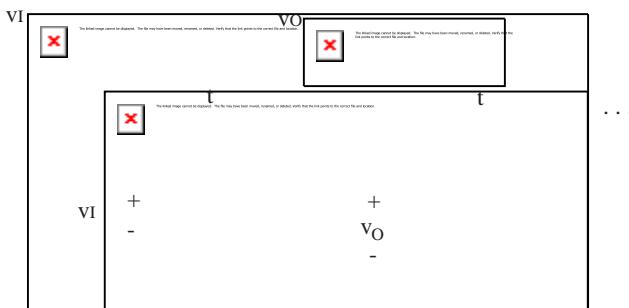


FIGURE 10.1 Observed response of the first inverter to a square-wave input.

This chapter will discuss systems containing a single storage element, namely, a single capacitor or a single inductor. Such systems are described by simple, first-order differential equations. Chapter 12 will discuss systems containing two storage elements. Systems with two storage elements are described by second-order differential equations.¹ Higher-order systems are also possible, and are discussed briefly in Chapter 12.

This chapter will start by analyzing simple circuits containing one capacitor, one resistor, and possibly a source. We will then analyze circuits containing one inductor and one resistor. The two-inverter circuit of Figure 10.1 is examined in detail in Section 10.4.

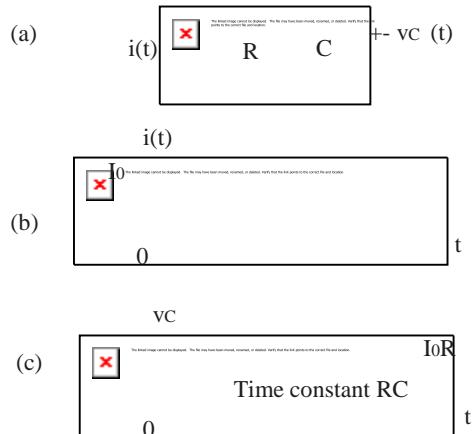
10.1 ANALYSIS OF RC CIRCUITS

Let us illustrate first-order systems with a few primitive examples containing a resistor, a capacitor, and a source. We first analyze a current source driving the so-called parallel RC circuit.

10.1.1 PARALLEL RC CIRCUIT, STEP INPUT

Shown in Figure 10.2a is a simple source-resistor-capacitor circuit. On the basis of the Thévenin and Norton equivalence discussion in Section 3.6.1, this circuit could result from a Norton transformation applied to a more complicated

FIGURE 10.2 Capacitor charging transient.



¹ However, a circuit with two storage elements that can be replaced by a single equivalent storage element remains a first-order circuit. For example, a pair of capacitors in parallel can be replaced with a single capacitor whose capacitance is the sum of the two capacitances.

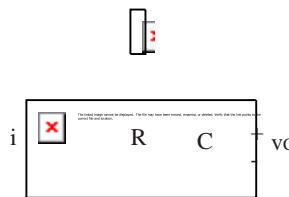
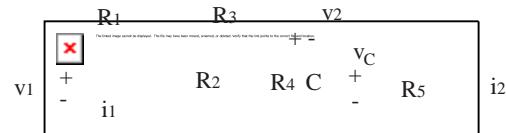


FIGURE 10.3 A more complicated circuit that can be transformed into the simpler circuit in Figure 10.2a by using Thévenin and Norton transformations.

$$v_C$$

$$v_C$$

$$i_t = \frac{d v_C}{dt}$$

$R_C + C$

$$\frac{d v_C}{dt} + \frac{v_C}{R_C} = \frac{i_t}{C}$$

$$v_{CT}$$

method of homogeneous and particular solutions

$$v_{CH}(t)$$

equation

$$\frac{dv}{dt} + \frac{vc}{RC} = 0 \quad (10.3)$$

associated with our nonhomogeneous differential equation 10.2. The homogeneous equation is derived from the original nonhomogeneous equation by setting the driving function, $i(t)$ in this case, to zero. Further, let $v_{CP}(t)$ be any solution to Equation 10.2. Then, the sum of the two solutions,

$$v_C(t) = v_{CH}(t) + v_{CP}(t)$$

is a general solution or total solution to Equation 10.2. $v_{CH}(t)$ is called the homogeneous solution and $v_{CP}(t)$ is called the particular solution. When dealing with circuit responses, the homogeneous solution is also called the natural response of the circuit because it depends only on the internal energy storage properties of the circuit and not on external inputs. The particular solution is also called the forced response or the forced solution because it depends on the external inputs to the circuit.

Let us now return to the business of solving Equation 10.2. To make the problem specific, assume that the current source $i(t)$ is a step function

$$i(t) = I_0 \quad t > 0 \quad (10.4)$$

as shown in Figure 10.2b. Further, we assume for now that the voltage on the capacitor was zero before the current step was applied. In mathematical terms, this is an initial condition

$$v_C = 0 \quad t < 0. \quad (10.5)$$

The method of homogeneous and particular solutions proceeds in three steps:

1. Find the homogeneous solution v_{CH} .
2. Find the particular solution v_{CP} .
3. The total solution is then the sum of the homogeneous solution and the particular solution. Use the initial conditions to solve for the remaining constants.

The first step is to solve the homogeneous equation, formed by setting the driving function in the original differential equation to zero. Then, any method of solving homogeneous equations can be used. In this case the homogeneous equation is

$$\frac{dv_{CH}}{dt} + \frac{v_{CH}}{RC} = 0. \quad (10.6)$$

We assume a solution of the form

$$v_{CH} = A e^{st} \quad (10.7)$$

because the homogeneous solution for any linear constant-coefficient ordinary differential equation is always of this form. Now we must find values for the constants A and s . Substitution into Equation 10.6 yields

$$A e^{st} + \frac{A e^{st}}{RC} = 0 \quad (10.8)$$

The value for A cannot be determined from this equation, but discarding the trivial solution of $A=0$, we find

$$\frac{1}{s + \frac{1}{RC}} = 0 \quad (10.9)$$

because e^{st} is never zero for finite s and t , so can be factored out. Hence

$$s = -\frac{1}{RC} \quad (10.10)$$

Equation 10.9 is called the characteristic equation of the system, and $s = -1/RC$ is a root of this characteristic equation. The characteristic equation summarizes the fundamental dynamic properties of a circuit, and we will have much more to say about it later chapters. For reasons that will become clear in Chapter 12, the root of the characteristic equation, s , is also called the natural frequency of the system.

We now know that the homogeneous solution is of the form

$$v_{CH} = A e^{-t/RC} \quad (10.11)$$

The product RC has the dimensions of time and is called the time constant of the circuit.

The second step is to find a particular solution, that is, to find any solution v_{CP} that satisfies the original differential equation; it need not satisfy the initial conditions. That is, we are looking for any solution to the equation

$$I_0 = \frac{V_{CP}}{R_{CP}} + C \frac{dv_{CP}}{dt} \quad (10.12)$$

Since the drive I_0 is constant in time for $t > 0$, one acceptable particular solution is also a constant:

$$v_{CP} = K \quad (10.13)$$

To verify this, we substitute into Equation 10.12

$$I_0 = \frac{K}{R} + 0 \quad (10.14)$$

$$K = I_0 R. \quad (10.15)$$

Because Equation 10.14 can be solved for K , we are assured that our “guess” about the form of the particular solution, that is, Equation 10.13, was correct.²

Hence the particular solution is

$$v_{CP} = I_0 R. \quad (10.16)$$

The total solution is the sum of the homogeneous solution (Equation 10.11) and the particular solution (Equation 10.16)

$$v_C = A e^{-t/RC} + I_0 R. \quad (10.17)$$

The only remaining unevaluated constant is A , and we can solve for this by applying the initial condition. Equation 10.5 applies for t less than zero, and our solution, Equation 10.17 is valid for t greater than zero. These two parts of the solution are patched together by a continuity condition derived from Equation 9.9: An instantaneous jump in capacitor voltage requires an infinite spike in current, so for finite current, the capacitor voltage must be continuous. This circuit cannot support infinite capacitor current (because $i(t)$ is finite, the infinite current would have to come from the resistor, and this is impossible). Thus we are justified in assuming continuity of v_C , hence we equate the solutions for negative time and positive time by solving at $t=0$

$$0 = A + I_0 R. \quad (10.18)$$

Thus

$$A = -I_0 R \quad (10.19)$$

and the complete solution for $t > 0$ is

$$v_C = -I_0 R e^{-t/RC} + I_0 R$$

² Alternatively, a guess of

$v_{CP} = K t$, where K is a constant independent of t , would not be correct, since substituting into Equation 10.12 yields

$$I_0 = \frac{K t}{R + CK}$$

which cannot be solved for a time-independent K .

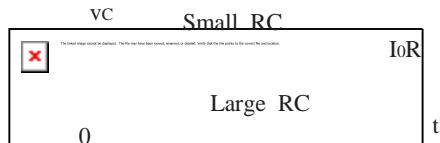


FIGURE 10.4 Significance of the RC time constant.

or

$$V_c = I_0 R (1 - e^{-t/RC}). \quad (10.20)$$

This is plotted in Figure 10.2c.

Some comments at this point help to give perspective. First, notice that capacitor voltage starts from a zero value at $t = 0$ and reaches its final value of $I_0 R$ for large t . The increase from 0 to $I_0 R$ has a time constant RC . The final value of $I_0 R$ for the capacitor voltage implies that all of the current from the current source flows through the resistor, and the capacitor behaves like an open circuit (for large t).

Also of second, the current from initial the value current of 0 source for the must capacitor be flowing voltage through it implies that the capacitor, at $t = 0$ and none through the resistor. Thus the capacitor behaves like an instantaneous short circuit. This illustrates the physical significance of the time constant RC can now be seen. Illustrated in Figure 10.4, it is the temporal scale factor that determines how rapidly the transient goes to completion.

Finally, it may seem that the solution to such a simple problem can't possibly be as involved as this appears. Correct. This problem and most first-order systems with step excitation can be solved by inspection (see Section 10.3). But here we are trying to establish general methods, and have chosen the simplest example to illustrate the method.

10.1.2 RC DISCHARGE TRANSIENT

With the capacitor now charged, assume that the current source is suddenly set to zero as suggested in Figure 10.5a, where for convenience, the time axis is redefined so that the turn-off occurs at $t = 0$. The relevant circuit to analyze the RC turn-off discharge transient now contains just a resistor and a capacitor as indicated in Figure 10.5c. The voltage on the capacitor at the start of the experiment is represented by the initial condition

$$V_c = I_0 R \quad t < 0. \quad (10.21)$$

This RC discharge scenario is identical to that of a circuit containing a resistor and a capacitor, where there is an initial voltage $V_c(0) = I_0 R$ on the capacitor.

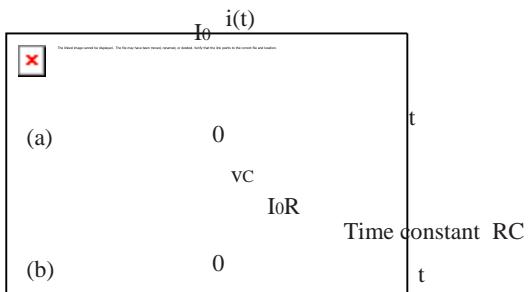


FIGURE 10.5 RC discharge transient.

Because the drive current is zero, the differential equation for $t > 0$ is now

$$0 = \frac{v_C}{R} + \frac{C dv_C}{dt} \quad (10.22)$$

As before, the homogeneous solution is

$$v_{CH} = A e^{-t/RC} \quad (10.23)$$

but now the particular solution is zero, since there is no forcing input, so Equation 10.23 is the total solution. In other words,

$$v_C = v_{CH} = A e^{-t/RC}$$

Equating Equations 10.21 and 10.23 at $t = 0$, we find

$$I_0 R = A \quad (10.24)$$

so the capacitor voltage waveform for $t > 0$ is

$$v_C = I_0 R e^{-t/RC}. \quad (10.25)$$

This solution is sketched in Figure 10.5b.

In general, for a resistor and capacitor circuit with an initial voltage $v_C(0)$ on the capacitor, the capacitor voltage waveform for $t > 0$ is

$$v_C = v_C(0)e^{-t/RC}. \quad (10.26)$$

Properties of Exponentials

Because decaying exponentials also occur frequently in solutions to simple RC and RL transient problems, it is helpful at this point to discuss some of the properties of these functions as an aid to sketching waveforms.

For a general exponential function of the form

$$x = Ae^{-t/\tau} \quad (10.27)$$

the initial slope of the exponential is

$$\frac{dx}{dt} \Big|_{t=0} = \frac{-A}{\tau}$$

Hence the initial slope of the curve, projected to the time axis, intercepts the time axis at $t = \tau$, irrespective of the value of A, as shown in Figure 10.6a.

Furthermore, becomes notice that when $t = \tau$, the function in Equation 10.27

$$x(t=\tau) = e^{-\frac{\tau}{\tau}} = \frac{A}{e}.$$

In other words, the function reaches $1/e$ of its initial value irrespective of the value of A. Figure 10.6b depicts this point in the exponential curve.

Because $e^{-5} = 0.0067$, it is common to assume for the t greater than five time constants, that is,

$$t > 5\tau$$

the function is essentially zero (see Figure 10.6a). That is, we assume the transient has gone to completion.

We will see later that these properties of the time constant make it useful in obtaining rough estimates for time durations associated with rising or falling exponentials.

10.1.3 SERIES RC CIRCUIT, STEP INPUT

Let us now convert the Norton source in Figure 10.2 to a Thévenin source in Figure 10.7 and determine the capacitor voltage as a function of time. The input waveform v_S is assumed to be a voltage step of magnitude V applied at $t = 0$,

FIGURE 10.6 Properties of exponentials.

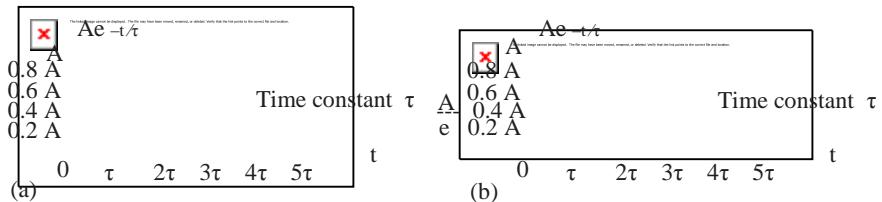
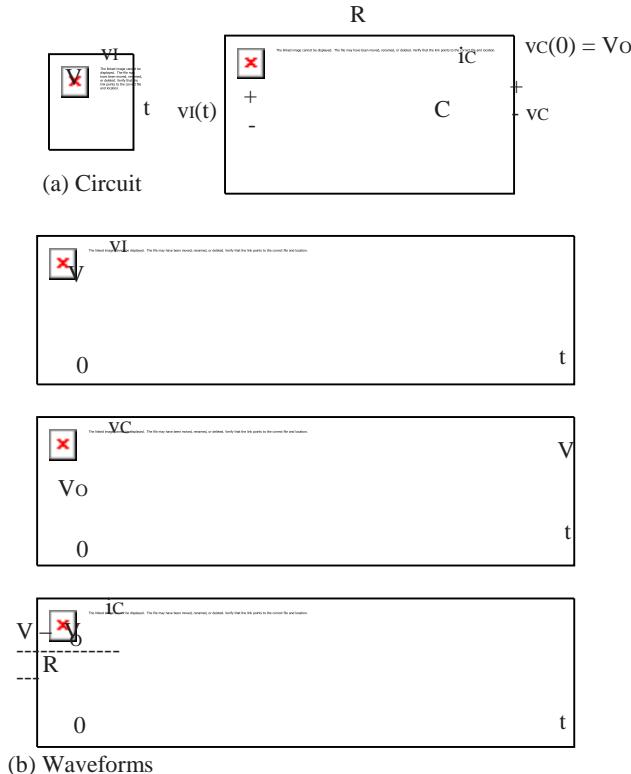


FIGURE 10.7 Series R C circuit with step input.



but this time around, we assume the capacitor voltage is V_o just before the step.³ That is, the initial condition on the circuit is

$$V_C = V_o \quad t = 0. \quad (10.28)$$

³For the purpose of determining the response for $t \geq 0$, it does not really matter how the capacitor voltage became V at $t = 0$, or the value of the capacitor voltage for $t = 0$. Nevertheless,

The differential equation can be found by using the node method. Applying KCL at the node with voltage v_C , we get

$$\frac{v_C - v}{R} + C \frac{dv_C}{dt} = 0.$$

Dividing by C and rearranging terms,

$$\frac{dv}{dt} + \frac{v_C}{RC} = \frac{V_L}{RC}. \quad (10.29)$$

The homogeneous equation is

$$\frac{dv_{CH}}{dt} + \frac{v_{CH}}{RC} = 0 \quad (10.30)$$

which, as expected, is the same as that in Equation 10.6 for the Norton circuit, since the Norton and Thévenin circuits are equivalent. Borrowing the homogeneous solution to Equation 10.6, we have

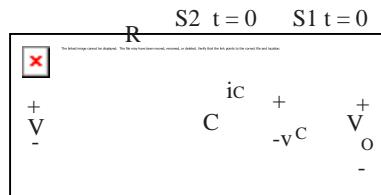
$$v_{CH} = Ae^{-t/RC} \quad (10.31)$$

where RC is the time constant of the circuit.

Let us now find the particular solution. Since the input drive is a step of magnitude V , the particular solution is any solution to

$$\frac{dv_{dtCP}}{dt} + \frac{v_{CP}}{RC} = \frac{RCV}{RC} . \quad (10.32)$$

the following is one possible circuit that will realize the given initial condition on the capacitor and the effect of a step input:



In the circuit, a DC source with value V_O is applied across the capacitor using switch $S1$. The DC source forces the capacitor voltage to V_O . This DC source is switched out as shown at $t=0$, and another DC source with voltage V is switched in using switch $S2$. This action applies a step voltage of magnitude V to the capacitor, which has an initial voltage V_O at $t=0$.

Because the drive is a step, which is constant for large t , we can assume a particular solution of the form

$$v_{CP} = K. \quad (10.33)$$

Substituting into Equation 10.32, we obtain

$$\frac{K}{RC} = \frac{V}{RC}$$

which implies $K = V$. So the particular solution is

$$v_{CP} = V. \quad (10.34)$$

Summing v_C and v_{CP} , we obtain the complete solution:

$$v_C = V + Ae^{-t/RC}. \quad (10.35)$$

The initial condition can now be applied to evaluate A . Given that the capacitor voltage must be continuous at $t=0$, we have

$$v_C(t=0) = V_0.$$

Thus, at $t=0$, Equation 10.35 yields

$$A = V_0 - V.$$

The complete solution for the capacitor voltage for $t > 0$ is now

$$v_C = V + (V_0 - V)e^{-t/RC} \quad (10.36)$$

where, V is the input drive voltage for $t > 0$ and V_0 is the initial voltage on the capacitor. As a quick sanity check, substituting $t=0$, we get $v_C(0) = V_0$,

and substituting $t=\infty$, we get $v_C(\infty) = V$. Both these boundary values are what we expect, since the initial condition on the capacitor is V_0 , and since the input voltage must appear across the capacitor after a long period of time.

By rearranging the terms, Equation 10.36 can be equivalently written as

$$v_C = V_0 e^{-t/RC} + V(1 - e^{-t/RC}). \quad (10.37)$$

Finally, from Equation 9.9, the current through the capacitor is

$$i_C = C \frac{dv_C}{dt} = \frac{V - V_0}{e^{-t/RC}} \quad (10.38)$$

This expression for i_C also matches our expectation since i_C must be 0 when t is large, and this is since the capacitor behaves like a voltage source with voltage V_0 during the step transition at $t=0$, the current at $t=0$ must equal $(V - V_0)/R$.

These waveforms are shown in Figure 10.7b.

If we desire the voltage v_R across the resistor, we can easily obtain it by applying KVL as

$$v_R = v_I - v_C$$

where we take the positive reference for v_R on the input side of the resistor.

Alternatively, we can obtain v_R by taking the product of the current and the resistance as

$$v_R = i_C R.$$

As one final point of interest, notice that Equation 10.36 was derived assuming both an initial non-zero state (V_0) and a non-zero input (a step of voltage V).

Substituting response (ZIRV): = 0 in Equation 10.36 we obtain the so called zero input

$$v_C = V_0 e^{-t/RC} \quad (10.39)$$

and response substituting (ZSR): $V_0 = 0$ in Equation 10.36 we obtain the zero state

$$v_C = V e^{-t/RC}. \quad (10.40)$$

In other words, the zero input response is the response for nonzero initial conditions, but where the input drive is zero. In contrast, the zero state response is the response of the circuit when the initial state is zero, that is, all capacitor voltages and inductor currents are initially zero.

~~Notice also that the total response is the sum of the ZIR and the ZSR,~~

~~as can be verified by adding the right-hand sides of Equations 10.39 and 10.40 and comparing to the right-hand side of Equation 10.36. We will have a lot more to say about the ZIR and the ZSR in Section 10.5.3.~~

10.1.4 SERIES RC CIRCUIT, SQUARE-WAVE INPUT

Examination of the waveforms in Figure 10.5a and 10.5b indicates that the presence of the capacitor has changed the shape of the input wave. When a square pulse is applied to the RC circuit, a decidedly non-square pulse, with slow rise and slow decay, results. The capacitor has allowed just a limited amount of wave shaping. This concept can be further developed by an experiment in which we drive the circuit with a square wave.

In this experiment, we will use a Thévenin source as in Figure 10.8. The source can be a standard laboratory square-wave generator. The input square wave is marked as in Figure 10.8. Several quite distinctive wave shapes for $v_C(t)$ can be derived, depending on the relation between the period of the driving square wave and the time constant RC of the network. These waveforms are all essentially variations on the solution derived in the preceding sections.

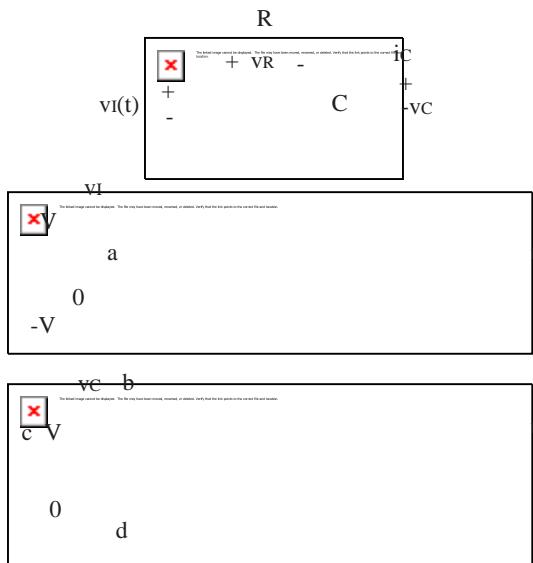


FIGURE 10.8 Response to squarewave.

For the case where the circuit time constant is very short compared to the square-wave period, the exponentials go to completion relatively rapidly, as suggested by waveform *b* in Figure 10.8. The capacitor waveform thus closely resembles the input waveform, except for a small amount of rounding at the corners.

If the time constant is a substantial fraction of the pulse length, then the solution appears as waveform *c* in Figure 10.8. Note that the drawing implies that the transients still go almost to completion, so there is an upper limit on the RC product for this solution to apply. Assuming, as noted here, that simple transients are complete for times greater than five time constants, the RC product must be less than one-fifth of the pulse length, or one-tenth the square-wave period for this solution to apply.

When the circuit time constant is much longer than the square-wave period, waveform *d*, shown in Figure 10.8, results. Here the transient clearly does not go to completion. In fact, only the first part of the exponential is ever seen. The waveform looks almost triangular, the integral of the input wave. This can be seen from the differential equation describing the circuit. Application of KVL gives

$$vi = iC R + vc. \quad (10.41)$$

Upon substitution of the constitutive relation for the capacitor, Equation 9.9, we obtain the differential equation

$$vi = RC \frac{dvc}{dt} + vc. \quad (10.42)$$

It is clear from Equation 10.42 or Figure 10.8 that as the circuit time constant becomes bigger, the capacitor voltage v_C must become smaller. For waveform d the time constant RC is large enough that v_C is much smaller than v_i , so in this case Equation 10.41 can be approximated by

$$v_i \approx iC. \quad (10.43)$$

Physically, the current is now determined solely by the drive voltage and the resistor, because the capacitor voltage is almost zero. Integrating both sides of Equation 10.42 assuming v_C is negligible, we obtain

$$v_C = \frac{1}{RC} v_i dt + K \quad (10.44)$$

where the constant of integration K is zero. Thus for large RC , the capacitor voltage is approximately the integral of the input voltage. This is a very useful signal-processing property. In Chapter 15 we will show that a much closer approximation to ideal integration can be obtained by adding an Op Amp to the circuit.

It is a simple matter to find the voltage across the resistor in the circuit of Figure 10.8 because we can find the current from the capacitor voltage using Equation 9.9,

$$v_R = iC = RC dv/dt.$$

Thus, during the charge interval, for example, from Equation 10.20, assuming the transients go to completion,

$$v_C = V(1 - e^{-t/RC}).$$

Hence

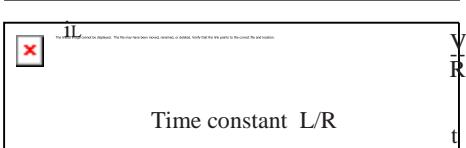
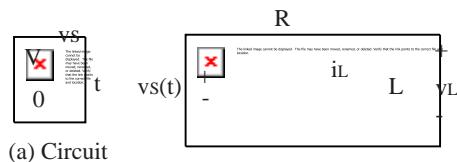
$$v_R = V e^{-t/RC}.$$

The wave shapes in Figure 10.8 change very little if the input signal v_i has zero average value, that is, if v_i is changed so that it jumps back and forth from $-V/2$ to $+V/2$. Specifically, v_C also has zero average value, and if the transients go to completion, as in waveforms b and c , the excursions will be $-V/2$ and $+V/2$.

10.2 ANALYSIS OF RL CIRCUITS

10.2.1 SERIES RL CIRCUIT, STEP INPUT

Figure 10.9 will serve as a simple illustration of a transient involving an inductor. (See the example discussed in Section 10.6.1 for a practical application of the analysis involving inductor transients.) The input waveform v_S is assumed to



(b) Waveforms

FIGURE 10.9 Inductorcurrent buildup.

beavoltagestepappliedat $t=0$ (seeFigure10.9a),andtheinductorcurrent isassumedtobezerojustbeforethestep.Thatis,theaditionalconditiononthe circuitis

$$i_L=0 \quad t<0. \quad (10.45)$$

Suppose that we are interested in solving for the current i_L . As before, we canusethenodenode methodtoobtainanequationinvolvingtheunknownnode voltage v_L , andthenusetheconstituentequationforaninductordfromEquation9.28tosubstitutefor v_L intermsofthevariableofinteresttous,namely i_L .Forvariety,however,wewillderivethesamedifferentialequationini i_L by applyingKVL:

$$-vs+i_LR+L\frac{di_L}{dt}=0. \quad (10.46)$$

Thehomogeneousequationis

$$L\frac{di_L}{dt}+i_LR=0. \quad (10.47)$$

Assumeasolutionoftheform

$$i_{LH}=A_{est}. \quad (10.48)$$

Hence

$$LsAe_{st} + RAe_{st} = 0. \quad (10.49)$$

For non-zero A ($A=0$ is a trivial solution)

$$Ls + R = 0.$$

or

$$\frac{R}{s + L} = 0 \quad (10.50)$$

$$s = -\frac{R}{L}. \quad (10.51)$$

Equation 10.50 is the characteristic equation for our circuit, and Equation 10.51 gives the natural frequency.

The homogeneous solution is thus

$$i_{LH} = Ae^{-(R/L)t} \quad (10.52)$$

where the time constant is in this case L/R .

The particular solution can be obtained by solving

$$i_{LP}R + L \frac{di_{LP}}{dt} = vs. \quad (10.53)$$

Because the drive is a step, which is constant for large t , it is again appropriate to assume a particular solution of the form

$$i_{LP} = K. \quad (10.54)$$

Substituting into Equation 10.53, and noting that for large t , $vs = V$, we obtain

$$KR = V.$$

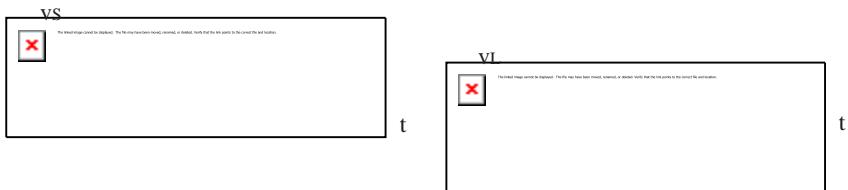
or,

$$K = \frac{V}{R}. \quad (10.55)$$

So, from Equation 10.54, the particular solution is

$$i_{LP} = \frac{V}{R} \quad (10.56)$$

FIGURE 10.10 Response to a square-wave input.



and the complete solution is of the form

$$i_L = \frac{V}{R} + A e^{-(R/L)t} \quad . \quad (10.57)$$

The initial condition together with a continuity condition, can now be applied to evaluate A. The continuity condition for inductor current can be found from Equation 9.28. If it can be shown that the inductor voltage cannot be infinite in the circuit, then di/dt must be finite, hence the inductor current must be continuous. For this particular circuit, with finite v_s , we are assured of finite v_L , hence i_L in Equation 10.57 can be evaluated at $t=0$, and set equal to the initial value, Equation 10.45:

$$\frac{V}{R} + A = 0. \quad (10.58)$$

The complete solution for the inductor current for $t > 0$ is now

$$i_L = \frac{V}{R} - I - e^{-(R/L)t} \quad (10.59)$$

and, from Equation 9.28, the voltage across the inductor is

$$\underline{\underline{v_L = L di/dt = -Ve^{-(R/L)t}}} \quad (10.60)$$

These waveforms are shown in Figure 10.9b. Notice that the inductor current has an initial value of 0 and a final value of V/R . Thus the inductor behaves like a instantaneous open circuit at $t=0$ and a short circuit for large t , for the step voltage input at $t=0$. v_L is correspondingly V at $t=0$ and 0 for large t . The response to a square-wave input is shown in Figure 10.10.

10.3 INTUITIVE ANALYSIS

The previous sections illustrated the general method of analyzing linear RC and RLC circuits. These several examples with step-function drive that we worked previously suggest that such circuits have a very limited range of solutions.

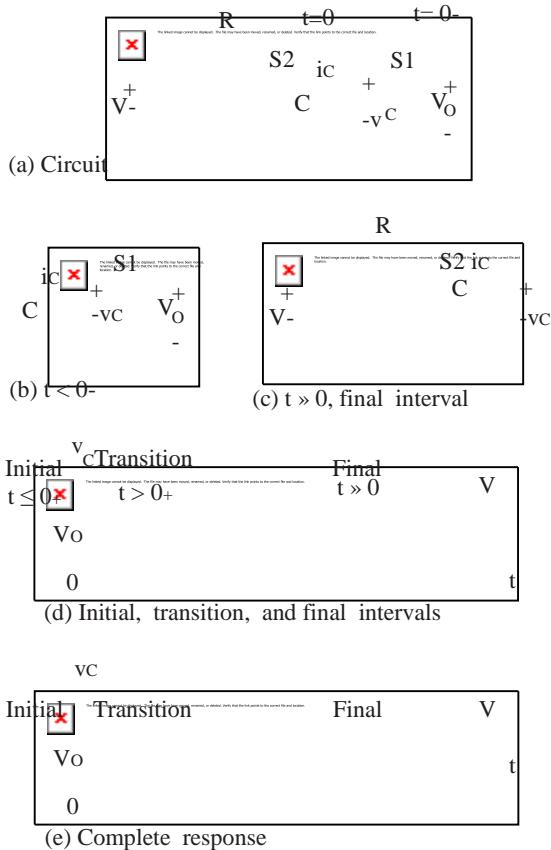


FIGURE 10.11 Steady-state response of a series RC circuit. The arrangement of switches provides for the initial voltage V_o on the capacitor, and an input step voltage of magnitude V at $t = 0$.

The two basic forms that we saw are $e^{-\alpha t}$ and $(1 - e^{-\alpha t})$. Accordingly, it turns out that for simple excitations, such as the step and the impulse, the response of first-order systems can be sketched easily using some intuition.

Let us illustrate using the step response of a series RC circuit in Figure 10.11 as an example. We will address the most general case, namely one in which there is both an nonzero initial state and a nonzero input. These seemingly elaborate arrangements of switches simply provides for the initial voltage V_o on the capacitor, and an input step voltage of magnitude V at $t = 0$, a situation similar to that in Section 10.1.3. For the purposes of sketching our result, we will further assume that $V > V_o$. As illustrated in Figure 10.11a, switch S_1 is initially closed and S_2 is open, resulting in the voltage V_o being applied directly across the capacitor. Just before $t = 0$, that is, at $t = 0^-$, S_1 is opened (S_2 remains open). Then, at $t = 0$, S_2 is closed (S_1 remains open). The closing of S_2 and opening of S_1 results in a series RC circuit with a step voltage V applied at $t = 0$.

Suppose we are interested in sketching the voltage v_C as a function of time.⁴ The form of the response can be sketched intuitively by identifying three intervals of operation as indicated in Figure 10.11d: the initial interval, which extends until $t = 0+$ (that is, the time instant just after $t = 0$), the transition interval, which is identified as the interval after $t = 0+$, and the final interval, where S_2 has been closed and S_1 has been open for a long time.

The overall response can be quickly sketched through inspection by first determining the initial and final interval values of the voltage on the capacitor.

Initial Interval ($t \leq 0+$) During this initial interval, when S_1 is closed ($t < 0-$), the effective circuit is as shown in Figure 10.11b, with a DC source with voltage V_0 appearing across the capacitor. Thus, the capacitor voltage is V_0 during $t < 0-$.

Next, notice that in the short period of time between $t = 0-$ and $t = 0$, and still within the initial interval, the capacitor is not connected to any other circuit (recall S_1 is opened at $t = 0-$ and S_2 is closed immediately thereafter at $t = 0$). Assuming the capacitor is ideal, it holds its charge and its voltage remains at V_0 until the switch S_1 is closed.

Then, at $t = 0$, S_1 is closed, resulting in a finite step of magnitude V being applied to a series RCC circuit in which the capacitor has a voltage V_0 across it. Let us now determine the capacitor voltage at $t = 0+$, just after the step. From the element law of the capacitor (Equation 9.7), we know that an instantaneous jump in capacitor voltage requires an infinite spike (that is, an impulse) in current. Since a finite step voltage applied across a resistor cannot support an infinite spike in current, we conclude that the capacitor voltage cannot change instantaneously, rather it must be continuous. Thus, the voltage across the capacitor at $t = 0+$ must also be V_0 . This is our initial condition on the capacitor. The voltage across the capacitor during the initial interval ($t \leq 0+$) is sketched in Figure 10.11d.

Final Interval ($t > 0$) We next turn our attention to the final interval. To determine the capacitor voltage in the final interval, observe that our situation is identical to that of a DC source with voltage V applied across the series combination of R and C shown in Figure 10.11c. Since the capacitor current is proportional to the rate of change of the capacitor voltage (Equation 9.7), in a DC situation, where all transients have died out, the current flowing through the capacitor must be zero. In other words, in a DC situation, the capacitor voltage has attained some fixed value, and hence the capacitor current is zero. Effectively, the capacitor behaves like an open circuit for DC sources. Since no current is flowing, the drop across the resistor must be zero. Thus, to

⁴ Other branch variables in the circuits such as i_C and v_R share the same general form and can be derived in an analogous fashion.

satisfy KVL, the capacitor voltage must equal V , the voltage of the DC source. This value is sketched in the final interval in Figure 10.11d.

Transition Interval ($t > 0^+$) We have now sketched the initial and final values of the capacitor voltage. The transition interval for $t > 0^+$ remains to be analyzed. During this interval, observe that the capacitor voltage cannot jump instantaneously from V_o to V due to the continuity condition. Specifically, we know from the solution to the homogeneous equation for the RC circuit that the transient follows an exponential form, either rising ($1 - e^{-t/RC}$) or falling ($e^{-t/RC}$), with time constant RC . (For the corresponding inductor-resistor circuit the time constant will be L/R .) In our case, since $V > V_o$, the transient will be arising exponential.

Complete Response The complete response for all of the three regions is sketched in Figure 10.11e.

The corresponding equation for the capacitor voltage that matches the initial and final values, and the exponential with time constant RC , for $t \geq 0$, is

$$v_C = V + (V_o - V)e^{-t/RC}.$$

In other words, for $t \geq 0$,

$$v_C = \text{final value} + (\text{initial value} - \text{final value})e^{-t/\text{time constant}} \quad (10.61)$$

or equivalently, rearranged a little bit,

$$\frac{v_C - \text{initial value}}{e^{-t/\text{time constant}}} + \text{final value}(1 - e^{-t/\text{time constant}}) \quad (10.62)$$

You might want to confirm that Equation 10.61 combined with the appropriate boundary conditions results in the same solutions as obtained by solving the differential equations in the previous sections. For example, for the RC discharge transient example of Section 10.1.2, the initial capacitor voltage is given as $v_C(0)$ and the final value is zero. Substituting $V_o = v_C(0)$ and $V = 0$ into Equation 10.61, we obtain

$$v_C = v_C(0)e^{-t/RC}$$

which is the same as the expression obtained in Equation 10.26.

At this point, we take a moment to make a couple of other helpful observations. Sometimes, we desire the response related to the capacitor current. The responses related to the capacitor current can be easily determined from the voltage response and the capacitor element law. However, the current response can also be directly obtained by using the same type of insight that we used to obtain the voltage response. Here, we would seek the initial and final values of the current. In our example, the final value of the capacitor current

after all transients have died out ($t=0$). The initial value of the current ($t=0$) can also be determined easily. Since the capacitor voltage at $t=0$ is V_0 , the instantaneous current through the capacitor at $t=0$ is given by

$$i_C(t=0) = \frac{V - V_0}{R}$$

which is the voltage across the resistor ($V - V_0$) divided by the resistance (R).

Thus, at the instant that the switch S_1 is closed, the capacitor behaves like an instantaneous voltage source with voltage V_0 . In like manner, if the initial voltage on the capacitor were zero (that is, $V_0=0$), then the capacitor would behave like an instantaneous short circuit. In either case, notice that the capacitor current is not necessarily continuous, only the state variable. In our example, the capacitor current jumps from 0 to $(V - V_0)/R$ at $t=0$. The current decays exponentially with time constant RC from the initial value of $(V - V_0)/R$ at $t=0$ to its final value of zero. The current response is plotted in Figure 10.12.

Inductors can be treated in a similar manner. The key difference is that the state variable for an inductor is its current. Accordingly, the inductor current is continuous (recall, from Equation 9.26, an instantaneous jump in inductor current requires an infinite spike, that is, an impulse, in the voltage). To determine initial and final values of the inductor current, remember that the inductor behaves like a long-term short circuit for DC current sources, and like an instantaneous open circuit for abrupt transitions.⁵ The time constant for circuits containing an inductor and a resistor is L/R . With these definitions, Equation 10.61 is equally applicable to inductor-resistor circuits.

As an inductor-resistor example, consider the current response of the series RLC circuit from Figure 10.9a redrawn in Figure 10.13. As sketched in Figure 10.13, the initial current through the inductor is zero. The final current through the inductor is V/R , because the inductor behaves like a long-term short circuit. The time constant of the circuit is L/R . Substituting into Equation 10.61, we get

$$i_L = \frac{V}{R} + \frac{V}{R} e^{-\frac{t}{L/R}}$$

or

$$i_L = \frac{V}{R} \left(1 - e^{-\frac{t}{L/R}} \right)$$

which is identical to Equation 10.59.

⁵ If the inductor current were nonzero, then it would behave like an instantaneous current source for abrupt transitions.

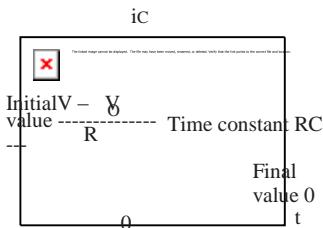


FIGURE 10.12 Current response of a series RC circuit to a step input.

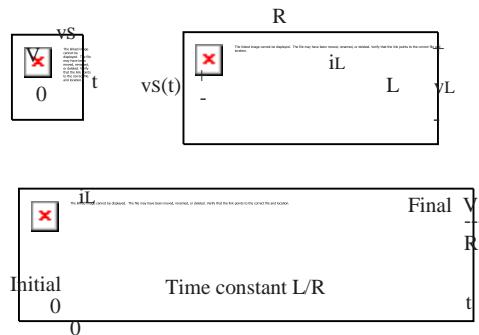


FIGURE 10.13 SeriesRL circuit, step response through intuitive analysis.

This section showed how we can quickly sketch the step response using intuition. A similar approach also works for impulse responses. Intuitive analysis for impulses is discussed further in Section 10.6.4.

10.4 PROPAGATION DELAY AND THE DIGITAL ABSTRACTION

The RC effects we have seen thus far are the source of delays in digital circuits, and are responsible for the waveforms shown in Figure 9.3 in Chapter 9, or those in Figure 10.1 in this chapter. Consider the two-inverter digital circuit shown in Figure 10.14 in which inverter A drives inverter B. Inverter A is driven by an input V_{IN1} and its output is V_{OUT1} . Figure 10.15 replaces the inverters with their internal circuits comprising MOSFETs and resistors.

Let us begin by reviewing the basic inverter circuit. Assume that the threshold voltage for both MOSFETs is 1 volt. When V_{IN1} is low (< 1 volt), MOSFET A is turned off, and no current flows from its drain to its source. Output voltage V_{OUT1} is high. In contrast, when V_{IN1} is high, MOSFET A is turned on. Its output voltage V_{OUT1} is given by the voltage-divider relationship

$$V_{OUT1} = \frac{R_{ON}}{R_{ON} + R_L} V_{IN1}$$

Ideally, the input V_{IN1} (corresponding to a sequence of 1's and 0's of the form shown in Figure 10.16) should produce the ideal output V_{OUT1} (ideal).

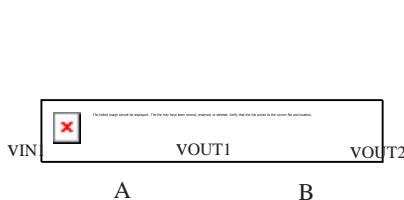


FIGURE 10.14 Inverters connected in series.

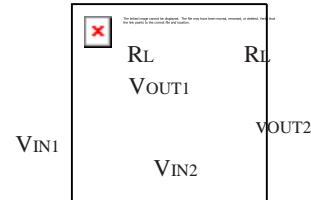


FIGURE 10.15 Internal circuit of the inverters.

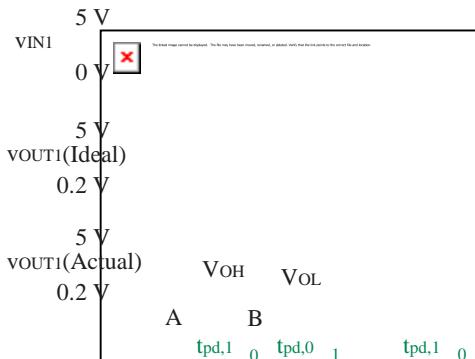


FIGURE 10.16 Characteristics of ideal and actual inverters.

As shown in Figure 10.16, the output of an ideal inverter should show a change at the same instant as the input. Furthermore, the output should be an ideal square wave just like the input.

However, in practice, if we were to observe the output V_{OUT1} on an oscilloscope, we would notice that the change in the output is not instantaneous; rather the output changes from one valid voltage level (for example, a logical 0) to another valid voltage level (for example, a logical 1) more slowly over a small period of time as suggested by the signal marked $V_{OUT1}(\text{actual})$ in Figure 10.16. How does this slow transition affect the behavior of the digital circuit?

Recall that the V_{OUT1} signal represents a digital signal, so it must reach V_{OH} so that the gate that produced it adheres to the static discipline and we obtain a nonzero noise margin. As suggested in the lowermost signal in Figure 10.16, notice that the V_{OH} crossing happens at time interval $tpd.1 \rightarrow 0$ after the input changes from a 1 to a 0. Thus, effectively, there is a delay of $tpd.1 \rightarrow 0$ between the moment that the input changes to a 0 to the moment that the output changes to a valid 1.

This period of time is called the propagation delay⁶ through inverter A for a 0 to 0 transition at the input and is denoted as $tpd.1 \rightarrow 0$.

As suggested in the lowermost signal in Figure 10.16,

the inverter is also characterized by a 0 \rightarrow 1 propagation delay. This delay is denoted as $tpd.0 \rightarrow 1$.

The $tpd.1 \rightarrow 0$ and $tpd.0 \rightarrow 1$ delays are not necessarily equal. For simplicity, we often characterize digital gates by a single delay called its propagation delay tpd and choose

$$tpd = \max(tpd.1 \rightarrow 0, tpd.0 \rightarrow 1) \quad (10.63)$$

6. The propagation delay is sometimes defined as the time interval from the 50% point of the input signal transition to the 50% point of the output signal transition.

10.4.1 DEFINITIONS OF PROPAGATION DELAYS

The following are more general definitions of propagation delays associated with digital gates with multiple inputs and outputs. The reader wishing to return to the computation of t_{pd} for our inverter example can skip this section without loss of continuity and proceed directly to Section 10.4.2.

$t_{pd,1 \rightarrow 0}$ We define $t_{pd,1 \rightarrow 0}$ for a given input terminal and a given output terminal of a combinational digital circuit as the signal propagation delay from the input terminal to the output terminal for a high-to-low instantaneous transition at the input. More precisely, $t_{pd,1 \rightarrow 0}$ for an input-output terminal pair is the time interval from the moment that the input changes from a 1 to a 0 to the moment that the output reaches a corresponding valid output voltage level (V_{OH} or V_{OL}).

$t_{pd,0 \rightarrow 1}$ Similarly, we define $t_{pd,0 \rightarrow 1}$ for a given input terminal and a given output terminal of a combinational digital circuit as the signal propagation delay through input-output terminal pair for a low-to-high instantaneous transition at the input. More precisely, $t_{pd,0 \rightarrow 1}$ for an input-output terminal pair is the time interval from the moment that the input changes from a 0 to a 1 to the moment that the output reaches a corresponding valid output voltage level.

t_{pd} for an Input-Output Terminal Pair: We define the propagation delay t_{pd} between an input terminal and an output terminal of a combinational circuit as

$$t_{pd} = \max(t_{pd,1 \rightarrow 0}, t_{pd,0 \rightarrow 1})$$

where $t_{pd,1 \rightarrow 0}$ and $t_{pd,0 \rightarrow 1}$ are the corresponding 1 \rightarrow 0 and 0 \rightarrow 1 delays for the same input-output terminal pair.

Propagation Delay t_{pd} for a Combinational Gate: If $t_{pd,i,j}$ is the propagation delay between input terminal i and output terminal j of a digital gate, then the propagation delay of the gate is given by

$$t_{pd} = \max_{i,j} t_{pd,i,j}$$

which is the maximum delay of all input-to-output paths. The propagation delay is also called the gated delay.

In the simple example shown in Figure 10.16, the propagation delay through the inverter for a low-to-high transition at the input, $t_{pd,0 \rightarrow 1}$, is also equal to the rise time of the output of the inverter. Similarly, $t_{pd,1 \rightarrow 0}$, is also equal to the fall time of the inverter output. The rise and fall times are properties of output terminals of circuits, while propagation delays measure the relative

signal transition times between inputs and outputs of circuits. The rise and fall times are defined as follows:⁷

Rise Time In general, the rise time for an output is defined as the delay in rising from its lowest value to a valid high (V_{OH}) at that output.

Fall Time The fall time for an output is defined as the delay in falling from its highest value to a valid low (V_{OL}) at the same output.

In general, the propagation delay and the rise/fall time are not equal. The $0 \rightarrow 1$ propagation delay for a digital circuit is the time between an input 0 to 1 transition (the input transition is assumed to happen instantaneously) and the corresponding output transition. The output transition is assumed to complete only when the output voltage crosses the appropriate output voltage threshold. The propagation delay and the rise/fall times are usually not equal when the digital circuit consists of multiple stages. When a circuit consists of multiple stages, the rise/fall time at the output is usually a function of the properties of the output circuit alone. However, the propagation delay is the sum of the delays of each of the stages.

How does the propagation delay impact our digital abstraction? Notice that the slowly rising output of the inverter now spends a non-zero amount of time in the invalid output voltage range, namely $V_{IL} \rightarrow V_{IH}$. This appears to violate the static discipline. Recall that the static discipline requires that devices produce valid output voltages that satisfy the output thresholds when valid input voltages are supplied. We get around this difficulty by observing that the inverter output eventually crosses the valid output threshold. Furthermore, notice that the static discipline does not take a position on time. In other words, it does not require gates to produce valid outputs instantaneously if the inputs change. Accordingly, to make this fact explicit, we can modify the statement of the static discipline by requiring that devices produce valid output voltages (in a finite amount of time) that satisfy the output thresholds when valid input voltages are supplied.

Revised statement of the static discipline The static discipline is a specification for digital devices. The static discipline requires devices to interpret correctly voltages that fall within the input thresholds (V_{IL} and V_{IH}). Provided valid

7. The rise and fall times are sometimes defined slightly differently. For example, the rise time of a node that transitions from a low to a high voltage might be defined as the time taken by a signal at that node to rise from 5% to 95% of the change in voltage. Alternatively, the rise time can be defined as the time taken by a signal at that node to rise from a valid low voltage V_{OL} to a valid high voltage V_{OH} . As one more possibility, the rise time might be defined as the time taken by a signal to rise from its lowest value to 50% of the voltage difference. Corresponding definitions for the fall time also exist. The vagueness of these definitions only serves the interests of product marketers, but for us, the important thing to learn is how to calculate the time intervals between any pair of signal values.

inputs are provided to the devices, the discipline also requires the devices to produce valid output voltages (in a finite amount of time) that satisfy the output thresholds (V_{OL} and V_{OH}).

We can also refine our combinational gate abstraction to include the notion of a propagation delay, so that the abstraction remains valid in the presence of transitioning signals. Recall, the properties of a combinational gate as previously defined in Chapter 5.3: (1) The gate's outputs are a function of its inputs alone and (2) the gate must satisfy the static discipline. In the presence of a finite gate delay, there is a small period of time following an input transition in which the outputs do not reflect the new inputs; rather they reflect the old inputs. Thus our previously defined gate abstraction is violated. We negotiate this inconsistency by introducing a timing specification into our gate abstraction.

Revised statement of the combinational gate abstraction A combinational gate is an abstract representation of a circuit that satisfies these properties:

1. Its output will be valid no later than t_{pd} after an instantaneous change in its inputs.
2. Its outputs are a function of its inputs alone (after an interval of time no greater than t_{pd} following a change in its inputs).
3. It satisfies the static discipline.

Now that we have included the propagation delay of a device in its abstract specification, an additional benefit results: A gate-level circuit will now carry information on both its logic function and its speed. A rough estimate of the delay from any input to any output of a logic circuit along a path with multiple gates can be obtained by summing the propagation delays of each of the gates in that path. Thus, for example, if inverters are characterized by a t_{pd} of 1 ns and OR gates with a t_{pd} of 2 ns, then in the circuit in Figure 5.16 in Chapter 5, the delay from the input A to output C would be 2 ns, while the delay from the input B to output C would be 3 ns. If digital circuit designers need more accurate timing information for a circuit comprising multiple devices, or if they need to derive the t_{pd} of a single device, then they must use the analysis methods discussed in the ensuing sections.

10.4.2 COMPUTING t_{pd} FROM THE SRC MOSFET MODEL

Let us now compute the magnitude of the propagation delay. We use the switch-resistor-capacitor (SRC) model of the MOSFET introduced in Section 9.3.1 to determine this delay. Recall that we augmented the SR model of the MOSFET with a gate-to-source capacitor and created the SRCMOSFET model shown in Figure 10.17.

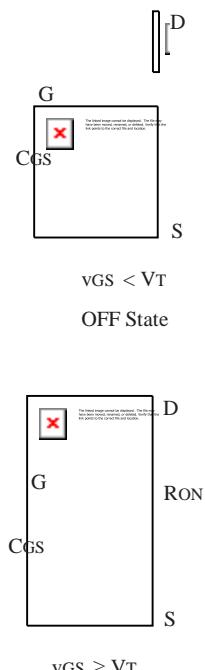


FIGURE 10.17 The switch-resistor-capacitor model of the MOSFET.

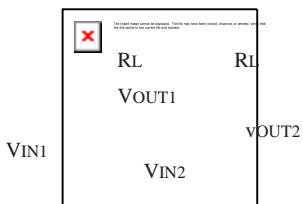


FIGURE 10.18 Internal circuits of the inverters.

Recall that the propagation delay results from the finite amount of time required for the output to transition from a given valid output voltage level to another when the input to the circuit transitions. The slower transition at the output is attributable to RC effects. Figure 10.18 replaces the inverters with their internal circuits comprising MOSFETs and resistors. Figure 10.19 further replaces the MOSFETs with their SRCCircuit model when VIN_1 applied to the inverter A corresponds to a logical 1. For this VIN_1 , the MOSFET in inverter A will be on, and the MOSFET in inverter B will be off. Similarly, Figure 10.20 shows the circuit model when VIN_1 applied to inverter A corresponds to a logical 0. For this VIN_1 , the MOSFET in inverter A will be off, and the MOSFET in inverter B will be on. Thus, when alternating logical 1's and 0's are applied to the input to the inverter pair, and the inverters are allowed to reach steady state after each transition, the equivalent circuit model alternates between the two circuits in Figures 10.19 and 10.20.

Let us first analyze the circuit qualitatively. Consider the case where VIN_1 has been high for a long period of time and focus on the part of the circuit bounded by the dashed box in the Figure 10.19, which includes the load resistor and R_{ON} of inverter A and the gate-to-source capacitor of inverter B. Since the circuit is in its steady state, the capacitor behaves as an open circuit, and so the voltage across the capacitor will be established by the voltage-dividersubcircuit comprising the supply V_s , and the resistors R_L and R_{ON} . Assuming $R_L \gg R_{ON}$, the capacitor voltage will have a low value (close to 0 volts).

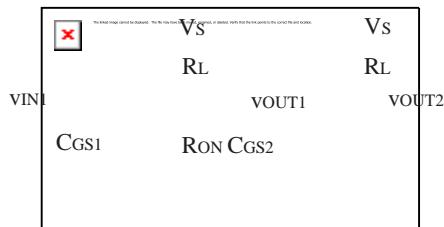


FIGURE 10.19 SRCCircuit model of inverters connected in series when the input is high.

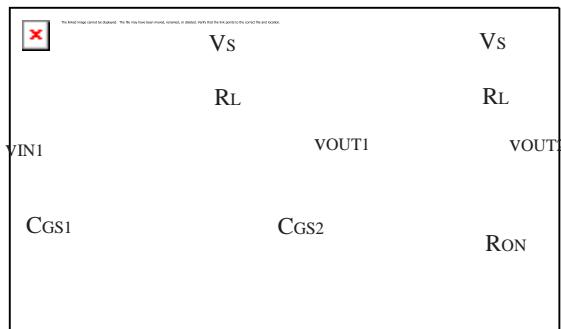


FIGURE 10.20 SRCCircuit model of inverters connected in series when the input is low.

Next, focus on the time instant when the input voltage V_{IN1} switches from a high to a low value (for example, 5 to 0 volts), turning the first MOSFET off. At this transition instant, the capacitor C_{GS2} is almost completely discharged (assuming that $R_L \gg R_{ON}$ for the inverters). Therefore, the voltage across C_{GS2} , which corresponds to the voltage V_{OUT1} on the output of inverter A, will be initially close to 0 V. This is depicted at the time instant A in Figure 10.16.

After the first MOSFET turns off, Figure 10.20 applies. Focus again on the part of the circuit bounded by the dashed box. It is easy to see that the circuit inside the dashed box is a first-order RC circuit. Remember, the voltage across C_{GS2} is low initially. Now, V_S begins to charge C_{GS2} through the resistor R_L . The equivalent RC circuit for the devices in the box are shown in Figure 10.21. As the capacitor charges up, the output voltage of inverter A rises. This voltage must rise above the valid logical output high threshold, namely V_{OH} , to satisfy the static discipline. Notice that although the second MOSFET will turn on when V_{OUT1} crosses its V_t threshold (for example, 1 V), we require V_{OUT1} to reach V_{OH} to achieve a modest noise margin. Notice that the presence of the capacitor C_{GS2} makes V_{OUT1} take a finite amount of time to rise to the required V_{OH} level. As we saw before, this interval of time is called the propagation delay for the inverter for a high-to-low transition at the input and is denoted by $t_{pd,1 \rightarrow \text{rise}}$.

time of the inverter.

Next, let us consider the time instant when the input voltage switches from 0 volts to 5 volts, turning the first MOSFET on. Let us assume that this 0-V-to-5-V transition happens after a sufficiently long period of time so that C_{GS2} is initially charged up to its steady-state value of 5 V. When the first gate is turned on, C_{GS2} begins to discharge. The RC circuit and its Thévenin equivalent for the discharge is shown in Figure 10.22. For the logical 0-to-logical 1 transition at the input to be reflected at the output of inverter A, the voltage across C_{GS2} needs to go below the valid logical output low threshold, V_{OL} . As before, although MOSFET B will turn off when V_{OUT1} drops below 1 volt, we require the output to go below V_{OL} to provide a adequate noise margin. The interval of time corresponding to the output capacitor discharge for an inverter is also called the propagation delay for the inverter for a low-to-high transition at the input and

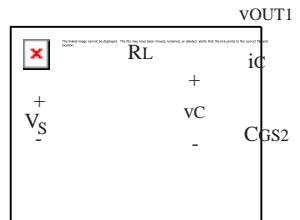
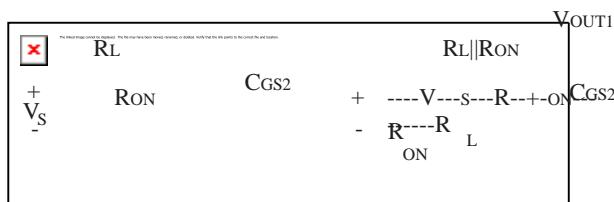


FIGURE 10.21 Equivalent circuit when C_{GS2} is charging.



(a) RC circuit model

(b) Thévenin equivalent network

FIGURE 10.22 Equivalent circuit when C_{GS2} is discharging.

is denoted by $t_{pd,0 \rightarrow 1}$. Furthermore, as stated previously, the output capacitor discharge time is also called the fall time of inverter A.

The propagation delay t_{pd} for inverter A is simply taken as the maximum of $t_{pd,0 \rightarrow 1}$ and $t_{pd,1 \rightarrow 0}$.

At this point, it is worth discussing a slight mismatch between the digital gate abstraction and the physical realities of computing the propagation delay. From the viewpoint of the digital gate abstraction, the propagation delay t_{pd} is a property of the digital gate. Accordingly, we might say that an inverter (for example, one identical to inverter A) always has a propagation delay of 2 ns. However, the example discussed thus far illustrates that the propagation delay of an inverter depends not only on the characteristics of its internal components, but also on the size of the capacitance that it is driving, and therefore the propagation delay of the inverter can change depending on its environment. In particular, the propagation delay of inverter A in our example depends on the input capacitance of inverter B. Thus, strictly speaking, it makes no sense to define the propagation delay of a device in isolation. However, for convenience, we would like to characterize devices with a single t_{pd} without defining their surrounding environment, so this simple device model can be used to obtain quick estimates of digital circuit delays when multiple gates are connected together. Accordingly, unless explicitly stated otherwise, device libraries or catalogs define a t_{pd} for a gate assuming it is driving a “typical” load — commonly, four minimum-sized inverters.⁸

Computing $t_{pd,0 \rightarrow 1}$

Let us now determine quantitatively the propagation delay for a low-to-high transition at the input of the inverter. Assume through the rest of this example that a valid output low voltage, V_{OL} , is 1 volt, and that a valid output high voltage, V_{OH} , is 4 volts. Also assume R_{ON} is 1 k, and that the threshold on-voltage for the MOSFET is 1 volt. Also assume that R_L is 10 k.

In this case, as discussed earlier, CGS₂ is initially charged to 5 volts. We need to determine the time taken for the capacitor voltage to drop from 5 to V_{OL} when $V_I = 1$ volt. The input is high. Figure 10.22 shows the equivalent circuit. Let us

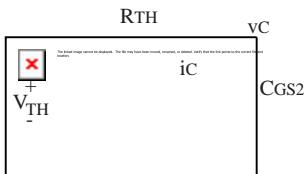


FIGURE 10.23 Equivalent circuit when CGS₂ is discharging.

denote the Thévenin equivalent resistance R_{LON} as R_{TH} , and the Thévenin equivalent voltage $V_{TH} = \frac{1}{2}(V_{OL} + V_{OH})$ as V_{TH} . Let us denote the capacitor voltage v_{OUT} by v_C , and the current through the circuit by i_C as shown in Figure 10.23.

8. A related metric that is sometimes used to characterize the speed of a process technology is called the fan-out-of-4 (or FO4) delay. The FO4 delay for a process technology is the propagation delay of a minimum-sized inverter driving four other inverters of the same size.

Using the node method, we obtain,

$$\frac{v_C - V_{TH}}{R_{TH}} + C_{GS2} \frac{dv_C}{dt} = 0.$$

Rearranging,

$$R_{TH} \frac{C_{GS2} dv_C}{dt} + v_C = V_{TH}. \quad (10.64)$$

Solving Equation 10.64 yields

$$v_C(t) = V_{TH} + A e^{-t/R_{TH}}. \quad (10.65)$$

Substituting the initial condition $v_C(0) = V_s$, we obtain the final solution:

$$v_C(t) = V_{TH} + (V_s - V_{TH}) e^{-t/R_{TH}}. \quad (10.66)$$

How long does it take for v_C to drop below 1 volt? To obtain this duration, we must solve for the value of t that satisfies

$$V_{TH} + (V_s - V_{TH}) e^{-t/R_{TH} C_{GS2}} < 1.$$

In other words,

$$t > -R_{TH} C_{GS2} \ln \frac{1 - V_{TH}}{V_s - V_{TH}}.$$

For $R_L = 10\text{k}$ and $R_{ON} = 1\text{k}$, $R_{TH} = 10000/11$, and $V_{TH} = V_s/11$.

Substituting $V_s = 5\text{V}$ and $V_{TH} = 5/11\text{V}$, the value of t must satisfy

$$t > -R_{TH} C_{GS2} \ln \frac{3}{25}.$$

Substituting for R_{TH} , the value of t must satisfy

$$t > -\frac{10000}{11} C_{GS2} \ln \frac{3}{25}. \quad (10.67)$$

Suppose the gate capacitance $C_{GS2} = 100\text{fF}$. We then have

$$t > -\frac{10}{11 \times 10^3 \times 100 \times 10^{-15} \times \ln(3/25)}$$

or,

$$t > 0.1928\text{ns}. \quad (10.68)$$

Thus $t_{pd,0 \rightarrow 1} = 0.1928\text{ ns}$.

Computing $t_{pd,1 \rightarrow 0}$

When the input V_{IN1} goes low, the circuit model that applies is shown in Figure 10.21. In this case, we know that initial voltage V_C0 on the capacitor is determined by the voltage-divider relationship:

$$V_{C0} = \frac{V_{sRON}}{R_{ON} + R_L} = 5/11 \text{ V.}$$

Our goal is to solve for the time it takes for the capacitor to charge up to $V_{OH} = 4$ volts. We obtain the following using the node method (writing v_C in place of v_{OUT1}),

$$\frac{v_C - V_s}{R_L} + C_{GS2} \frac{dv_C}{dt} = 0.$$

Rearranging, we get

$$RLC_{GS2} \frac{dv_C}{dt} + v_C = V_s. \quad (10.69)$$

Solving Equation 10.69 yields

$$v_C(t) = V_s + A e^{-t/RLC_{GS2}}. \quad (10.70)$$

Using the initial condition, we get

$$v_C(t) = V_s + (V_{C0} - V_s) e^{-t/RLC_{GS2}}, \quad (10.71)$$

substituting, $V_{C0} = 5/11 \text{ V}$ and $V_s = 5 \text{ V}$,

$$v_C(t) = 5 - (50/11) e^{-t/RLC_{GS2}}. \quad (10.72)$$

How long does it take for v_C to go above $V_{OH} = 4 \text{ V}$ from an initial $5/11 \text{ V}$? To determine the delay, we must solve for the time that satisfies

$$5 - (50/11) e^{-t/RLC_{GS2}} > 4.$$

Simplifying, we get

$$t > -RLC_{GS2} \ln(11/50). \quad (10.73)$$

In other words,

$$t > -10 \times 10^3 \times 100 \times 10^{-15} \ln(11/50) \quad (10.74)$$

$$t > 1.5141 \text{ ns.}$$

The delay $t_{pd,1 \rightarrow 0}$ is thus 1.5141 ns.

Notice the RLCGS2 factor in Equation 10.73. In typical circuits, a ballpark estimate of the delay can be obtained by simply taking the product of the capacitance and the effective resistance through which it charges. In our case,

$$t_{pd,1 \rightarrow 0} \approx RLCGS2 = 10 \times 10^3 \times 100 \times 10^{-15} = 1 \text{ ns.}$$

Similarly, the ballpark estimate of $t_{pd,0 \rightarrow 1}$ is given by $t_{pd,0 \rightarrow 1} \approx R_{TH} C = 10/11 \times 10^3 \times 100 \times 10^{-15} = 0.09 \text{ ns.}$

Computing t_{pd}

By your definition, the propagation delay of the gate t_{pd} is the greater of the rising and falling delays. In other words,

$$t_{pd} = \max(t_{pd,0 \rightarrow 1}, t_{pd,1 \rightarrow 0})$$

Therefore, $t_{pd} = 1.5141 \text{ ns.}$

example 10.1 wire length on a vlsi chip In this example, we will examine how wire length becomes an important issue in the design of VLSI chips. Consider the inverter pair circuit in Figure 10.14. Suppose the two inverters are on the opposite ends of a chip that is 1 cm on a side. The resulting long wire connecting them cannot longer be treated as an ideal conductor with no resistance or capacitance. Instead we must replace the wire with an ideal wire in combination with a wire capacitance and a wire resistance. The resulting RC delays can be significantly higher than the RC delays of inverters connected to each other with short wires.

Figure 10.24 depicts graphically the wire connecting the two inverters on the VLSI chip. Assume the wire is of length L and width W . The MOSFETs have gate lengths L_g and gate widths W_g . Since the length of the wire is significant, we need to model it carefully. Let the wire resistance be denoted R_{wire} and the wire capacitance C_{wire} . The circuit model for the inverter pair taking into account wire parasitics is shown in Figure 10.25.

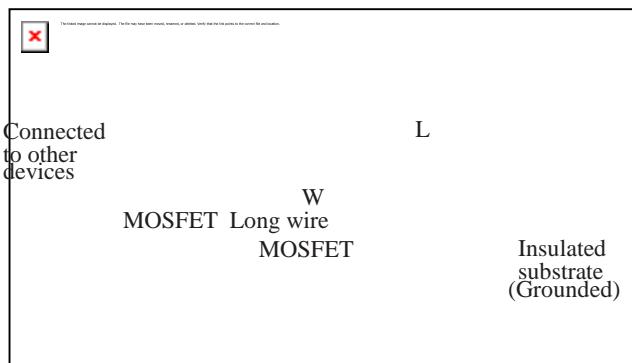
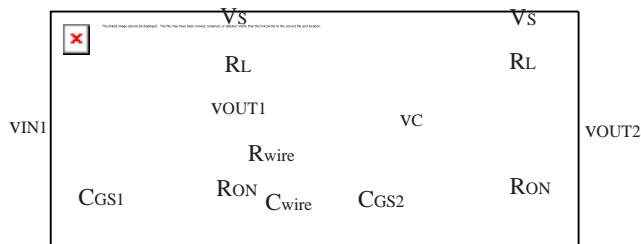


FIGURE 10.24 Longwire on a VLSI chip.

FIGURE 10.25 Circuit model of long wire on a VLSI chip.



(Here we assume that the parasitic inductance of the wire according to the model in Figure 9.7 in Chapter 9 is zero.)

If the sheet resistance of the wire is R_P (see Equations 1.10 and 1.9), we know,

$$R_{\text{wire}} = (L/W)R_P.$$

Similarly, if C_o is the capacitance per unit area of the wire, (formed between the wire, insulation, and the grounded substrate), we know

$$C_{\text{wire}} = LWC_o.$$

Clearly, the longer the wire, the larger its capacitance and resistance. Recalling that delays are related to the RC time constants, notice that the RC product for the wire is

$$R_{\text{wire}}C_{\text{wire}} = (L/W)R_P \times LWC_o = L^2R_P C_o.$$

The L^2 term in the RC product implies that wire delays grow as the square of wire lengths. Assume that the wire is 1 μm wide and 1000 μm long. Further, assume R_P is 2 and C_o is $2\text{fF}/\mu\text{m}^2$. Therefore,

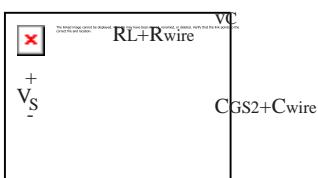


FIGURE 10.26 Charging the wire capacitor on a VLSI chip.

$$R_{\text{wire}}C_{\text{wire}} = 1000 \times 2 = 2\text{k}$$

and

$$C_{\text{wire}} = 1000 \times 2\text{fF} = 2\text{pF}.$$

The RC time constant for the wire is

$$R_{\text{wire}}C_{\text{wire}} = 2 \times 10^3 \times 2 \times 10^{-12} = 4\text{ns}.$$

Figures 10.26 and 10.27 show the relevant circuit models for charging and discharging the wire capacitance C_{wire} and gate capacitance C_{GS2} . Let us assume values for V_{OL}

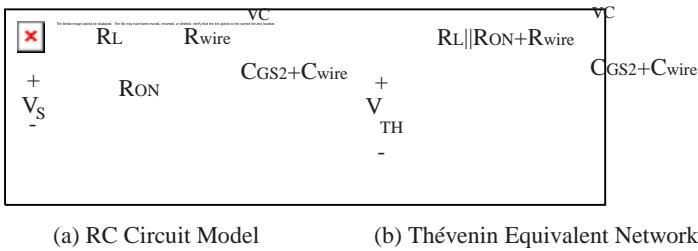


FIGURE 10.27 Discharging the wirecapacitor on a VLSI chip.

and V_{OH} to be the same as those used in Section 10.4.2. In other words, $V_{OH} = 4V$ and $V_{OL} = 1V$.

When the input V_{IN1} transitions from high to low, Figure 10.26 applies, and we can use the results from Section 10.4.2 to compute the propagation delay $t_{pd,1 \rightarrow 0}$ by using $(R_L + R_WIRE)$ in place of R and $(C_GS2 + C_WIRE)$ in place of C_GS2 . Thus, the propagation delay for $R_L = 10k\Omega$, $R_{ON} = 1k\Omega$, $C_GS2 = 100fF$ is given by

$$\begin{aligned} t_{pd,1 \rightarrow 0} &= -(R_L + R_WIRE) \times (C_GS2 + C_WIRE) \ln(11/50) \\ &= -(10+2) \times 10^3 \times (100+2000) \times 10^{-15} \times \ln(11/50). \end{aligned}$$

Thus,

$$t_{pd,1 \rightarrow 0} = 38.15\text{ns.} \quad (10.75)$$

When the input V_{IN1} makes a low to high transition, Figure 10.27 applies, and we can use the results from Section 10.4.2 to compute the propagation delay $t_{pd,0 \rightarrow 1}$ with $(R_L R_{ON} + R_WIRE)$ in place of R_T and $(C_GS2 + C_WIRE)$ in place of C_GS2 . For $R_{ON} = 10k\Omega$, $R_{ON} = 1k\Omega$, $C_GS2 = 100fF$, we get:

$$\begin{aligned} t_{pd,0 \rightarrow 1} &= -(R_L R_{ON} + R_WIRE)(C_GS2 + C_WIRE) \ln(3/25) \\ &= -\frac{10}{11} + 2 \times 10^3 \times (100+2000) \times 10^{-15} \times \ln(3/25), \end{aligned}$$

or,

$$t_{pd,0 \rightarrow 1} = 12.9\text{ns.} \quad (10.76)$$

Thus, we see that $t_{pd,0 \rightarrow 1} = 12.9\text{ns}$, which is significantly higher than the delay when the wire effects were not included.

Choosing the larger of the rise and fall delays, we observe that $t_{pd} = 38.15\text{ns}$. Clearly, the wire delay has increased the circuit delay by more than an order of magnitude.

10.5 STATE AND STATE VARIABLES

10.5.1 THE CONCEPT OF STATE

Capacitors and inductors can be discussed from a somewhat different point of view, one that emphasizes the memory aspect of the devices, as introduced in Equation 9.13 in Section 9.1.1. This section introduces an analysis of capacitor and inductor circuits based on their state, and will show how that this representation facilitates computer analysis of circuits, which is particularly useful when the circuit is nonlinear or it contains a large number of storage elements.

Let us begin by quickly reviewing the concept of state. If we apply an arbitrary current waveform to a capacitor, as in Figure 10.28, then the charge on the capacitor, and hence the capacitor voltage will be the integral of that current, as indicated in the figure.

$$q(t) = \int_{-\infty}^t i(t)dt. \quad (10.77)$$

It might at first appear that to perform this integral we need to know the complete current waveform from $t = -\infty$. Not so. All we need is the charge (or voltage, since $q = Cv$) at one time, and the current waveform thereafter. If the charge at $t = t_0$ is $q(t_0)$, then from Equation 10.77 the charge at some time t

2

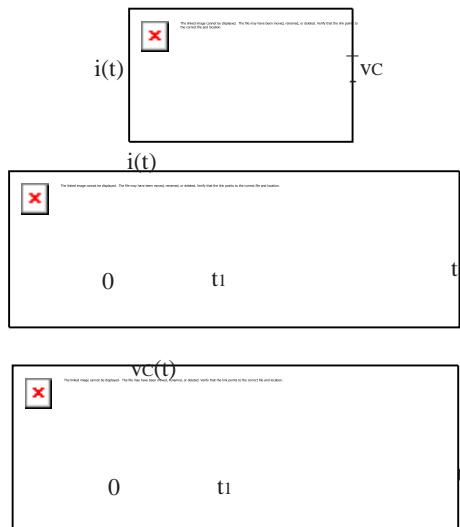


FIGURE 10.28 Voltage as a state variable.

greater than i is

$$q(t_2) = \int_{-\infty}^{t_1} i(t) + \int_{t_1}^{t_2} i(t) dt \quad (10.78)$$

$$= q(t_1) + \int_{t_1}^{t_2} i(t) dt. \quad (10.79)$$

All of the relevant past history of the circuit prior to t_1 is summarized in one value, $q(t_1)$. Variables that have this property are called state variables. Thus Equation 10.79 indicates that if we know the value of the state variable at one time, and the value of the input variable thereafter, we can find the value of the state variable for any subsequent time.

For linear time-invariant capacitors, the capacitor voltage is also a state variable, because

$$q = Cv.$$

For an inductor, the fundamental state variable is the total flux linked by the inductor, λ . Recall from Equation 9.32, if the inductor is linear and time-invariant, the current is equally appropriate as a state variable since it is linearly related to λ as

$$i = L\dot{\lambda}.$$

From this point of view, the first-order differential equations for the RC and RL circuits, Equations 10.2, 10.42, and 10.46 can all be written as state equations

$$\underline{d}t_d(\text{state variable}) = f(\text{state variable}, \text{input variable}). \quad (10.80)$$

For the linear case, f is a linear function, so Equation 10.80 becomes

$$\underline{d}t_d(\text{state variable}) = K_1(\text{state variable present value}) + K_2(\text{input variable}). \quad (10.81)$$

For example, consider Equation 10.2 for the circuit in Figure 10.2a:

$$\frac{dvc}{dt} + \frac{vc}{RC} = \frac{i(t)}{C}$$

This equation can be written in the canonical state equation form of Equation 10.81 as

$$\frac{dv}{dt} + \frac{v}{RC} = -\frac{R}{C}vc + \frac{i(t)}{C} \quad (10.82)$$

where the only state variable is vc .

10.5.2 COMPUTER ANALYSIS USING THE STATE EQUATION

One advantage of the state equation formulation is that even in the nonlinear case, the equations can be readily solved on a computer.⁹ If the input signal and the initial value of the state variable are known, then the slope of the state variable, that is,

$$\frac{dv}{dt}(state\ variable)$$

can be found from Equation 10.81. The value of the state variable at time $t+tc$ can now be estimated by standard numerical methods (Euler's method, Runge-Kutta, etc.). The process can now be repeated until the entire waveform is found.

Continuing with our example in Equation 10.82, suppose that the input signal $i(t)$ is known for all time. Also, suppose that the value of the state variable at time $t=t_0$, namely $v_C(t_0)$, is known. Then, Euler's method¹⁰ approximates the value of the state variable at time $t=t_0 + ta^0$

$$v_C(t_0 + t) = v_C(t_0) - \frac{v_C(t_0)}{RC} t + \frac{i(t_0)t}{C} \quad (10.83)$$

The value of v_C at time $t=t_0 + 2t$ can be determined in like manner from the value of $v_C(t_0 + t)$ and $i(t_0 + t)$. Subsequent values of v_C can be determined using the same process. By choosing small enough values of t , a computer can determine the waveform for $v_C(t)$ to an arbitrary degree of accuracy. This process illustrates the fact that the initial state contains all the information that is necessary to determine the entire future behavior of the system from the initial state and the subsequent input.

This procedure works even for circuits with many capacitors and inductors, linear or nonlinear, because these higher-order circuits can be formulated in terms of a set of first-order state equations like Equation 10.80, one for each energy-storage element (with an independent state variable) in the network. Chapter 12 discusses such an example in Section 12.10.1.

9. To build intuition, we will describe a simple computer method here. However, we note that other more efficient methods are employed in practice.

10. Euler's method is based on the following discrete approximation:

$$\frac{dv_C(t)}{dt} \approx \frac{v_C(t+t) - v_C(t)}{t}$$

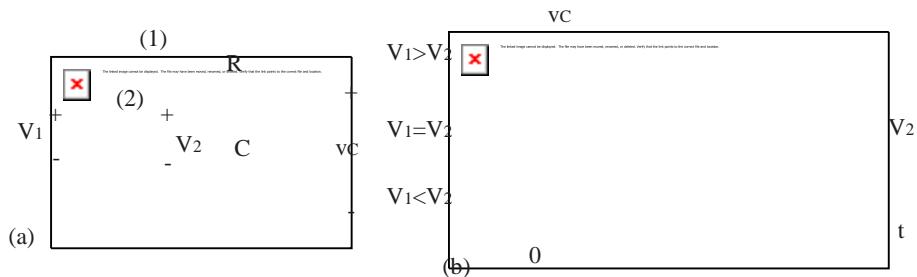


FIGURE 10.29 Transientwith
initialchargeoncapacitor.

10.5.3 ZERO-INPUT AND ZERO-STATE RESPONSE

Another advantage of the state variable point of view is that it allows us to solve transient problems by superposition. Specifically, we find first the zero-input response, the response for the true initial conditions, with the input drive zero. Then we find the zero-state response, the response of the circuit when the initial state is zero, that is, all capacitor voltages and inductor currents are initially zero. The total response is the sum of the zero-input response (ZIR) and the zero-state response (ZSR).

Relating these ideas to Equation 10.81, finding the zero-input-response involves solving the equation:

$$\frac{d}{dt}(state\ variable) = K_1(state\ variable\ present\ value) \quad (10.84)$$

using the true initial conditions for the state variable. Finding the zero-state-response involves solving the equation:

$$\frac{d}{dt}(state\ variable) = K_1(state\ variable\ present\ value) + K_2(input\ variable) \quad (10.85)$$

with the initial value of the state variable set to 0.

Let us illustrate these ideas with an example. The circuit shown in Figure 10.29a contains a switch, which is moved from position (1) to position (2) at $t = 0$. If the switch has been in position (1) for a long time, the capacitor will be charged to the voltage V_1 . That is, the initial condition for the circuit is

$$V_C = V_1 \quad t < 0. \quad (10.86)$$

When the switch is moved to position (2), there will be a transient charge (or discharge) until the capacitor voltage reaches a new steady state.

The governing differential equation is the same as the previous capacitor example in Section 10.1.4, Equation 10.42:

$$v_i = RC \frac{dv_C}{dt} + v_C. \quad (10.87)$$

Writing the same equation in canonical state equation form, we get

$$\frac{dv_C}{dt} = -\frac{RC}{+} v_C + \frac{V_1}{RC}. \quad (10.88)$$

First, let us first solve for the capacitor voltage directly by finding the homogeneous solution and particular solution. We will then derive the capacitor voltage by obtaining the ZIR and ZSR.

The homogeneous solution is

$$v_C = A e^{-t/RC}. \quad (10.89)$$

By inspection from Equation 10.89, the particular solution must be

$$v_C = V_2. \quad (10.90)$$

The complete solution is the sum of these two:

$$v_C = A e^{-t/RC} + V_2. \quad (10.91)$$

Equating Equation 10.91 at $t=0$ to the stated initial condition, Equation 10.86,

$$v_C = V_1 = A + V_2. \quad (10.92)$$

$$A = V_1 - V_2. \quad (10.93)$$

Hence the complete solution for $t > 0$ is

$$v_C = V_2 + (V_1 - V_2)e^{-t/RC}. \quad (10.94)$$

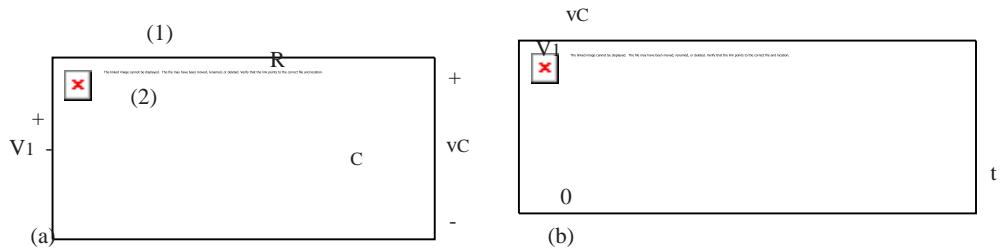
Plots of this result are shown in Figure 10.29b. As indicated, the response depends on the relative size of V_1 and V_2 . For one particular value, namely $V_1 = V_2$, there is no transient, as is obvious from physical considerations.

In Equation 10.94 the first term is the particular solution, and the second is the homogeneous solution.

Next, to obtain insight into the method involving the ZIR and ZSR, a trivial rewrite of Equation 10.94 yields

$$v_C = V_1 e^{-t/RC} + V_2 (1 - e^{-t/RC}). \quad (10.95)$$

Now the first term is the response to an initial state, in this case an initial capacitor, and no input. This we call the zero-input response (ZIR). The second



term is the response to an external input, for no initial capacitor charge: the zero-state response (ZSR).¹¹ To verify, let us now solve directly for the ZIR and the ZSR by superposition.

The subcircuit for finding the ZIR is shown in Figure 10.30a. As before, the capacitor is initially charged to \$V_1\$, but here the input for \$t > 0\$ is zero, so after the switch moves to position (2), the capacitor simply discharges to zero. Formally, the corresponding equation to be solved to obtain the ZIR is

$$\frac{dv}{dt} = -RC v_C \quad (10.96)$$

with the initial condition on the capacitor voltage being \$V_1\$.

The homogeneous solution is

$$v_C = V_1 e^{-t/RC}. \quad (10.97)$$

This is the complete zero-input response, because the particular solution is zero.

The subcircuit for finding the zero-state response is shown in Figure 10.31a. The corresponding equation to be solved to obtain the ZSR is

$$\frac{dv}{dt} = -RC v_C + \frac{V_1}{RC}. \quad (10.98)$$

with the initial condition on the capacitor voltage chosen as 0.

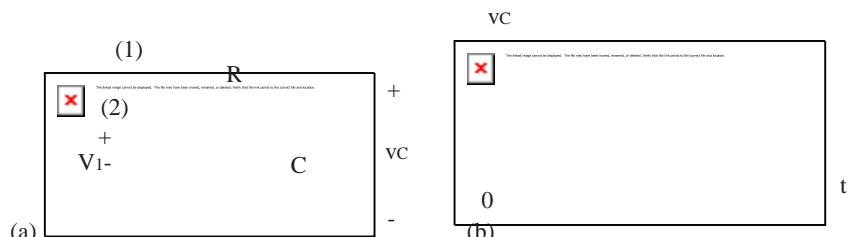


FIGURE 10.30 Zero-input subcircuit and response.

¹¹Notice the similarity between this and Equation 10.62.

FIGURE 10.31 Zero-state subcircuit and response.

The homogeneous solution is as in Equation 10.89, and the particular solution is again V_2 , so the solution is of the form

$$v_C = A e^{-t/RC} + V_2. \quad (10.99)$$

This time by definition the initial condition is zero, so evaluating right after the switch is thrown,

$$0 = A + V_2 \quad (10.100)$$

and the complete zero-state response for $t > 0$ is

$$v_C = V_2(1 - e^{-t/RC}). \quad (10.101)$$

The total response is the sum of the ZIR and ZSR from Equations 10.101 and 10.97 and is given by

$$v_C = V_1 e^{-t/RC} + V_2(1 - e^{-t/RC}). \quad (10.102)$$

Observe that Equation 10.102 agrees with the formulation of Equation 10.94.

Comments

The particular solution and the homogeneous solution are terms which apply to a method of solving differential equations.

Zero-input and zero-state responses arise from a particular way of partitioning the circuit problem into two simpler subproblems. The resulting subcircuits can be solved by finding the homogeneous solution and particular solution in each case.

For the ZIR, the particular solution will by definition be zero. Hence all ZIRs will be homogeneous solutions.

But all ZSRs are not particular solutions, because there is also a homogeneous solution associated with the ZSR. The $e^{-t/RC}$ term in Equation 10.101 is an example of this.

A major advantage to the state variable point of view is that any arbitrary ZIR can be added to any ZSR solution we have already worked out. Thus any transient problem with zero initial conditions can be easily generalized to one with arbitrary initial conditions. This concept will be illustrated in the examples in Section 10.6.

10.6 ADDITIONAL EXAMPLES

10.6.1 EFFECT OF WIRE INDUCTANCE IN DIGITAL CIRCUITS

Section 10.4 showed that RC effects lead to propagation delay in digital circuits. It turns out that when parasitic inductors are present, RL effects can be a similar source of propagation delay. Consider the inverter circuit shown in Figure 10.32a. Assume that a poor design has resulted in a long wire connecting the MOSFET drain to the output of the inverter. A circuit model of the inverter showing the parasitic wire inductance is depicted in Figure 10.32b.

Assume that the inverter has a 0-V input as an initial condition. The MOSFET is in its off state and the current i_L through the inductor L will be 0. The voltage v_L across the inductor is also 0. Now suppose that a 0-V to V_s -step is applied to the input of the inverter as illustrated in Figure 10.32a. Assume that our goal is to determine the current i_L through the inductor and the voltage v_L across the inductor as a function of time.

The step input to the inverter results in a corresponding V_s -step applied to the RL circuit at the output of the inverter as illustrated in Figure 10.32c. From the initial conditions, at $t=0$, both i_L and v_L are 0. From this point on, the situation is identical to that for the RL transient discussed in Section 10.2.1 with V_u used in place of V_s . Therefore the analysis presented in Section 10.2.1 applies.

It is interesting to speculate as to what will happen if the switch in Figure 10.32c is opened after being closed for a long time. When the switch is opened, the inductor current cannot go to zero instantaneously. Since a practical open switch behaves as an extremely high resistance, the current through the inductor will result in a huge voltage spike across the switch, and possibly damage it.

10.6.2 RAMP INPUTS AND LINEARITY

Solutions become somewhat more complicated when we move beyond simple step inputs. Consider the case of a series RC circuit with a voltage ramp drive,

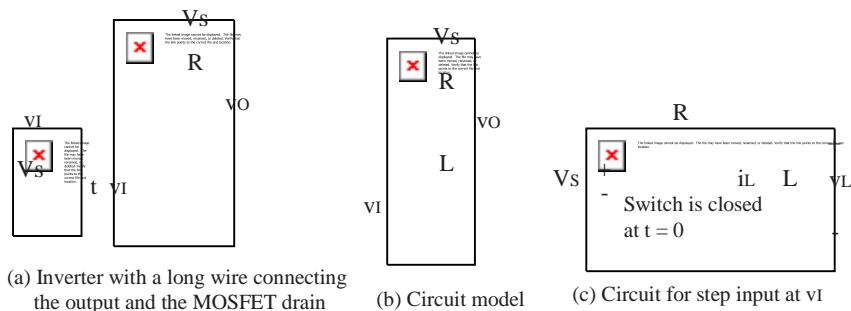


FIGURE 10.32 Inverter circuit with parasitic inductance.

that is

$$v_I = S_1 t \quad t > 0 \quad (10.113)$$

where S_1 has the dimensions of volts per second. The circuit and input waveform are sketched in Figures 10.33a and b. Let us first find the zero-state response, by assuming that the capacitor is initially uncharged. The differential equation is, from before,

$$v_I = S_1 t = RC \frac{dv_C}{dt} + v_C \quad (10.114)$$

We will solve this using our usual method of homogeneous and particular solutions. The homogeneous solution has the usual form:

$$v_C = A e^{-t/RC} \quad (10.115)$$

This homogeneous solution is plotted in Figure 10.33c. We must now find a particular solution that is appropriate for a ramp input. Because the drive is a ramp, a good first guess is a ramp of the same slope as the input:

$$v_C = K_2 t \quad (10.116)$$

Substituting this into the differential equation, Equation 10.114, we obtain

$$S_1 t = R C K_2 + K_2 t \quad (10.117)$$

Because there is no solution for K_2 unless $RC = 0$, our initial guess for the particular solution is not quite correct. We need another degree of freedom in the solution, so an appropriate second guess is

$$v_C = K_2 t + K_3 \quad (10.118)$$

Now from Equation 10.114:

$$S_1 t = R C K_2 + K_2 t + K_3 \quad (10.119)$$

Whence

$$S_1 = K_2 \quad (10.120)$$

$$K_3 = -S_1 RC \quad (10.121)$$

and the particular solution is

$$v_C = S_1(t - RC) \quad (10.122)$$

This is a ramp with the same slope as the input ramp, except delayed in time by one time constant, as shown in Figure 10.33d.

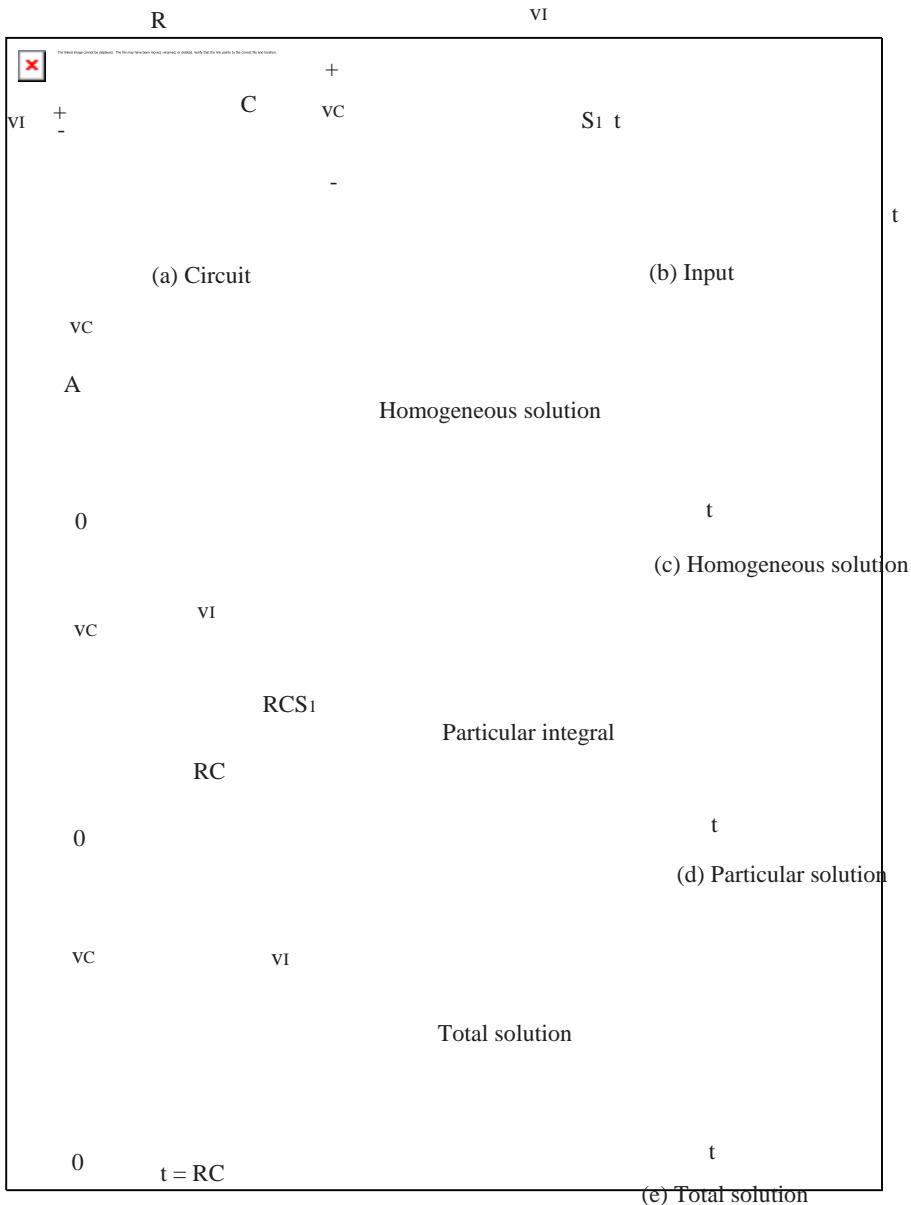


FIGURE 10.33 Response of RC circuit to a ramp.

The complete solution is of the form

$$v_C = A e^{-t/RC} + S_1(t - RC) \quad \text{for } t > 0. \quad (10.123)$$

Because we are finding the zero-state response, the initial condition is by definition zero, so evaluating Equation 10.123 at $t=0$, we find

$$A = S_1 RC.$$

Hence the complete solution for $t > 0$ is

$$v_C = S_1(t - RC) + S_1 RC e^{-t/RC} \quad (10.124)$$

and is plotted in Figure 10.33e.

The waveforms in Figures 10.33b and 10.33e are related in a special way to those in Figures 10.2b and 10.2c. Note first that the input signal in this problem is the integral of the input signal in Figure 10.2 (assuming a Thévenin source). Now, from Figures 10.33e and 10.2c, or from Equations 10.124 and 10.20, the output signal here is the integral of the output signal in Figure 10.2, ¹² again, assuming that we are dealing with the zero-state response.

In general, as long as one restricts integral operation to gt greater than zero, the zero-state response of the integral of some input signal is the integral of the zero-state response to that signal.

This follows from superposition if one considers integration as a summation process. In effect we are commuting two linear operators. The same is true for differentiation as well:

The response to a signal derived by differentiating an input can be obtained by differentiating the output.

Let us follow this example one step further, and consider the case where there is an initial voltage V_0 on the capacitor at $t = 0$, before the ramp is applied.

12. Notice that if we take the integral of Equation 10.20, namely,

$$v_C = I_0 R (1 - e^{-t/RC})$$

we obtain

$$v_C = I_0 R t + I_0 R R C e^{-t/RC} + K_1$$

where, to get the zero initial condition on v_C , we set the constant of integration $K_1 = -I_0 R R C$, and obtain

$$v_C = I_0 R (t - RC) + I_0 R R C e^{-t/RC},$$

which is a Thévenin inversion of Equation 10.124.

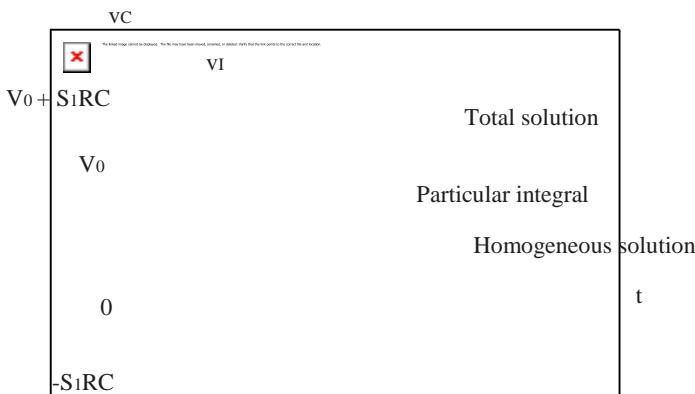


FIGURE 10.34 Ramp response for initial charge on capacitor.

Formally, the initial condition now is

$$v_C = V_0 \quad t < 0. \quad (10.125)$$

This time around, since there is an initial condition on the capacitor, we are no longer dealing with just the zero-state response, so we cannot simply take the integral. One approach is to notice that Equation 10.124 is in effect the zero-state response, so if we find the zero-input response corresponding to the initial condition of Equation 10.125, then the complete solution is the sum of these two responses. We know from previous examples, or from Equation 10.97, that the ZIR for an RC circuit with an initial voltage V_0 is

$$v_C = V_0 e^{-t/RC} \quad (10.126)$$

so the total solution for $t > 0$ is

$$v_C = V_0 e^{-t/RC} + S_1 t - S_1 RC(1 - e^{-t/RC}). \quad (10.127)$$

One possible form of this solution is sketched in Figure 10.34. This example illustrates one of the advantages of the state-variable approach. Once we have found the solution for some input wave form and zero initial conditions, the solution for the same input with arbitrary initial conditions can be found by adding the appropriate ZIR solution.

example 10.2 tv deflection system

Most television sets use magnetic deflection in the cathode-ray tube. To obtain the raster scan for the picture, it is necessary to develop a ramp of current flowing through the deflection coil, as sketched in Figure 10.35. We wish to find the required waveform of v_i that will

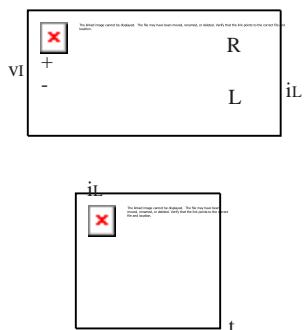


FIGURE 10.35 TV deflection coil.

generate the current ramp. The coil losses have been explicitly modeled in Figure 10.35 by the resistor R .

The differential equation for the circuit is, from KVL

$$v_L = iR + L \frac{di}{dt} \quad (10.128)$$

We want a current waveform, for $t > 0$, of the form

$$i = S_1 t. \quad (10.129)$$

Hence

$$(10.130)$$

$$v_L = S_1 R t + S_1 L$$

for $t > 0$. Thus to produce a ramp of current in the inductor, we need to drive with the sum of a fast step and a ramp.



example 10.3 solution by integrating factors

10.6.3 RESPONSE OF AN RC CIRCUIT TO SHORT PULSES AND THE IMPULSE RESPONSE

It was shown in Section 10.1.4 that when the time constant of an RC circuit becomes much longer than the period of a periodic input signal, the capacitor voltage begins to approximate the integral of the input wave. Let us examine this property in more detail by finding the response of the RC circuit in Figure 10.36 when the input is a short pulse of amplitude V_p and duration t_p .

We have seen several problems of this sort, so the general form of the capacitor voltage can be written by inspection. Assuming that the capacitor is initially uncharged, the response during the pulse, when the capacitor is charging is

$$v_C = V_p \left(1 - e^{-t/RC} \right) \quad 0 \leq t \leq t_p. \quad (10.135)$$

If t_p is long enough for this transient to essentially get to completion, then at $t = t_p$, the end of the pulse, the capacitor voltage will be V_p . The response after the pulse has ended, when the capacitor is discharging, is thus

$$v_C = V_p e^{-(t-t_p)/RC} \quad t \geq t_p. \quad (10.136)$$

The $-t_p$ factor in the exponent indicates that there is a time delay in the start of the wave of an amount t_p . This solution is shown in Figure 10.36b.

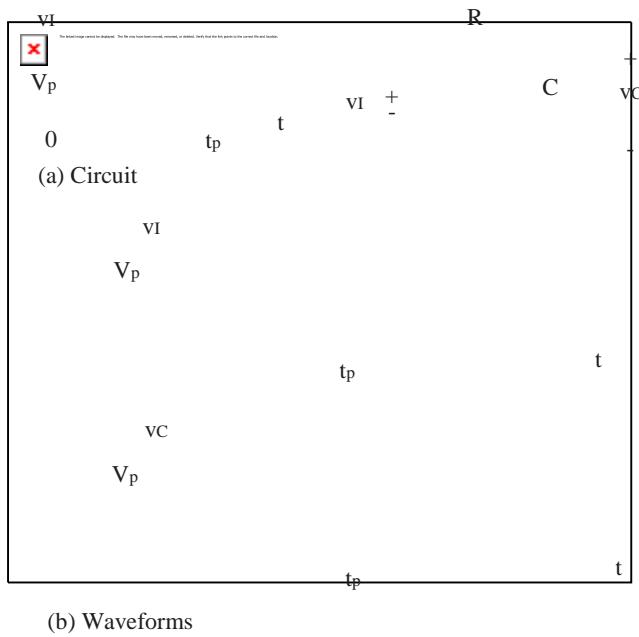


FIGURE 10.36 Response of RC circuit to pulse.

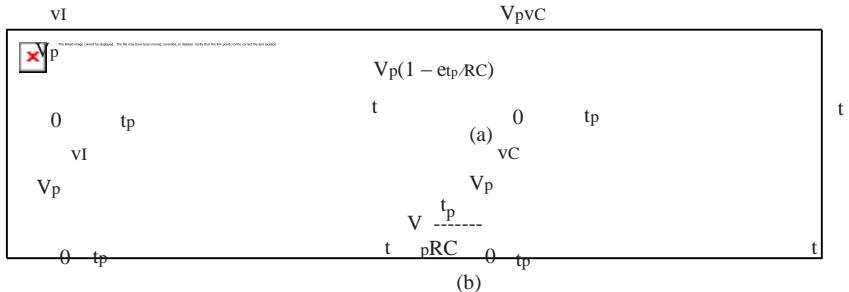


FIGURE 10.37 Response of RC circuit to short pulse.

If the pulse is made shorter than in Figure 10.36, the charging transient can no longer reach completion. This is illustrated in Figure 10.37a. Equation 10.135 is still appropriate for the charging interval, but the response no longer reaches V_p . The maximum value, at $t = t_p$, is

$$v_C(t_p) = V_p \left(1 - e^{-t_p/RC}\right). \quad (10.137)$$

The discharge now has essentially the same form as before, but is smaller. That is, for $t > t_p$, the capacitor voltage is

$$v_C = V_p \left(1 - e^{-t_p/RC}\right) e^{-(t-t_p)/RC}. \quad (10.138)$$

If we make the pulse even shorter yet, as in Figure 10.37b, the picture actually becomes simpler. The charging part of the wave begins to look almost like a straight line. Mathematically, this can be shown by expanding the exponential in a series

$$e^{-x} = \frac{1}{1+x} = 1 - x + \frac{x^2}{2!} - \dots \quad (10.139)$$

when the charging waveform becomes, from Equation 10.135

$$v_C = V_p \left(1 - \frac{t}{RC} - \frac{1}{2} \left(\frac{t}{RC} \right)^2 + \dots \right) \quad (10.140)$$

For times much less than the time constant RC , that is, $t \ll RC$, we can discard all higher terms, leaving

$$v_C \approx V_p R C t \quad (10.141)$$

which is the equation for the straight line we observe in the first part of Figure 10.37b.

Physically, when the pulse is very short the capacitor voltage is always much smaller than the pulse voltage, so during the pulse the current is roughly constant at a value

$$i_C \approx V_p R \quad (10.142)$$

The capacitor voltage is the integral of this current, hence is a ramp:

$$v_C = \frac{1}{C} \int i_C dt = \frac{1}{C} V_p R t \quad (10.143)$$

$$V_p R C t \quad (10.144)$$

At the end of the pulse, the capacitor voltage has reached its maximum value of

$$v_C(t_p) = \frac{V_p t_p}{R C} \quad (10.145)$$

so the discharge waveform for $t > t_p$ is

$$v_C = \frac{V_p t_p}{R C} e^{-\frac{(t-t_p)}{R C}} \quad (10.146)$$

The important feature of this equation is that the response is now proportional to the area ($V_{p\text{tp}}$), rather than the height (V_p), of the input pulse. In other words,

$$v_C = \frac{\text{Area of Pulse}}{RC} e^{-(t-t_p)/RC}. \quad (10.147)$$

For very short pulses (that is, for $t_p \ll RC$), even the delay term in the exponent can be neglected, and the response reduces to

$$v_C = \frac{A}{RC} e^{-t/RC}. \quad (10.148)$$

Because in the limit ($t_p \ll RC$) a short pulse of large amplitude but constant area becomes an impulse (see Section 9.4.3) Equation 10.148 is often referred to as the impulse response of the circuit. In other words, if we have an impulse voltage input with area (or strength) A

$$v_I(t) = A\delta(t),$$

the response is given by

$$v_C = \frac{A}{RC} e^{-t/RC}. \quad (10.149)$$

Figure 10.38 sketches the impulse voltage input and the corresponding response according to Equation 10.148.

The impulse response is a very convenient way of characterizing linear systems, because the expression contains all of the essential information about the dynamics of the system. This concept is pursued in depth in courses on signals and systems.

10.6.4 INTUITIVE METHOD FOR THE IMPULSE RESPONSE

The intuitive method discussed in Section 10.3 applies equally well for impulse responses. Shown in Figure 10.39a is our familiar parallel source-resistor-capacitor circuit from Figure 10.2a. Suppose that the current input is an impulse of area Q that is applied at $t=0$ as shown in Figure 10.39b. Assume we wish to find the capacitor voltage v_C .

As discussed in Section 10.3, we will first sketch the form of the response in the t -initial us start interval by looking ($t < 0+$) and the initial the final interval. interval For ($t < 0, 0$). the current source supplies zero current and hence behaves like an open circuit. Assuming that this situation has existed for a long time, the capacitor will have no charge on it, and hence v_C will be 0. If the capacitor voltage were non-zero, there would be

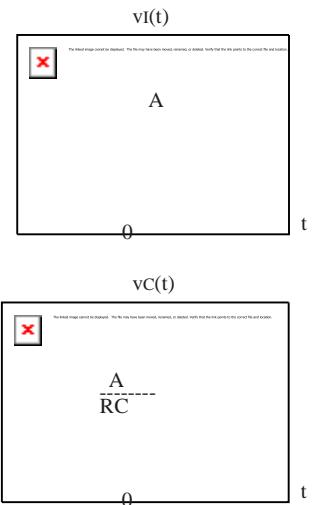


FIGURE 10.38 Impulse response of series RC circuit.

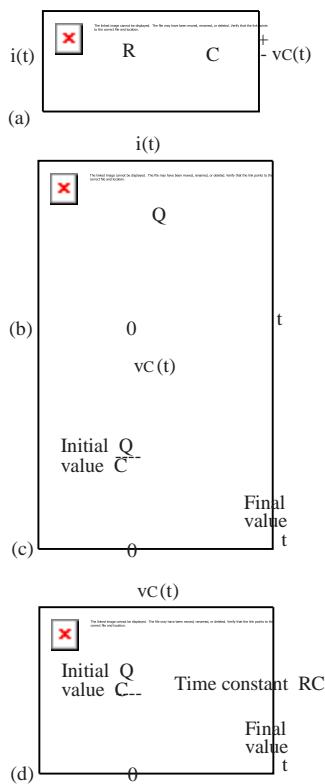


FIGURE 10.39 Intuitivemethod
of sketchingtheimpulseresponse
ofparallelRCcircuit.

a current through R. This current would deplete the charge on the capacitor, till no charge exists.)

Next, the current impulse appears at $t = 0$. The capacitor behaves like an instantaneous short to the current impulse, and so the current flows through the capacitor over the resistor. The entire impulse current flows through the capacitor at $t = 0$, depositing charge Q on it. Corresponding to the appearance of charge Q on the capacitor, from Equation 9.8, the capacitor voltage jumps instantaneously to

$$vc(0) = \frac{Q}{C}.$$

Thus, at $t = 0+$ we are left with the voltage Q/C across the capacitor. Observe that the impulse has effectively established the initial conditions on the circuit.

This completes our intuitive analysis of the initial interval. vc during this interval is sketched in Figure 10.39c.

Next, we examine the final interval ($t > 0$). Since its current is zero for $t > 0$, we can again replace the current source with an open circuit. After a long period of time, a DC situation exists, and the capacitor voltage will be zero. The zero value for vc for $t > 0$ is also sketched in Figure 10.39c.

Finally, in the transition interval, the capacitor follows its usual exponential response with time constant RC . The complete curve is sketched in Figure 10.39d.

10.6.5 CLOCK SIGNALS AND CLOCK FANOUT

In most digital systems, a clock signal is provided to different modules of the system. A clock signal is typically a square wave between 0 volts and the supply voltage. The clock signal provides a global time base that prescribes when actions happen in systems. The use of a clock attempts to solve the following problem faced by the receiver in a pair of communicating digital systems: How to determine when a signal supplied by the sender is valid. Or conversely, how to recognize when a signal might be in the midst of transitioning to a new value. For example, we might use a stable-high clock discipline in which the sender promises to provide output signals so that they remain stable during the high part of the clock waveform. In other words, signals are allowed to transition only during the low parts of a clock. Correspondingly, the receiver promises to observe incoming signals only when the clock is high. Accordingly, the receiver circuit guarantees that its own outputs are stable when the clock is high, provided, of course, valid inputs are fed to it.

As an example of the benefit of clocked circuits, consider the digital system in Figure 10.40 in which two digital circuits are coupled to each other. Both are fed by the same time base or clock. Inputs are fed to the first circuit in a way that input transitions happen only during the low parts of the clock signal. As shown in Figure 10.40, assume an input sequence 011 is fed to circuit 1. Similarly it produces outputs (for example 101) that are stable during the high

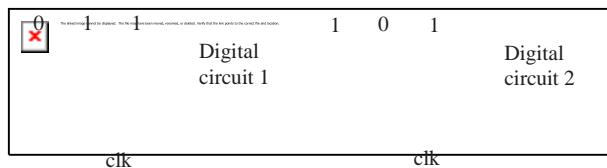


FIGURE 10.40 Clocked digital systems.

periods of the clock. Since the same clock is fed to both circuits, digital circuit 2 can observe the signal only during the periods in which the signal is valid.

Now suppose we did not use a clock. As we saw previously, RC delays cause signals to go through invalid signal levels for a finite period of time when they transition from one value to another. Without some mechanisms such as a clock and an associated discipline, there would be no way in which the second digital circuit could tell when it was receiving a valid signal. As we shall see in a later chapter, telling apart a valid signal from a transitional value is particularly difficult when signals display oscillatory or ringing behavior.

The use of a clock discipline represents an instance of time discretization. Lumping of time into invalid periods and valid periods gives us the clocked digital abstraction and significantly simplifies the orchestrating of communication between individual circuit modules. Lumping occurs because we do not care about the precise moment when a signal is sampled, provided, of course, the signal is sampled within the valid period.

Figure 10.41 shows a clocked digital system in which several modules are provided a global clock time base produced by a single clock device. One approach simply connects the clock signal generator to all the modules using one long wire. This naive approach often fails because of the RC delay associated with the long wire and the input capacitances of the driven modules. Figure 10.42 shows a circuit model for the clock distribution system. We have lumped the resistance of the wire into a single resistance R_{wire} . Although it is not shown in Figure 10.42, the resistance of the gated driving the clock will also appear in series with the resistance of the wire. The gate capacitors appear as parallel loads on the wire and therefore add together to yield a large equivalent capacitor:

$$C_{\text{eq}} = \sum_{i=1}^n C_{\text{GSi}}$$

We know from our previous examples that slow rise and fall times at the output of a circuit result in signal delay. The rise and fall times are proportional to the RC time constant. A large value for C results in long rise and fall times, thereby limiting the clock frequency. As Figure 10.43 illustrates, notice that to achieve a valid clock signal, the clock period T must be larger than the sum of the rise and fall times of the clock signal. For the clock example, let us define the rise time

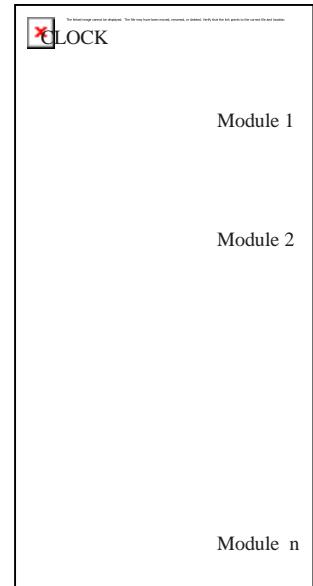
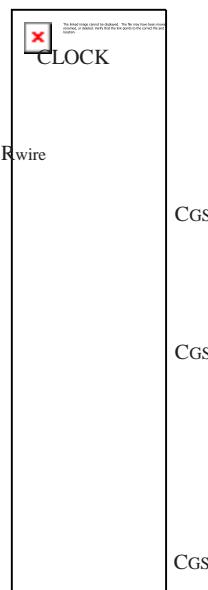


FIGURE 10.41 Clock signal for digital modules.



to the time taken for the clock signal to rise from a valid output low voltage (V_{OL}) to a valid high output voltage (V_{OH}). Let us also define the fall time as the time taken for the clock signal to fall from a valid output high voltage (V_{OH}) to a valid low output voltage (V_{OL}). As is clear from Figure 10.43, to yield a valid digital clock signal, the clock time period must satisfy the following constraint:

$$T > t_r + t_f.$$

Figure 10.44 shows a common solution to the clock distribution problem, limits the number of gate capacitors the signal has to drive by building a fanout buffer tree. The fanout degree of the circuit shown in Figure 10.44 is 3.

As a simple exercise, let us determine the greatest fanout degree that will support a clock frequency of 333 MHz. Let us suppose the clock signal is driven by an inverter as shown in Figure 10.45. Let us characterize the clock driver inverter by $R_L = 1\text{k}$, $R_{ON} = 100$, and $C_{GS} = 100\text{fF}$. Let us also assume that we desire a symmetric clock. Thus the clock period T must be greater than twice the greater of the rise and fall times at the output of the inverter. Since the load resistance R_L is much bigger than the ON resistance of the MOSFET, the

FIGURE 10.42 Clocksignal chargingthegatecapacitors.

FIGURE 10.43 Clockfrequency.

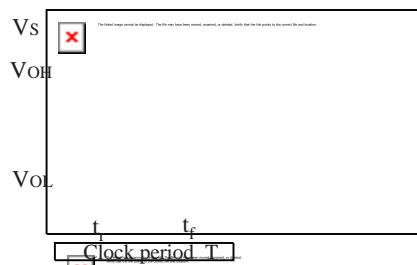
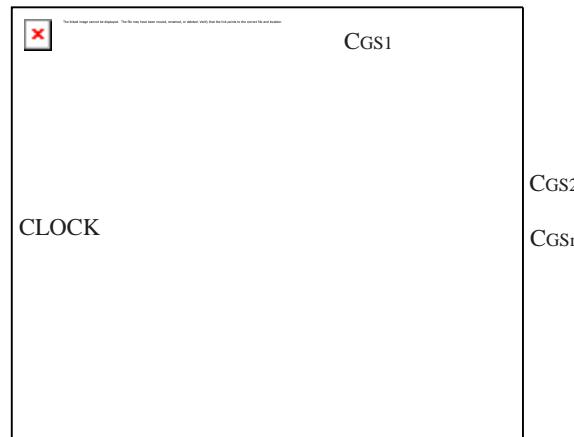


FIGURE 10.44 Fanoutclock signal.



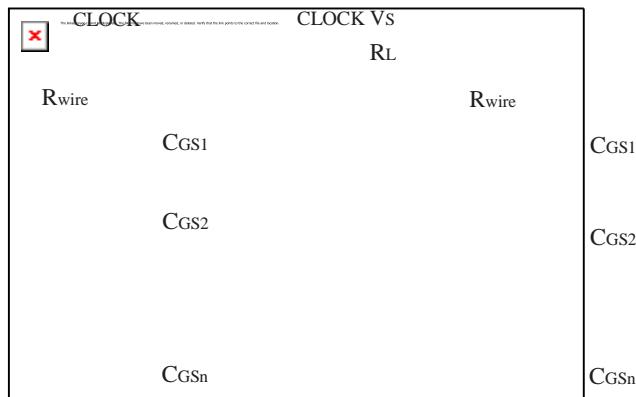


FIGURE 10.45 Clockinverter
chargingthegatecapacitors.

risetime will be greater than the falltime. Accordingly, we focus on calculating the risetime. As defined earlier, let C_{eq} represent the total capacitance driven by the clock inverter.

Let us now compute t_r . As defined earlier, t_r is the time taken for the clock signal to rise from V_{OL} to V_{OH} . The equivalent circuit for computing t_r is suggested in Figure 10.46. The circuit shows the equivalent capacitor being charged by the supply V_s through the R_{eq} and R_{wire} resistances. Let us denote $Req = R_{eq} + R_{wire}$. Then, in view of the method shown in Figure 10.46, we get

$$\frac{VC - V_s}{Req} + C_{eq} \frac{dVc}{dt} = 0.$$

Rearranging, we obtain the differential equation

$$Req C_{eq} \frac{dVc}{dt} + Vc = V_s. \quad (10.150)$$

Solving Equation 10.150, we get

$$Vc(t) = V_s + Ae^{-t/Req}. \quad (10.151)$$

We know that the voltage on the capacitor at $t=0$ is V_{OL} . Using this initial condition, we solve for A and obtain

$$Vc(t) = V_s - (V_s - V_{OL})e^{-t/Req}. \quad (10.152)$$

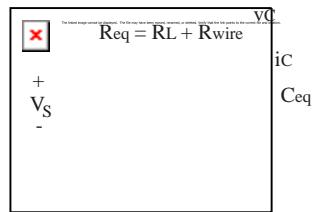


FIGURE 10.46 Equivalent circuitfordeterminingtheclock risetime.

The time taken for V_C to reach V_{OH} from its initial value of V_{OL} , namely t_r , can be obtained from

$$V_{OH} = V_S - (V_S - V_{OL})e^{-t_r/ReqC_{eq}} \quad (10.153)$$

In other words,

$$t_r = -ReqC_{eq} \ln \frac{V_S - V_{OH}}{V_S - V_{OL}} \quad (10.154)$$

Assuming $V_{OL}=1\text{V}$, $V_{OH}=4\text{V}$, and $V_S=5\text{V}$

$$t_r = -ReqC_{eq} \ln \frac{1}{4}$$

For $R_L=1\text{k}\Omega$ and $R_{wire} \approx 0$, we get

$$t_r = 1.386 \times 10^3 C_{eq}$$

To achieve a frequency greater than 333MHz , the period T must be less than $1/333\text{MHz}=3\text{ns}$. Accordingly, since $t_r < T/2 = 1.5\text{ns}$,

$$1.5 \times 10^{-9} > 1.386 \times 10^3 C_{eq}$$

In other words,

$$C_{eq} < 1.08 \text{ pF}$$

Thus the total drive capacitance must be less than 1.08 pF . Suppose the inverters used in the clock buffer tree are identical to the clock driver inverters, then if the value of each gate capacitor is 100fF , the maximum fanout degree must be less than $1080\text{fF}/100\text{fF}$. Thus the maximum fanout degree is 10.

10.6.6 RC RESPONSE TO DECAYING EXPONENTIAL *

10.6.7 SERIES RL CIRCUIT WITH SINE-WAVE INPUT

Figure 10.48 shows a series RL circuit being driven with a sine-wave voltage source suddenly applied at $t=0$:



FIGURE 10.48 RL circuit with sine-wave drive.

Let us find the voltage across the inductor, assumed to be ideal. For simplicity we assume zero initial state,

$$i_L = 0 \quad t < 0 \quad (10.168)$$

From KVL around the loop,

$$Vi = i_L R + L \frac{di_L}{dt} \quad (10.169)$$

The homogeneous solution, from Section 10.2.1, Equation 10.52, is

$$i_L = Ae^{-(R/L)t}. \quad (10.170)$$

Because the input is a sine wave, a reasonable first guess for the particular solution is

$$i_L = K \sin(\omega t). \quad (10.171)$$

From Equation 10.169 for $t > 0$,

$$V \sin(\omega t) = KR \sin(\omega t) + L\omega K \cos(\omega t). \quad (10.172)$$

This can't be solved for K unless L is zero, so our first guess is not quite right. We need another degree of freedom in the solution, so try

$$i_L = K_1 \sin(\omega t) + K_2 \cos(\omega t). \quad (10.173)$$

Now Equation 10.169 becomes

$$V \sin(\omega t) = K_1 R \sin(\omega t) + K_2 R \cos(\omega t) + K_1 \omega \cos(\omega t) - K_2 \omega \sin(\omega t) \quad (10.174)$$

Equating sine terms, and equating cosine terms, we find

$$V = K_1 R - K_2 L \omega \quad (10.175)$$

$$0 = K_1 L \omega + K_2 R \quad (10.176)$$

which yields, via Cramer's Rule (see Appendix D),

$$K_1 = V \frac{R}{R^2 + \omega^2 L^2} \quad (10.177)$$

$$K_2 = V \frac{-\omega L}{R^2 + \omega^2 L^2}. \quad (10.178)$$

The complete solution is of the form

$$i_L = A e^{-(R/L)t} + V \frac{R}{R^2 + \omega^2 L^2} \sin(\omega t) - V \frac{\omega L}{R^2 + \omega^2 L^2} \cos(\omega t), \quad t \geq 0. \quad (10.179)$$

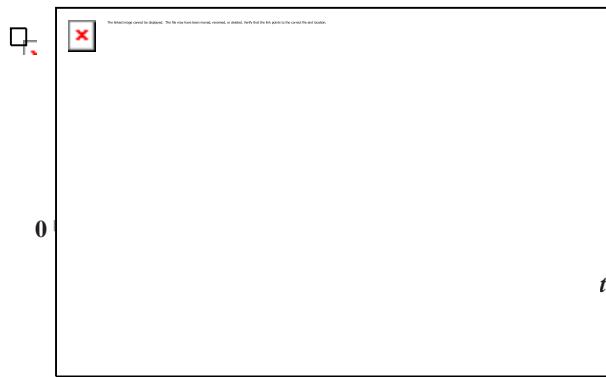
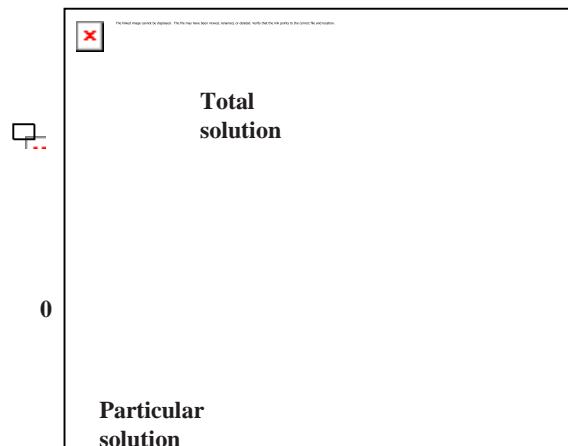


FIGURE 10.49 Waveforms for
RL circuit with sine wave drive.



The value of A can be found by applying the initial condition, Equation 10.168, to Equation 10.179, with $t = 0$, whence

$$A = \frac{V_0 L}{R^2 + \omega_0^2 L^2}. \quad (10.180)$$

The solution is shown in Figure 10.49.

Equation 10.179 is fairly easy to interpret when it is large enough that the exponential term has died away. If the drive frequency is very low, such that

$$\frac{R}{\omega L}, \quad (10.181)$$

then the current reduces to

$$i_L = \frac{V_R \sin(\omega t)}{\omega L} \quad (10.182)$$

That is, at low frequencies, the current is determined only by the resistor, and the inductor behaves like a short circuit.

At high frequencies, that is, for

$$\omega L \gg \frac{R}{L} \quad (10.183)$$

Equation 10.179 reduces to

$$i_L = \frac{-V \cos(\omega t)}{\omega L} \quad (10.184)$$

In this case, the current is determined almost solely by the inductor. Note that the current is still sinusoidal, but now is 90 degrees out of phase with the applied voltage. Also, the magnitude of the current becomes smaller and smaller as the frequency of the applied sine wave increases.

It is a little disappointing that such a simple circuit can lead to this level of algebra. But fortunately there is a simpler approach that can be used for linear circuits. This approach, discussed in Chapter 13, reduces all the differential equations to algebraic expressions.

10.7 DIGITAL MEMORY

This chapter demonstrated previously that the memory aspect of capacitors and inductors formalized using the notion of state variables provided many uses in the analog domain. The same memory property can also be utilized in the digital domain to implement digital memory using the analogous concept of digital state. Digital memory is not only an important application of capacitors, but it is of fundamental importance in its own right.

10.7.1 THE CONCEPT OF DIGITAL STATE

A common example of the use of memory involves the digital calculator. Suppose we wish to compute the value of the expression $(a \times b) + (c \times d)$. We might first multiply a and b and store the result $(a \times b)$ in memory. We might then multiply c and d , and add the resulting value $(c \times d)$ to $(a \times b)$ by recalling the latter value from memory. Observe that the calculator contained a key to explicitly store a given value into the memory. Observe further that once a value was stored in memory, it could be read from memory any number of times, without affecting the value in memory. In fact, it remained valid

until another value was explicitly stored in memory or it was erased. Erasure corresponds to replacing the existing value with a zero value.

Memory has many uses. In this example, memory is used as a scratchpad area to store partial results. Memory is also useful to store values input to a system from the outside world. Memory enables short-lived external inputs to be available to system circuitry for a longer period of time.

Memory is also useful in enabling better resource utilization. Suppose we wish to add three numbers A_0 through A_2 . The addition can be accomplished using two adder circuits as follows: The first and second numbers are fed to the first adder. The result of the first adder and the third value are fed to the second adder. The sum S is obtained as the output of the second adder.

Alternatively, we can utilize memory to accomplish the addition of three numbers with a single adder as follows: Feed the first and second numbers to the adder. Store the partial result in memory. Then feed the partial result from memory and the third number to the same adder. The adder output is the desired result.

The same concept can be generalized to add a long sequence of numbers. At any given instant, the memory stores the partial result corresponding to all the numbers that occurred till that instant. For our addition example, notice that future results depend only on the values stored in memory and future inputs. Future results do not depend on the exact how the memory was time sequenced, just its final state. This observation stems from the concept of a “state variable” that we saw earlier. The value stored in memory is simply a digital state variable in a manner analogous to an analog state variable value stored on a capacitor.

The next section discusses how capacitors can be used to build digital memory.

10.7.2 AN ABSTRACT DIGITAL MEMORY ELEMENT

Before we discuss how to implement memory, let us first define an abstract memory element and understand how it can be used in a small system. Figure 10.50 shows an abstract memory element that can store one bit of data. It has an input d_{IN} , an output d_{OUT} , and a control input called $store$. As suggested by the waveforms in Figure 10.50, the input d_{IN} is copied into memory when the $store$ signal is high. The value stored in the memory is available to

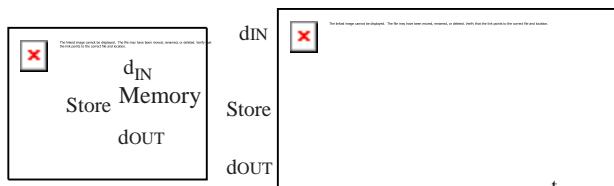


FIGURE 10.50 An abstract one-bit memory element.

be read as the output $DOUT$. If no new value is written into the memory, the last written value is stored indefinitely. If the memory is read while it is being written (that is, when the store signal is high), then the output simply reflects the value at the input.

example 10.4 motion detector circuit revisited

Let us use the memory element that we have just defined in a simple digital design. Recall the motion detector circuit from Chapter 5. The motion detector circuit was required to produce a signal L to turn on a set of lights when the signal M from a motion sensor was high, provided it was not daytime. We assumed that a light sensor produced a signal D that was high when it was day. We had written the following logic expression for L :

$$\overline{L} = \overline{MD}.$$

A problem with this design is that the lights that were returned on by the assertion of M would go off the instant M was de-asserted.¹³ Let us consider a more useful design in which we require the lights to stay one even after the motion signal M goes away. To make this happen, we need some form of memory to remember the occurrence of M , even after the M signal goes away. The desired circuit uses a memory element and is shown in Figure 10.51. In this circuit, the signal M is connected to the store input of the memory, and the signal D is connected to the dIN input of the memory. As depicted in the signal waveforms in Figure 10.51, the memory output remains high if motion is detected even when D is false.¹⁴

10.7.3 DESIGN OF THE DIGITAL MEMORY ELEMENT

How do we implement a memory element? The memory element must be designed so that it stores indefinitely any value that has been written into it. Recall that a capacitor has the same property. Provided its discharge path has a high time constant, a capacitor can store a charge for a long period of time. Furthermore, we can use a switch to enable charging the capacitor from a given input.

13. To ‘assert’ is to set the value to logical 1, while to ‘de-assert’ is to set the value to logical 0.

14. Our circuit shown in Figure 10.51 has one other problem. How do the lights turn off? It should be apparent from the circuit that L will go back to 0 when motion is detected during the daytime. However, relying on the appearance of signal M during the daytime to turn off the lights is unappealing. One solution is to modify your memory abstraction to include a reset signal as follows: The value in memory is set to 0 when the reset input is high. (Our memory abstraction can include the additional property that the reset signal overrides the store signal if both are on at the same time.) Our motion detector circuit output L cannot be turned off by asserting the reset signal of the memory. The reset terminal of memory can be connected to the signal D so that the memory contents and therefore the lights go off whenever it is day.

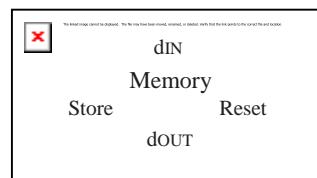


FIGURE 10.51 A motion detector circuit using memory.

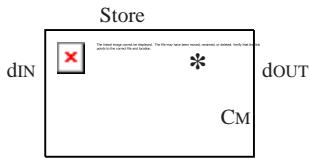
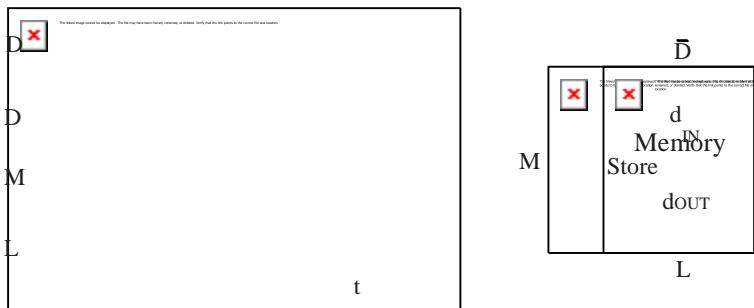


FIGURE 10.52 Circuit implementation of a memory element.

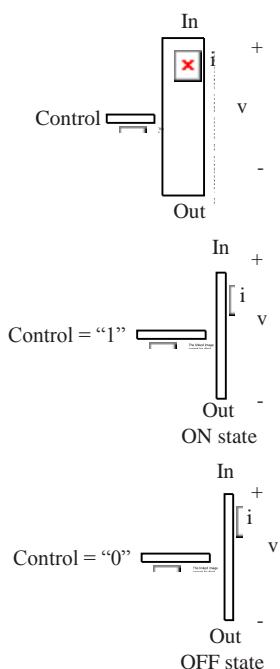


FIGURE 10.53 Three-terminal switch model.

Based on this intuition, consider the simple memory element circuit comprising a capacitor and an ideal switch shown in Figure 10.52. The switch is controlled by the store input and has the circuit model shown in Figure 10.53. When connected as shown in Figure 10.52, assume that a logical high value on the store input turns the switch into its ON state, while a logical low value on the store input turns the switch into its OFF state.

As discussed in Section 6.1, a circuit containing a switch can be analyzed by considering two linear subcircuits: one for the switch in its ON state (see Figure 10.54) and one for the switch in its OFF state (see Figure 10.56). A high on the store terminal turns the switch on, and results in the circuit illustrated in Figure 10.54. The capacitor then charges up (or discharges) to the value of the input voltage at the *In* terminal when the switch is turned on. Remember, the switch is symmetric about its input and output terminals. Thus, for example, if the *DIN* terminal had a high voltage corresponding to a logical 1 (produced, for example, by a voltage source, as illustrated in Figure 10.55), the capacitor will offer a high voltage at the node marked with an asterisk when the store signal is asserted. In this situation, the ideal external voltage source charges up the capacitor instantly through the ideal switch (assuming the capacitor had a low voltage initially). Alternatively, if the *DIN* terminal had a low voltage corresponding to a logical 0, the capacitor will offer a low voltage at the node marked with an asterisk when the store signal is asserted. In this latter situation, the capacitor discharges instantly through the ideal switch and the ideal external voltage source (assuming that the capacitor had a high voltage initially) and attains the same voltage as the voltage source.

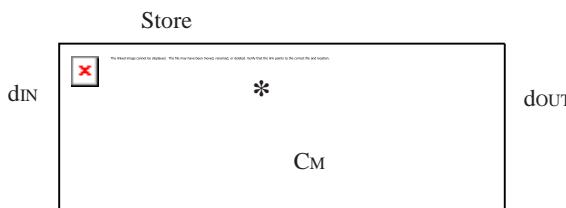
Conversely, when the store signal goes low, the switch turns off (see Figure 10.56). Consequently, the *DOUT* terminal of the capacitor begins to float and the charge previously deposited on the capacitor is held in place. Thus, for example, if a high voltage had been previously stored on the capacitor, a high voltage will appear at the capacitor terminal *DOUT* even after the store signal goes low. In the ideal case, if the resistance between the *DOUT* terminal and ground is infinite, the capacitor will hold the charge forever.

The waveforms shown in Figure 10.50 will apply to the memory element circuit shown in Figure 10.52 under the following idealized assumptions: When the store signal is high, the RC time constant associated with the capacitor circuit is negligible, and when the store signal is low, the RC time constant associated with the capacitor circuit is infinite. The RC time constant of the circuit when the store signal is high is given by the product of C_M and the sum of the on resistances of the switch and the driving element. Similarly, the RC time constant of the circuit when the store signal is low is given by the product of C_M and the resistance seen by the capacitor.¹⁵

There is, however, one remaining problem with our memory element circuit. Recall that the static discipline required that our digital circuit elements such as gates be restoring. In other words, in order to obtain positive noise margins, the voltage threshold requirements on the outputs of gates was more stringent than those on the inputs. For example, the static discipline required that a V_{IH} input to a gate be restored to V_{OH} at the output, where $V_{OH} > V_{IH}$ for a positive noise margin. In order to operate digital memory elements without digital gates, we require that our digital memory elements satisfy the same set of voltage thresholds.

Unfortunately, our digital memory circuit as described in Figure 10.52 is non-restoring. In other words, if a voltage V_{IH} corresponding to a valid 1 was applied to its input, the output of the memory element would not be restored to V_{OH} , rather it would beat V_{IH} as well.

As suggested in Figure 10.57, a simple modification of our memory circuit can make it restoring. This design adds a pair of series-connected inverters (or a buffer) to the output of our previous memory element circuit. The buffer will restore a V_{IH} voltage on the capacitor terminal to a V_{OH} voltage at the DOUT output. Interestingly, when a buffer is included in the memory element circuit, we do not need to implement a special capacitor to hold charge. Rather, the gate capacitance of the buffer CGS forms the memory capacitance CM.



15. We can also modify the memory element circuit to include a reset signal as follows: In this circuit, we use a second switch to discharge the capacitor to ground when the reset signal is high. Additionally, to make this circuit work, we must use non-ideal switches that are designed such that the ON resistance of the reset switch is much lower than that of the store switch. By doing so, we can ensure that a reset will override the store when the store and reset are on at the same time.

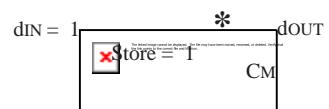


FIGURE 10.54 Charging up the memory capacitor, when the store signal is high.

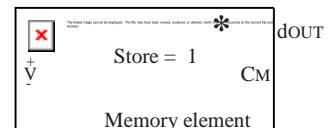


FIGURE 10.55 The memory element circuit model including the driving external source, when the store signal is high.

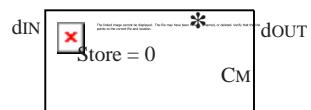


FIGURE 10.56 Charge storage in the memory capacitor, when the store signal is low.

FIGURE 10.57 Circuit implementation of a signal restoring memory element.



FIGURE 10.58 Memory capacitor discharge due to load resistances for the unbuffered memory element.

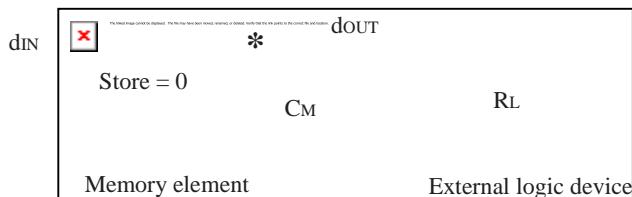
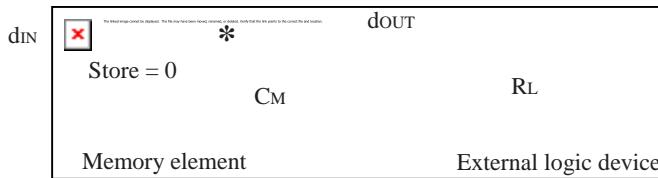


FIGURE 10.59 Memory capacitor's charge is protected in the buffered memory element.



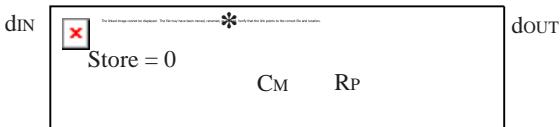
By isolating the capacitor from the circuit that reads the stored value, the buffer offers added advantages. As shown in Figure 10.58, devices that read the value stored on the capacitor might have relatively low resistances associated with them, thereby discharging the capacitor in our original unbuffered memory circuit. In contrast, the buffered design of the memory element circuit shown in Figure 10.59 protects the capacitor's charge from the external circuit. By careful design of the memory element, the input resistance of the buffer can be made to be very large, thereby ensuring a large discharge time constant.

In practice, capacitors will leak their charge over time due to parasitic resistances. Let us suppose the capacitor gradually discharges through a parasitic resistance R_P (see Figure 10.60). In this situation, for how long will the value stored in the capacitor remain valid after the store signal is de-asserted?

There are two cases to consider. First, if a 0 is stored on the capacitor, then the 0 value will be held indefinitely even with a low parasitic resistance. Notice that as the capacitor discharges to ground, the 0 stored on it will remain a 0.

The second case is more interesting. In this case, a 1 is written on the capacitor. Assume that the voltage corresponding to a 1 is V_S . The value stored on the capacitor will be read as a valid 1 by the buffer until it reaches the V_{IH} voltage threshold. Thus the period over which the memory element will store a valid 1 is the interval over which the voltage drops from V_S to V_{IH} . We can compute this duration from capacitor discharge dynamics (for example,

FIGURE 10.60 Charge leakage from the memory capacitor for the buffered memory element.



see Equation 10.26). When a capacitor C_M charged to an initial voltage V_s discharges through a resistor R_P , its voltage v_C as a function of time is given by the following equation:

$$v_C = V_s e^{-t/R_P C_M}$$

The time taken for v_C to drop from V_s to V_{IH} is given by

$$t_{V_s \rightarrow V_{IH}} = -R_P C_M \ln \frac{V_{IH}}{V_s}$$

As an example, suppose that $C_M = 1 \text{ pF}$, $R_P = 10^9 \Omega$, $V_s = 5 \text{ V}$, and

$V_{IH} = 4 \text{ V}$. Then $t_{V_s \rightarrow V_{IH}} = 0.22 \text{ milliseconds}$.

10.7.4 A STATIC MEMORY ELEMENT

The one-bit memory element that we have discussed thus far is called a dynamic one-bit memory element or a dynamic D-latch. It is dynamic in the sense that it stores a value written into it only for a finite amount of time (due to nonzero parasitic resistances in practical implementations). The static one-bit memory element or a static D-latch is another type of memory element that has the same logic properties as the dynamic D-latch, but can store a value written into it indefinitely.

Figure 10.61 shows one possible circuit for a static memory element. In this circuit, a non-ideal switch with a very high ON resistance is connected between the power supply and the storage node of the memory element. When the output of the memory element is a logical 1, this switch is turned on and introduces a small stream of charge into the storage node to offset any leakage. Because it trickles charges into the node, this switch is called a trickle switch. The ON resistance of the trickle switch is made very large compared to the ON resistance of the store switch, so that the trickle input can be overridden easily by the input dIN . A detailed circuit design of the static latch is beyond the scope of this book. The interested reader is referred to ‘Principles of CMOS VLSI Design,’ by Weste and Eshraghian.

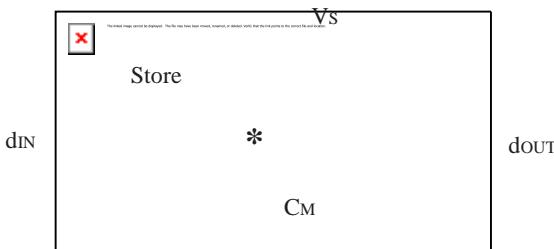


FIGURE 10.61 Circuit implementation of a static memory element using a trickle switch.

10.8 SUMMARY

The first-order differential equations that result from applying KVL and KCL to networks containing sources, resistors, and one energy-storage element can be derived using the node method or the other approaches described in Chapter 3. These differential equations can be solved by finding the homogeneous solution and the particular solution.

The response of RC circuits resembles rising or decaying exponentials with the time constant RC . As an example, for a series RC circuit driven by a voltage given by step of amplitude V_1 at $t = 0$, the capacitor voltage for $t > 0$ is

$$v_C(t) = V_1 + (V_0 - V_1)e^{-t/RC}$$

where V_0 is the initial voltage on the capacitor.

In general, the response of a first-order circuit (RC or RL) will be of the form

$$v_C = \text{final value} + (\text{initial value} - \text{final value})e^{-t/\text{time constant}}$$

where the time constant is RC for a resistor-capacitor circuit and L/R for an resistor-inductor circuit. This form of the response in RC and RL circuits is shared by other branch variables such as the capacitor or inductor current and resistor voltage.

Capacitors behave like open circuits when a circuit containing capacitors is driven by a DC voltage source. Conversely, a capacitor behaves like an instantaneously short circuit when inputs make an abrupt transition (for example, a step). (If the capacitor voltage were nonzero, then the capacitor would behave like a voltage source for abrupt transitions.)

Inductors behave like short circuits when a circuit containing inductors is driven by a DC current source. Conversely, an inductor behaves like an instantaneous open circuit for inputs that make an abrupt transition (for example, a step). (If the inductor current were nonzero, then it would behave like a current source for abrupt transitions.)

The zero-input response is the response of the system to the initial stored energy, assuming no drive.

The zero-state response is the response to an applied drive signal, for no initial stored energy.

When the input signal is a short pulse (short compared to the time constant of the circuit), the response is proportional to the area of the applied pulse rather than to its height or shape.

It is often convenient to break down a problem involving energy-storage elements into two parts. First, calculate the zero-input response, the response

of the system to the initial stored energy, assuming no drive. Then calculate the zero-state response, the response to the applied drive signal, for no initial stored energy.

If we restrict integral operations to t greater than zero, the zero-state response of the integral of some input signal is the integral of the zero-state response to that signal. The same is true for differentiation: The response to a signal derived by differentiating an input can be obtained by differentiating the output.

The rise time for an output node is defined as the delay in rising from its lowest value to a valid high (V_{OH}) at that output.

The fall time for an output node is defined as the delay in falling from its highest value to a valid low (V_{OL}) at the same output.

The delay $t_{pd,1 \rightarrow 0}$ for an input-output terminal pair of a gate is the time interval between a 1 to a 0 transition at the input to the moment that the output reaches a corresponding valid output voltage level (V_{OH} or V_{OL}).

The delay $t_{pd,0 \rightarrow 1}$ for an input-output terminal pair of a gate is the time interval between a 0 to a 1 transition at the input to the moment that the output reaches a corresponding valid output voltage level (V_{OL} or V_{OH}).

exercise 10.1 Using superposition, determine the current $i_1(t)$ for the network shown in Figure 10.62. The network is at rest for $t < 0$.

exercise 10.2 Find and sketch the zero state response for $t > 0$ in Figure 10.63. $i_s(t) = 10\text{ mA}$ step at $t = 0$.

exercise 10.3 In the circuit in Figure 10.64, $i(t) = 100\mu\text{A}$, $0 < t < 1\text{ s}$, zero otherwise. At time $t = 2\text{ s}$, the voltage $v_c = 5\text{ V}$. What is v_c at time $t = -1\text{ s}$?

exercise 10.4 In the circuit in Figure 10.65, the switch is closed at $t = 0$ and opened at $t = 1\text{ second}$. Sketch $v_c(t)$ for all times.

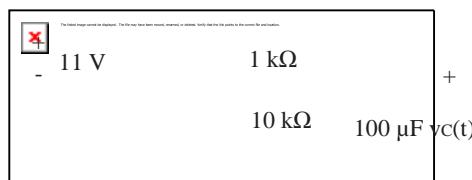


FIGURE 10.65

exercise 10.5 Find and sketch the zero-input response for $t > 0$ in each network in Figure 10.66 for the given initial conditions.

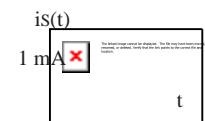
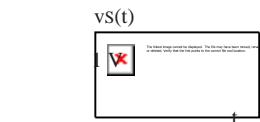
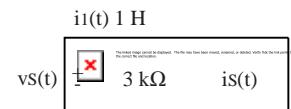


FIGURE 10.62

EXERCISES

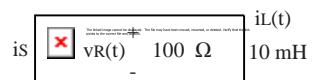


FIGURE 10.63



FIGURE 10.64

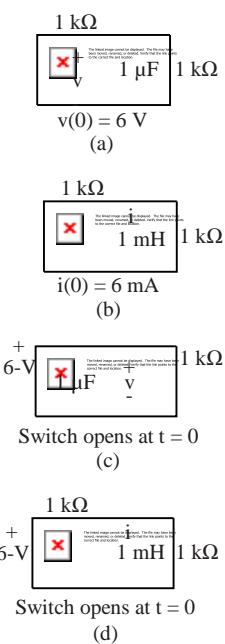


FIGURE 10.66

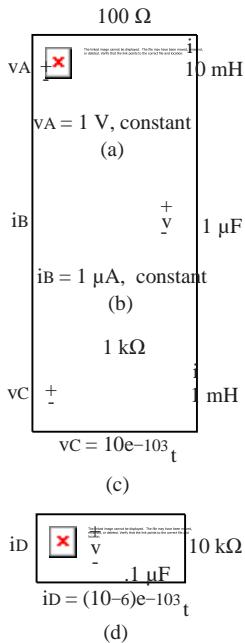


FIGURE 10.67

exercise 10.6 Find and sketch the response for $t > 0$ in each network in Figure 10.67. Assume that the input is as shown for $t > 0$, and assume initial zero state (in other words, show the zero-state response).

exercise 10.7 For the current source shown in Figure 10.68, assume it consists of a single rectangular current pulse of amplitude I_0 amps and duration τ seconds.

a) Find the zero-state response to i .

b) Sketch the zero-state response for the cases:

i) $t \rightarrow RC$

ii) $t=RC$

iii) $t \rightarrow RC$

c) Show that for $t > 0$ RC , (the case of a short pulse), the response for $t > t_0$ depends only on the area of the pulse ($I_0 t_0$) and not on t_0 or τ separately.



FIGURE 10.68

exercise 10.8 Identify the state variable in each network in Figure 10.69. Write the corresponding state equation and find the time constants.

exercise 10.9 In the circuit in Figure 10.70, $v(t) = 5 \text{ mV}$ for $0 < t < 1 \text{ s}$, and zero otherwise. At time $t = 4 \text{ s}$, $i(t) = 7 \text{ A}$. What is $i(t)$ at time $t = -1 \text{ s}$?

exercise 10.10 Identify appropriate state variables for the network in Figure 10.71 and write the state equations.

exercise 10.11 In Figure 10.72, $R_1 = 1 \text{ k}\Omega$, $R_2 = 2 \text{ k}\Omega$, and $C = 10 \mu\text{F}$.

The driving voltage $v_S = 0$ for $t < 0$. Assume v is a 3° volt step at $t = 0$. Make a sketch of $v(t)$ for $t > 0$. Be sure to label the dimensions of the voltage and time axes and identify characteristic waveform shapes with suitable expressions.

exercise 10.12 Identify state variables and write appropriate state equations for the circuit in Figure 10.73.

exercise 10.13 Referring to Figure 10.74, before the switch is closed, the capacitor is charged to a voltage $v_S = 2 \text{ V}$. The switch is closed at $t = 0$. Find an expression for $v(t)$ for $t > 0$. Sketch $v(t)$.

exercise 10.14 Find the time constant of the circuit shown in Figure 10.75.

exercise 10.15 A two-input RCC circuit is shown in Figure 10.76. (Parts a, b, and c are independent questions.)

a) You should realize that the “bridge” of capacitors can be replaced by a single capacitor in this problem. What is the value of the single equivalent capacitor?

b) Consider operation with $i(t) = 0$ and $v(t) = 0$ for $t \geq 0$. The voltage $v_o(t)$ is known to be 1 volt at $t = 0$. Determine $v_o(t)$ for all $t > 0$.

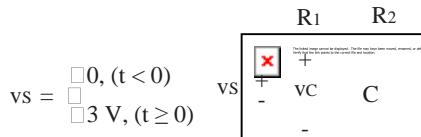


FIGURE 10.72

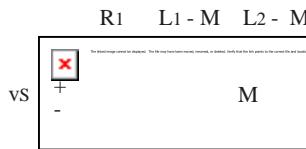


FIGURE 10.73

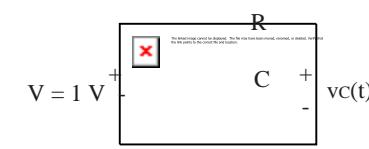


FIGURE 10.74

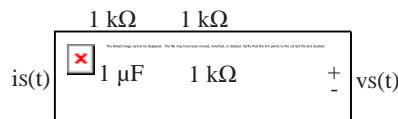


FIGURE 10.75

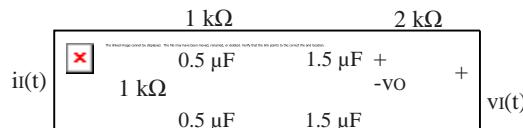


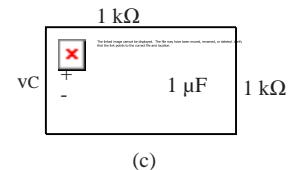
FIGURE 10.76



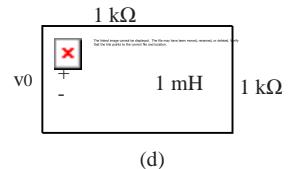
(a)



(b)



(c)



(d)

FIGURE 10.69



FIGURE 10.70

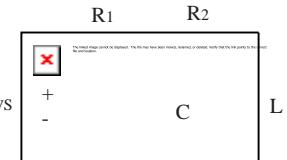


FIGURE 10.71

c) A different constraint is that sources $i_1(t)$ and $v_1(t)$ are zero for $t < 0$ and that $v_0(0) = 0$. Sources $i_1(t)$ and $v_1(t)$ undergo step transitions of +1 mA and +1 volt, respectively, at time $t=0$. Determine $v_0(t)$ for all time.

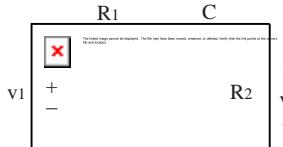


FIGURE 10.77

exercise 10.16 In the circuit in Figure 10.77, $R_1 = 1 \text{ k}\Omega$, $R_2 = 2 \text{ k}\Omega$, and $C = 3 \mu\text{F}$. Assume initial rest conditions (zero initial state), and assume that $v_{00} = 1$ volt. Find $v_0(t)$ for $t > 0$. Sketch and label.

exercise 10.17 Consider the circuit shown in Figure 10.78. Sketch and label $v_0(t)$ for $i_1(t)$ a step as shown in Figure 10.79. Assume $v_{00} = 0$ for $t < 0$.

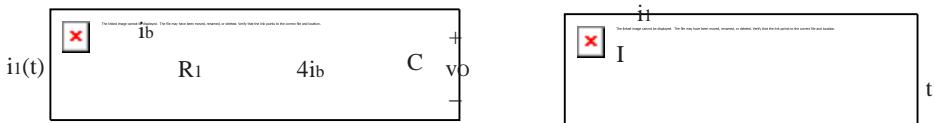


FIGURE 10.78



FIGURE 10.79

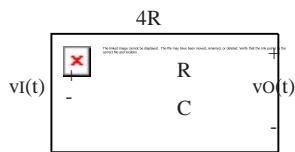


FIGURE 10.80

exercise 10.18 For the circuit shown in Figure 10.80, find the characteristic equation and the zero input response assuming that the capacitor was initially charged to 1 volt. Label your graph.

exercise 10.19 The excitation function for all four of the circuits shown in Figure 10.81 is

$$v_s(t) = \begin{cases} 0, & t < 0 \\ 10V, & t \geq 0. \end{cases}$$

For each of the circuits, select the time function on the right that corresponds in magnitude and shape to the output, $v_0(t)$. Assume that all capacitors and inductors have zero initial states, (the appropriate state variable is zero for less than zero). If no matching response exists, say so and explain briefly. All responses are made up of “straightlines” and “exponentials.” You may choose a time function more than once. (Note that part (d) shows an op-amp circuit. Op-amps will be covered in later chapters.)

exercise 10.20 An RC network is shown in Figure 10.82. The voltage v_{00} and the current i_{00} are constant for all time. Prior to $t=0$, the circuit is in equilibrium with the switch closed. At time $t=0$, the switch is opened, and it is then closed sometime later. The waveform in Figure 10.83 is observed for $v_{00}(t)$

What are the values of τ_1 , τ_2 , and the final value V_1 ? (Note: The figure may not be to scale.)

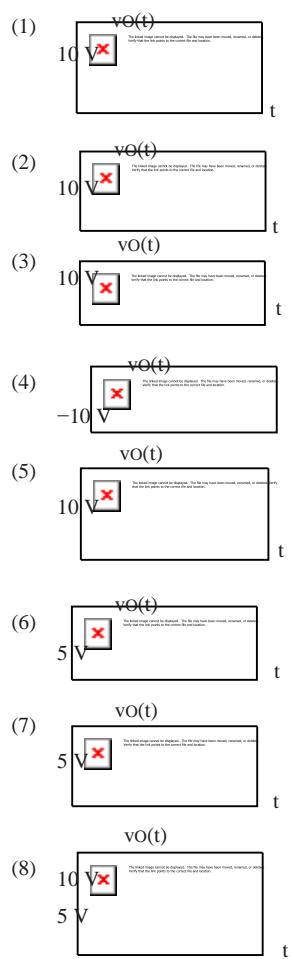
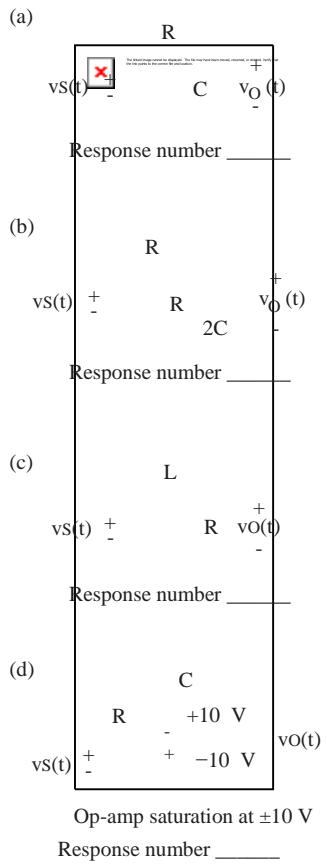


FIGURE 10.81

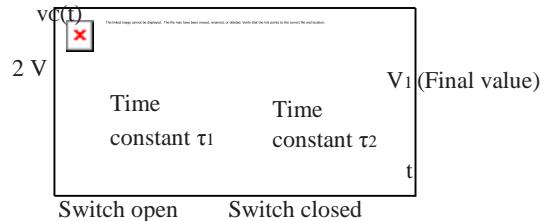
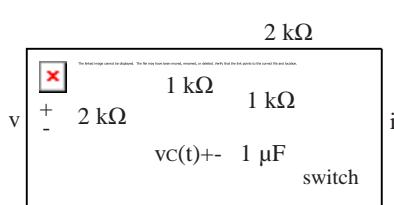


FIGURE 10.82

FIGURE 10.83

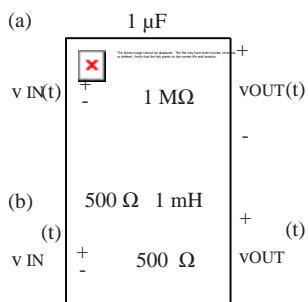


FIGURE 10.84

exercise 10.21 In the two following cases in Figure 10.84 the input $v_{IN}(t) = 10u_{-1}(t) + 10 - V$ step 16 starting at time $t = 0$. Give for each case:

- The time constant of the circuit.
- An analytic expression for the signal $v_{OUT}(t)$ as a function of time.
- A labeled sketch of the output signal $v_{OUT}(t)$ as a function of time. Be sure to label the time and voltage scales.

exercise 10.22 In each of the following cases, find by inspection and give

- i) an expression for the time constant τ ,
- ii) a sketch of the signal versus time,
- iii) an analytic expression for the signal in terms of τ and any other necessary parameters.

- a) Referring to Figure 10.85, find $v(t)$ for $t > 0$ given $i(t=0) = I_0$.
- b) Referring to Figure 10.86, find $i_2(t)$ given $i_1(t=0) = I_0/2$.
- c) Referring to Figure 10.87, find $v(t)$ for $t > 0$ given that the switch is moved from 1 to 2 at $t = 0$.

FIGURE 10.85

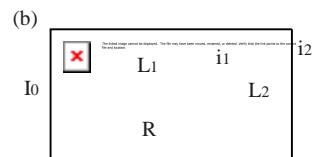


FIGURE 10.86

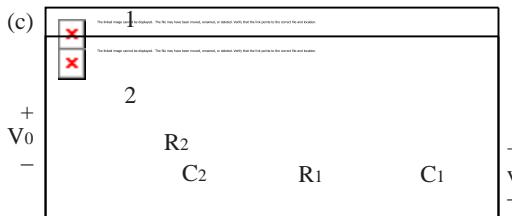


FIGURE 10.87

exercise 10.23 For the circuit in Figure 10.88, with no charge on the capacitor at $t = 0$, given that if $v_C = At u_{-1}(t)$ then $v_C = [A(t-\tau) + A\tau e^{-\tau/t}] u_{-1}(t)$. Note that $u_{-1}(t)$ represents a unit step at $t = 0$.

16. Recall that the notation $u_0(t)$ represents an impulse at time t . Then the notation $u_n(t)$ represents the function that results from differentiating the impulse times, and the notation $u_{-n}(t)$ represents the function that results from integrating the impulse times. Thus $u_{-1}(t)$ represents the unit step at time t , $u_{-2}(t)$ the ramp, and $u_{-1}(t)$ the doublet at time t . The unit step $u_{-1}(t)$ is also commonly represented as $\delta(t)$, and the unit impulse $u_0(t)$ as $\delta'(t)$.



FIGURE 10.88

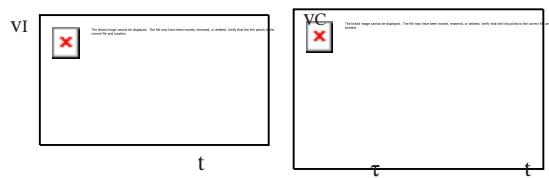


FIGURE 10.89

Find the following:

- $v_c(t)$ when the input is the same as previously given but $v_c(t=0)=V_0$.
- $v_c(t)$ when $v_c(0) = 0$ and $v_i(t) = B u_{-1}(t)$. Note that $u_{-1}(t)$ represents a unit step att=0.
- $v_c(t)$ for $t \geq T$ when $v_c(0)=0$ and

$$v_i(t) = \begin{cases} 0 & t \leq 0 \\ At & 0 \leq t \leq T \\ AT & T \leq t. \end{cases}$$

exercise 10.24 A digital memory element is implemented as illustrated in Figure 10.90. Sketch the waveform at the output of the memory element for the input signals shown in Figure 10.91. Assume that the switch is ideal and that the memory element has a 0 stored initially.

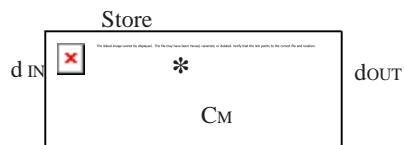


FIGURE 10.90

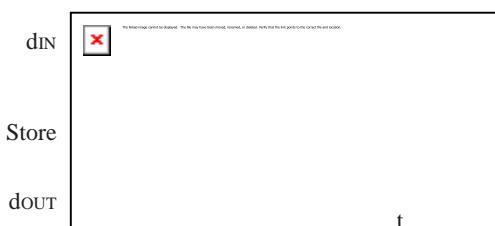
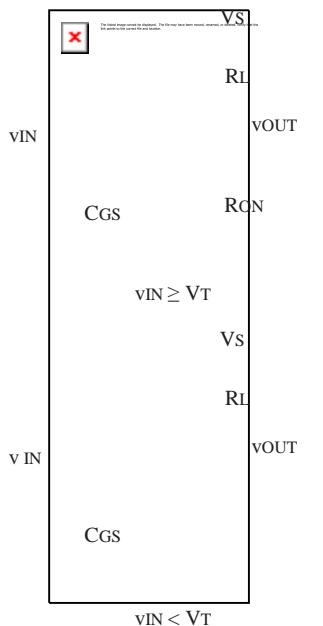


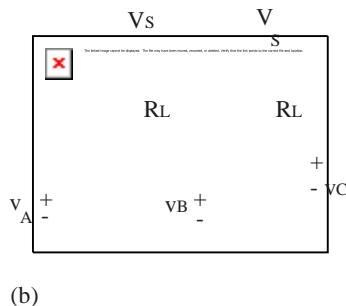
FIGURE 10.91

PROBLEMS

problem 10.1 Figure 10.92a illustrates an inverter INV1 driving another inverter INV2. The corresponding equivalent circuit for the inverter pair is illustrated in Figure 10.92b. A, B, and C represent logical values, and v_A , v_B , and v_C represent voltage levels. The equivalent circuit model for an inverter based on the SRC model of the MOSFET is depicted in Figure 10.93.



(a)



(b)

FIGURE 10.92

- Write expressions for the rise and fall times of INV1 for the circuit configuration shown in Figure 10.92. Assume that the inverters satisfy the static discipline with voltage thresholds $V_{IL} = V_{OL} = V_L$ and $V_{IH} = V_{OH} = V_H$. (Hint: The rise time of INV1 is the time v_B requires to transition from the lowest voltage reached by v_B (given by the voltage divider action of R_L and R_{ON}) to V_H for a v_A to 0 -step transition at the input v_A . Similarly, the fall time of INV1 is the time v_B requires to transition from the highest voltage reached by v_B (that is, V_S) to V_L for a v_A to V_S -step transition at the input v_A .)
- What is the propagation delay t_{pd} of INV1 in the circuit configurations shown in Figure 10.92, for $R_{ON} = 1\text{k}\Omega$, $R_L = 10R_{ON}$, $C_{GS} = 1\text{nF}$, $V_S = 5\text{V}$, $V_L = 1\text{V}$, and $V_H = 3\text{V}$?

FIGURE 10.93

problem 10.2 The inverter-pair comprising INV1 and INV2 studied in Problem 10.1 (see Figure 10.92) drives another inverter INV3 as illustrated in Figure 10.94a. Logically, these series-connected pairs of inverters INV1 and INV2 function as a buffer, as depicted in Figure 10.94b. The equivalent circuit of the buffer circuit driving INV3 is illustrated in Figure 10.94c. For this problem, use the equivalent circuit model for an inverter based on the SRC model of the MOSFET as depicted in Figure 10.93. Assume further that each of the inverters satisfies the static discipline with voltage thresholds $V_{IL} = V_{OL} = V_L$ and $V_{IH} = V_{OH} = V_H$. Assume further that the MOSFET threshold voltage is V_T . (Note that to satisfy the static discipline, the following is true: $V_L < V_T < V_H$.)

- Referring to Figure 10.94c, assume that the input to the buffer v_A undergoes a step transition from 0V to V_S at time $t = 0$. Write an expression for $v_B(t)$ for $t \geq 0$

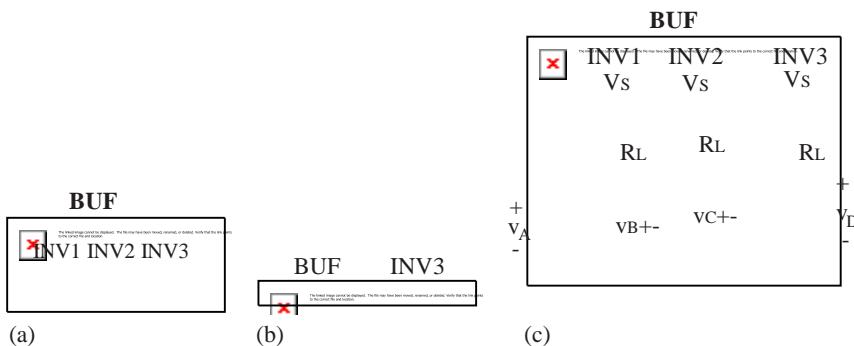


FIGURE 10.94

for the step transition in v_A . (Hint: See the fall time calculation in Problem 10.1a.)

Sketch the form of v_B for $t \geq 0$.

- Referring to Figure 10.94c, assume that the input to the buffer v_A undergoes a step transition from 0 V to V_s at $t = 0$. Write an expression for $v_C(t)$ for $t \geq 0$ for the step transition in v_A . (Hint: Refer to the sketch of v_f drawn in part (a).) The MOSFET in INV2 stays on for $v_B \geq V_T$, and turns off when $v_B < V_T$.) Sketch the form of $v_f(t)$ for $t \geq 0$.
- Write an expression for the rise time of the buffer for the circuit configuration shown in Figure 10.94c. (Hint: Refer to the sketch of v_C from part (b).) The rise time of the buffer is the time v_C requires to transition from the lowest voltage reached by v_C to V_H from the time the input v_A makes a step transition from 0 V to V_s . Note that the rise time of the buffer includes the internal buffer fall delay, which is the time v_B takes to transition from V_s to V_T , and the additional time v_C takes to transition from its lowest voltage to V_H .)
- Referring to Figure 10.94c, assume that the input to the buffer v_A undergoes a step transition from V_s to 0 V at $t = 0$. Write an expression for $v_B(t)$ for $t \geq 0$ for the step transition in v_A . Sketch the form of $v_f(t)$ for $t \geq 0$.
- Referring to Figure 10.94c, assume that the input to the buffer v_A undergoes a step transition from V_s to 0 V at $t = 0$. Write an expression for $v_C(t)$ for $t \geq 0$ for the step transition in v_A . (Hint: Refer to the sketch of v_f drawn in part (d).) The MOSFET in INV2 stays off for $v_B < V_T$, and turns on when $v_B \geq V_T$.) Sketch the form of $v_f(t)$ for $t \geq 0$.
- Write an expression for the fall time of the buffer for the circuit configuration shown in Figure 10.94c. (Hint: Refer to the sketch of v_C from part (e).) The fall time of the buffer is the time v_C requires to transition from V_H to the lowest voltage the input v_A makes a step transition from V_s to 0 V. Note that the fall time of the buffer is the sum of two components: (1) the internal buffer rise delay, or the time v_B takes to transition from its lowest voltage to V_T and (2) the additional time v_C takes to transition from V_s to V_L .)

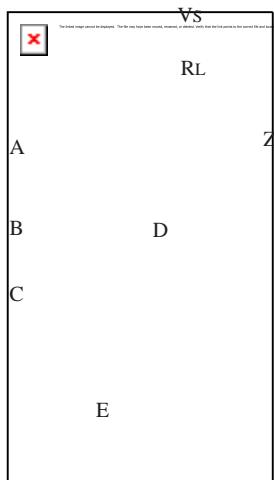


FIGURE 10.95

- g) Compute the rise time and the fall time for the buffer assuming that $R_{ON} = 1\text{k}\Omega$, $R_L = 10R_{ON}$, $C_{GS} = 1\text{nF}$, $V_S = 5\text{V}$, $V_L = 1\text{V}$, $V_T = 2\text{V}$, and $V_H = 3\text{V}$.
- h) What is the propagation delay of the buffer when the buffer output is connected to a single inverter using an ideal wire as shown in Figure 10.94c?
- i) Notice that unlike the delay calculation in Problem 10.1, we needed the value of V_T to obtain the buffer delay. Why was it necessary in the case of the buffer?
- j) An approximate value for the buffer delay can be obtained by doubling the individual inverter delay. Estimate the buffer delay by using the inverter delay computed in Problem 10.1b. What is the percentage error in the value of this estimated delay as compared to the accurate buffer delay computed in part (i) of this problem?

problem 10.3 The circuit depicted in Figure 10.95 implements the logic function $Z = (ABC + D)E$. Suppose the output of this circuit drives an inverter with a gate capacitance of C_G . Assume that the MOSFETs in the circuit have on resistance R_{ON} , and that the high and low voltage thresholds are $V_{IH} = V_{OH} = V_H$ and $V_{IL} = V_{OL} = V_L$, respectively.

- a) What combination of logical inputs will result in the worst-case fall time for the circuit?
- b) Derive an expression for the worst-case fall time in terms of V_S , R_L , R_{ON} , V_L , and V_H . Not all variables need appear in your answer.
- c) Derive an expression for the worst-case rise time.

problem 10.4 Figure 10.96 illustrates an inverter INV A connected to another inverter INV B by a wire of length l on a VLSI chip.



FIGURE 10.96

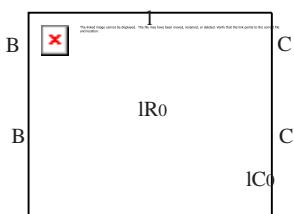


FIGURE 10.97

Figure 10.97 shows a lumped circuit model for the (nonideal) wire of length l in a VLSI chip, and Figure 10.98 shows the equivalent circuit model for the inverter pair connected by the nonideal wire based on the SRC model for the MOSFET. Assume that the logic devices satisfy a static discipline with voltage thresholds given by $V_{IL} = V_{OL} = V_L$ and $V_{IH} = V_{OH} = V_H$, and that the supply voltage is V_S .

Suppose INV A is driven by a 0 to 1 transition at its input (denoted v_{INA}) at $t = 0$. Determine $t_{pd,0 \rightarrow 1}$, the propagation delay through INV A for a 0 to 1 transition at its input. Recall that by our definition $t_{pd,0 \rightarrow 1}$ is the time taken by the input to INV B,

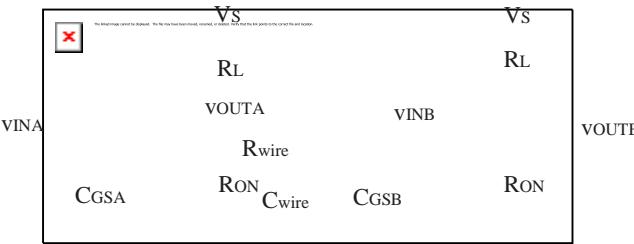


FIGURE 10.98

namely $V_{IN B}$, to fall from V_S to V_L following the 0-to-1 transition at the input of INV A. Express your answer in terms of V_S , V_L , R_{ON} , C_{GS} , the wire length L , and the wire model parameters. By what factor does the delay increase for a $2 \times$ increase in the wire length?

problem 10.5 Figure 10.99 illustrates an inverter INV A driving other inverters INV1 through INVn. As in Problem 10.1, each of the inverters is constructed using a MOSFET and a resistor R_L , and the inverters satisfy the static discipline with voltage thresholds $V_{IL} = V_{OL} = V_L$ and $V_{IH} = V_{OH} = V_H$. Model the MOSFETs using the SRC model with MOSFET on resistance R_{ON} and gate capacitance C_G as in Problem 10.1 (see Figure 10.93.)

- What are the rise and fall times for INV A? (Hint: Sum the input capacitances of each of the inverters into a single lumped value, and use your answer from Problem 10.1 to solve this part.) How does the rise time increase as the number of driven inverters n increases?
- What is the propagation delay t_{pd} of INV A in the circuit configurations shown in Figure 10.99, for $R_{ON} = 1\text{ k}\Omega$, $R_L = 10R_{ON}$, $C_{GS} = 1\text{ nF}$, $V_S = 5\text{ V}$, $V_L = 1\text{ V}$, and $V_H = 3\text{ V}$.
- Now, assume that each of the wires connecting the output of INV A to each of the inverters INV1 through INVn is nonideal as depicted in Figure 10.100. Model each of the wires using the model shown in Figure 10.101. Assuming that the input of INV A makes a step transition from 1 to 0, find the rise time at the input of anyone of the inverters INV1 driven by INV A.
- Compute the value of the rise time determined in part (c) for the following parameters: $R_{ON} = 1\text{ k}\Omega$, $R_L = 10R_{ON}$, $C_{GS} = 1\text{ nF}$, $R_W = 100\text{ }\Omega$, $C_W = 10\text{ nF}$, $V_S = 5\text{ V}$, $V_L = 1\text{ V}$, and $V_H = 3\text{ V}$.

problem 10.6 As can be seen from the answer to Problem 10.4, long wires have a serious negative impact on the delay. One way to alleviate the wire delay

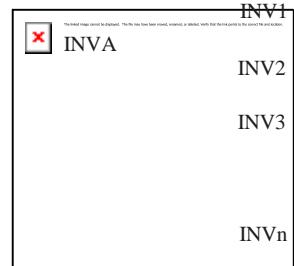


FIGURE 10.99

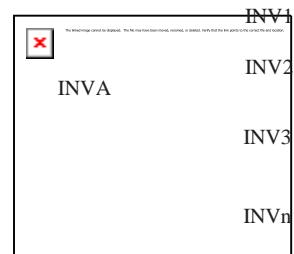


FIGURE 10.100

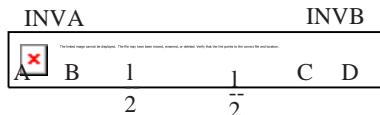


FIGURE 10.101

problem is to introduce buffers when driving long wires, as illustrated in Figure 10.102. Assume that the buffer is constructed as depicted in Figure 10.94 using a pair of inverters. The inputs to the inverters are labeled A and B, and the outputs are labeled C and D. The input to INV A is labeled A and its output is labeled B. The input to INV B is labeled C and its output is labeled D. The propagation delay from A to B is labeled 1, and the propagation delay from C to D is also labeled 1. The total propagation delay from A to D is labeled 2.

By introducing a buffer, the effective length of wire driven by either the inverter INV A or the buffer is $l/2$. For large l , given the nonlinear relationship between wire length and delay, the sum of the delays in driving the two $l/2$ wire segments is smaller than driving a single wire segment of length l .

FIGURE 10.102

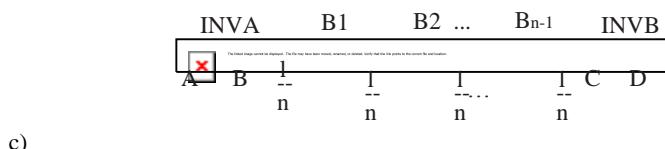


a) Compute the propagation delay between the input of INV A and the input of INV B for the circuit in Figure 10.102. Assume that rising transitions are longer than falling transitions at the output of either the inverters or the buffers.

(Hint: The total delay from the input of INV A to the output of INV B is the sum of the following two quantities: (1) the propagation delay of INV A driving the wire segment of length $l/2$ and a capacitance C_{GS} corresponding to the gate capacitance of the buffer, and (2) the propagation delay of the buffer driving the second wire segment of length $l/2$ and a capacitance C_{GS} corresponding to the gate capacitance of INV B. Remember, the buffer has zero delay when it is driving zero output capacitance.)

Figure 10.103 shows a circuit in which $n-1$ buffers are introduced between INV A and INV B. INV A and each of the buffers drives a segment of wire of length l/n . Compute the propagation delay between the input of INV A and the input of INV B for this case.

FIGURE 10.103



c)

Determine the number of buffers for which the propagation delay for the circuit in Figure 10.103 is minimized.

problem 10.7 Figure 10.104 shows a buffer BUF1 driving a large load capacitor C_L . The buffer is built using an inverter pair as in Figure 10.94c. The width-to-length ratio of each NMOS transistor in the buffer is W/L and the resistors have a value R_L .

Accordingly, the gate capacitance seen at the input of the buffer is given by $(W/L)C_{GS}$

The buffer satisfies a static discipline with voltage thresholds given by $V_{IL} = V_{OL} = V_L$ and $V_{IH} = V_{OH} = V_H$. The supply voltage is V_S . Assume that the internal buffer delay (as defined in Problem 10.2c) is zero. Assume that there is a 0-to-1 transition at the input A at time $t = 0$.

- Compute the propagation delay for the buffer BUF1 driving the load C_L for the rising transition at the input A.
- Now consider Figure 10.105. This figure shows the use of a second buffer with larger transistors and smaller valued load resistors ($x > 1$) interposed between the first buffer and the load capacitor. Compute the propagation delay for the buffer BUF1 in series with BUF2 driving the load C_L for the rising transition at the input A. Assuming that C_L is much larger than the input gate capacitances of the two buffers, and that $x > 1$, is the delay computed in part (b) greater than or less than the delay computed in part (a)?

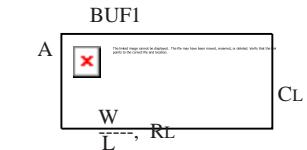
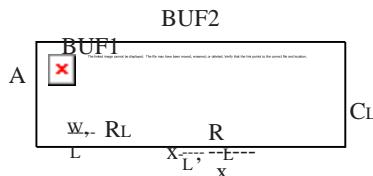


FIGURE 10.104

- Consider Figure 10.106. This figure shows the use of a series of n buffers in which BUF1 has transistors that have a width x times that of BUF $i-1$ and resistors that are a factor x smaller than that of BUF $i-1$. n is chosen such that C_L is six times the gate capacitance of BUF n . In other words, n satisfies the equation:

$$C_L = x^n W \quad \dots$$

Compute the propagation delay for the sequence of n buffers driving the load C_L for the rising transition at the input A. As before, assume that C_L is larger than the input gate capacitances of each of the buffers and that $x > 1$.

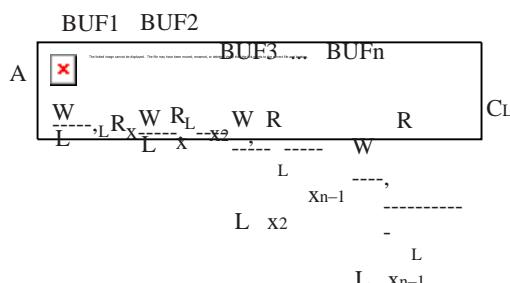


FIGURE 10.106

c) Determine the value of x for which the propagation delay computed in part (b) is minimized.

problem 10.8 In this problem, you will study the effect of parasitic inductances in VLSI packages. VLSI chips are sealed inside plastic or ceramic packages and connections to certain nodes of their internal circuitry (for example, power supply, ground, input nodes, and output nodes) need to be extended outside the package. These extensions are commonly accomplished by first connecting the internal node to a metallic “pad” on the VLSI chip. In turn, the pad is connected to one end of a package “pin” using a wire that is bonded to the pad at one end and the pin at the other. The package pin, which extends outside the package, is commonly connected to external connections using a PC board.

Together the package pin, the bond wire, and the internal chip wire are associated with a nonzero parasitic inductance. In this problem, we will study the effect of the parasitic inductance associated with power supply connections. Figure 10.107 shows a model of our situation. Two inverters with load resistors R_1 and R_2 and MOSFETs with width-to-length ratios W_1/L_1 and W_2/L_2 , respectively, are reconnected to the same power supply node on the chip that is labeled with a voltage V_P . Ideally this chip-level power supply node would be extended with a metal wire outside the chip to the external power supply V_S shown in Figure 10.107. However, notice the parasitic inductance L_P interposed between the power supply node on the chip (marked with voltage V_P) and the external power supply node (marked with voltage V_S .)

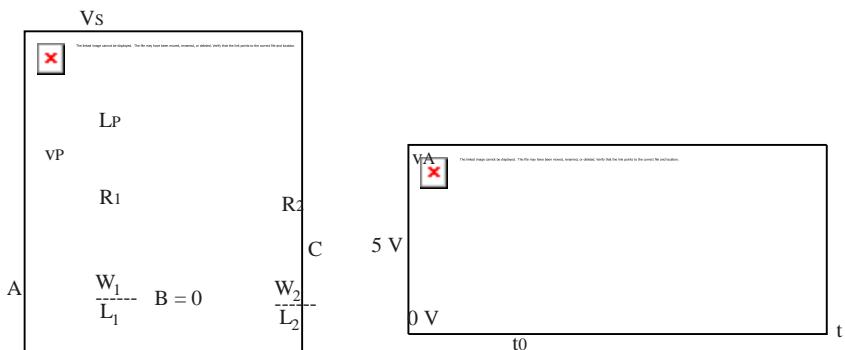


FIGURE 10.107

Assume that the input B is 0 V at all times. Assume further that the input A has 0 V applied to it initially. At time $t = t_0$, a 5-V step is applied at the input A . Plot the form of v_A as a function of time. Clearly show the value of v_A just prior to t_0 and just after t_0 . Assume that the ON resistance of a MOSFET is given by the relation $(W/L)R_n$ and that MOSFET's threshold voltage is $V_T < V_S$. Also assume that $V_T < 5$ V.

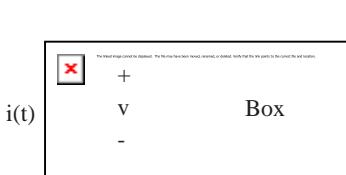


FIGURE 10.108

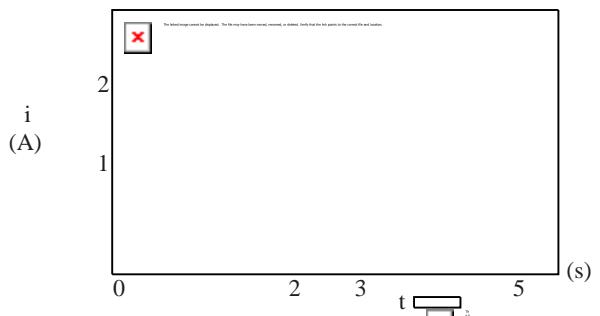


FIGURE 10.109

problem 10.9 A certain box, known to contain only linear elements (and no independent sources), is connected as shown in Figure 10.108.

The current waveform $i(t)$ has the form shown in Figure 10.109.

The voltage is zero for all $t < 0$, and is 1 volt for $0 < t < 2$. What is v during the interval from $t=2$ to $t=5$? Show one simple possibility for the circuit in the box.

problem 10.10 As illustrated in Figure 10.110, a capacitor and resistor can be used to filter or smooth the waveforms we derived from a half-wave rectifier, to get something closer to a DC voltage at the output, for use in a power supply, for example.

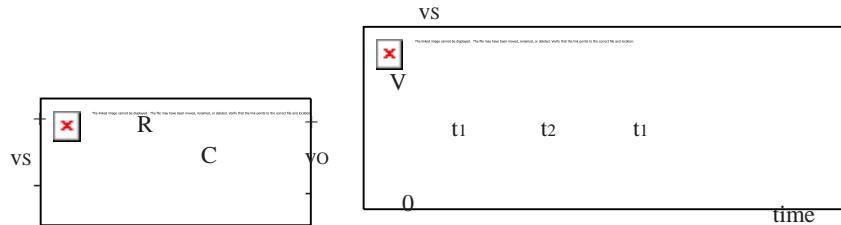


FIGURE 10.110

For simplicity, assume the voltage from source vs is a square wave. Assume that at $t=0$, $v = 0$, that is, the circuit is at rest. Now assuming that R is small enough to make the circuit time constant much smaller than τ , calculate the voltage waveforms for each half cycle of the input wave. Find the average value of the output voltage v_o for $t_1=t_2$.

Sketch the waveforms carefully. For this choice of R , it should be clear that no useful smoothing has been accomplished.

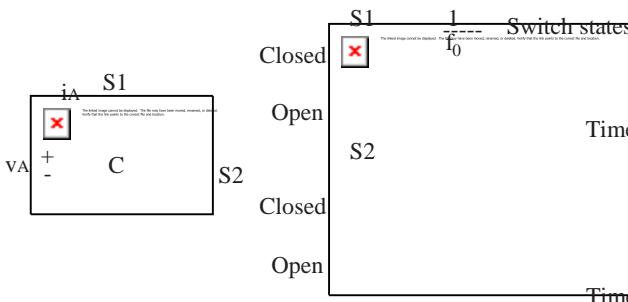
problem 10.11 For R much larger than the value used in Problem 10.10, so that the circuit time constant is much larger than τ or t_2 , (so that the exponentials can be approximated by straight lines) calculate v_o for the first half cycle of vs , and the second half cycle. Sketch the result. Note that the solution does not return to the initial point of $v_o=0$ after one cycle, so is not in the “steady state” yet.

problem 10.12 You can see from Problem 10.10 that for circuit time constant $\tau = t_2 - t_1$ and t_2 the capacitor voltage starts from some value V_{\min} and increases when v is positive; then when v is zero, v starts at some value V and decreases. By definition, the “steady state” of the circuit is when v charges from V_{\min} to V_{\max} , then discharges from V_{\max} to the same V_{\min} . Assuming $t_1 = t_2$, sketch the voltage waveform in the steady state.

Find the average value of the voltage v . Problem 10.11 may give you a hint. Explain your answer. It may help to consider the waveform v_S to be made up of a DC voltage $V/2$ and a symmetrical square wave whose values alternate between $+V/2$ and $-V/2$.

problem 10.13 This problem (see Figure 10.111) involves a capacitor and two switches. The switches are periodically driven by external clock controls at frequency f_0 such that first S_1 is closed and S_2 is open for time $\frac{1}{2}f_0$, and then S_2 is closed and S_1 is open for time $\frac{1}{2}f_0$.

FIGURE 10.111



You can assume that the clock drives are non-overlapping; that is, S_1 and S_2 are never both closed at the same instant. S_1 opens just before S_2 closes, and S_2 opens just before S_1 closes.

- Find an effective average current i_A by determining the average rate of charge transfer over several clock cycles. Suppose $v_A = A \cos(\omega t)$ where $\omega = 2\pi f_0$. Sketch i_A and v on the same axes.
- Examine your results for i_A and v_A from part (a). They should be in phase, and the amplitude of i_A should be proportional to the amplitude of v_A . This is a funny form of “resistor.” What is the “resistor” value? Where does the energy supplied by v_A actually go?

(Comment: Circuits of this type are now commonly used in a type of MOS integrated circuit to make elements that simulate resistors with precisely controlled values. The value of such elements is that precise control of capacitor sizes and clock frequencies is easy in MOS integrated circuits, but precise control of resistor values is hard.)

problem 10.14 State variables can be used to describe the behavior of a wide range of physical systems. For each of the examples below, try to determine the following:

- i) The number of state variables that are needed to describe the system, that is, how many state variables.
- ii) Which physical variables can serve as state variables.
- iii) The form of the state equations, including the identification of inputs.
- iv) A simple circuit that can represent the system (an electrical analog.)

Here are the examples:

- a) A hockey puck leaves a hockey player's stick with velocity v_0 and slides along the ice until it comes to rest (assume a very large hockey rink, or a very weak shot.)
- b) Halfway through your shower each morning, the water temperature suddenly plunges toward freezing, presumably because your roommates were up earlier and showered first.
- c) A simple pendulum starts from rest with an initial angular displacement θ_0 , and rocks back and forth until it eventually comes to rest.

(COMMENT: Part (a) is easy if you concentrate only on the velocity, and is more difficult in terms of the circuit analogy if you include the position as well. Parts (b) and (c) lend themselves to excellent descriptions with circuit analogs.)

problem 10.15 Figure 10.112 shows the use of a filter choke.

Assume that the waveform for v_s for parts (a) and (b) is a series of square pulses starting at $t=0$ as shown in Figure 10.113.

Assume that the waveform for v_s for parts (c) and (d) is a half-rectified sine wave as shown in Figure 10.114.

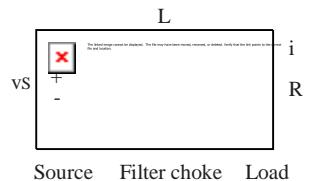


FIGURE 10.112

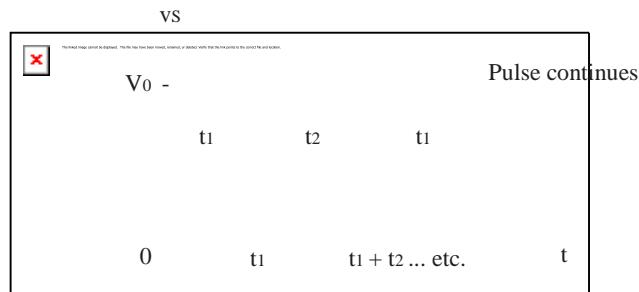


FIGURE 10.113

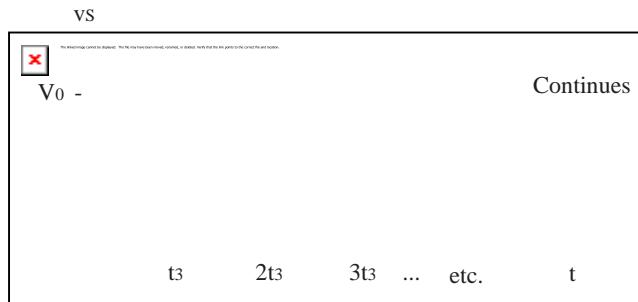


FIGURE 10.114

a) Assume initial rest conditions at $t=0$, and assume that both t_1 and t_2 are long compared to the time constant of the network. Determine each of the following:

- Calculate the current waveform for the first cycle ($0 \leq t < t_1 + t_2$), the second cycle [$(t_1 + t_2) \leq t \leq 2(t_1 + t_2)$], and a typical cycle after steady-state periodic conditions have been reached.
- How many cycles are required to go from initial rest to steady-state conditions?
- In steady state, determine the average load current, the amplitude of the variations in load current through one cycle, the average energy stored in the inductor, and the ratio of this stored energy to the energy dissipated in the load during one complete cycle.

b) Repeat part (a) for the case where both t_1 and t_2 are short compared to the time constant of the network.

c) Now assume that as a filter designer, you are faced with the problem of selecting the inductor value to produce a relatively smooth, ripple-free current in a load from a voltage source with a strongly pulsating value, such as the half-wave rectified sine waves shown in Figure 10.114. What method would you use to specify the inductor value with which to achieve a specified maximum variation in load current? Why might the specifications of a huge L value, much larger than might be needed, be a poor design?

d) Try your hand at a design: Assume that the source waveform is half-wave rectified 60 Hz 115 VAC, the load resistor is 16.2, and it is desired to have a load current ripple of 5% of the average load current. Make reasonable approximations.

problem 10.16 Consider the circuit shown in Figure 10.115.

a) Plot v_R and v_C for several cycles of the indicated input waveform. Assume the RC time constant is $10t_1$.

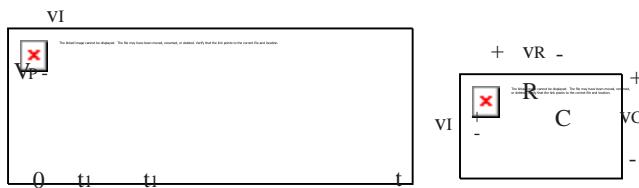


FIGURE 10.115

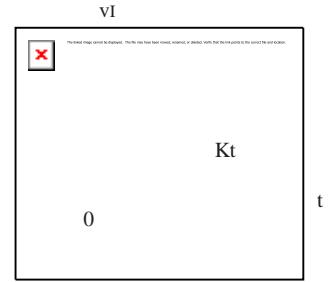
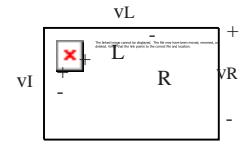
b) During the first several cycles, the v_C waveform does not repeat, but after some time, v_C is cyclic. Find and sketch this cyclic waveform. Dimension key values.

problem 10.17 Referring to Figure 10.116, for $v_I = Kt$, a ramp starting at $t=0$, find expressions for v_R and v_L . Plot the waveforms.

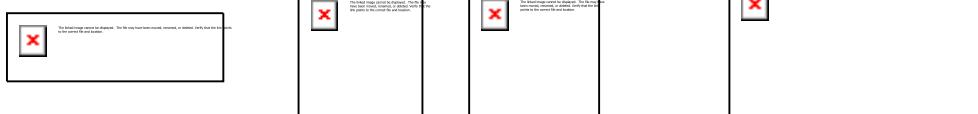
problem 10.18 Referring to Figure 10.117, given an initial inductor current $i_L(0)=1\text{ mA}$, find the expression for v_R and v_L . Plot the waveforms.

problem 10.19 The purpose of this problem is to illustrate the important fact that although the zero-state response of a linear circuit is a linear function of its input, the complete response is not. Consider the linear circuit shown in Figure 10.118.

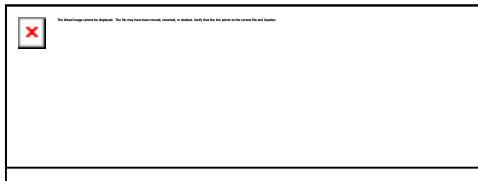
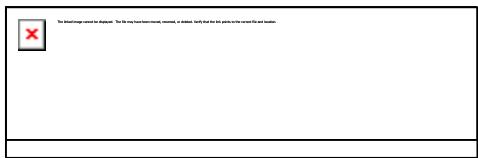
a) Let $i_L(0)=2\text{ mA}$. Let i_1 and i_2 be the responses resulting from voltages e_1 and e_2 applied one at a time, where



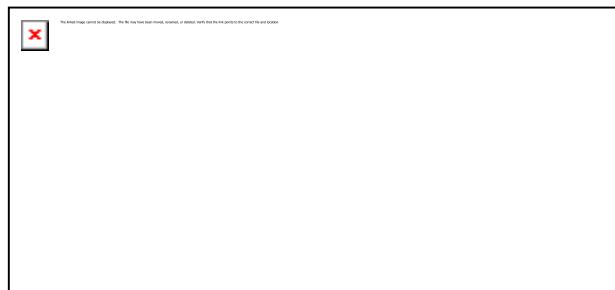
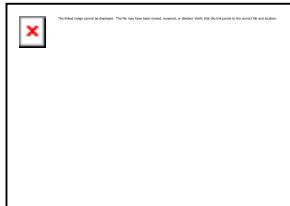
$$e_1 =$$

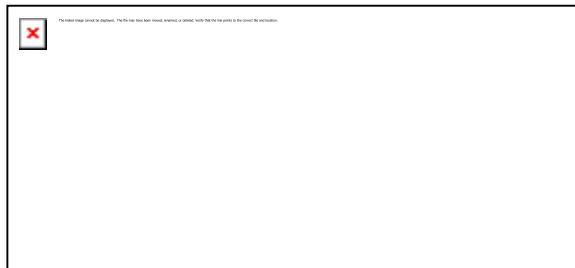


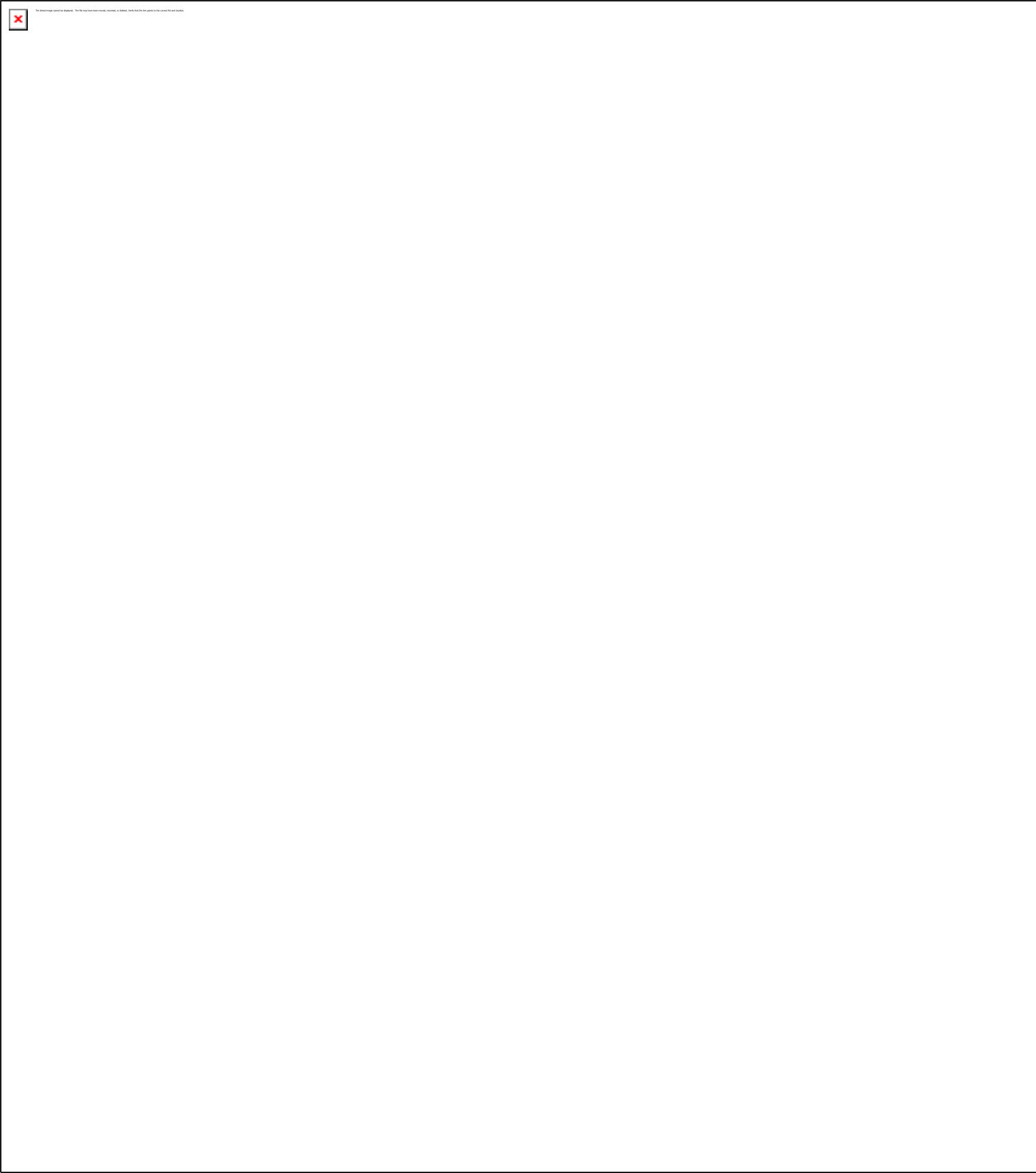




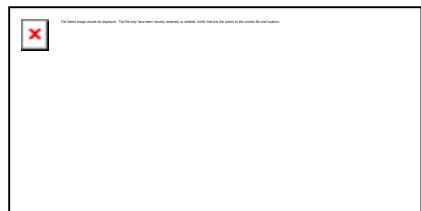












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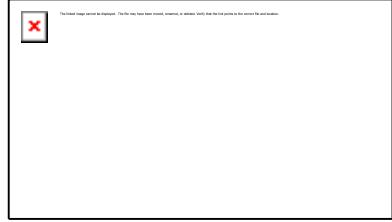
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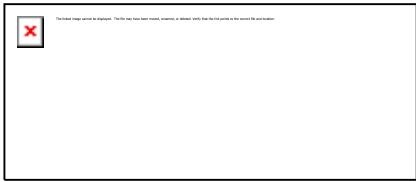
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File and try again.

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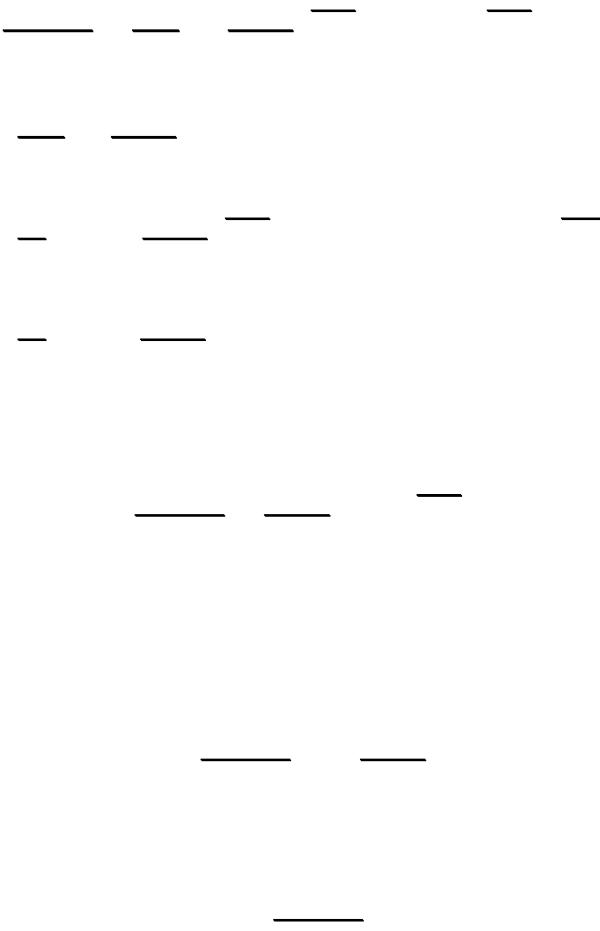


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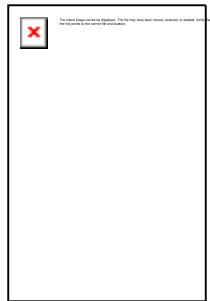
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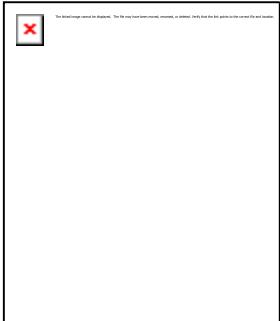
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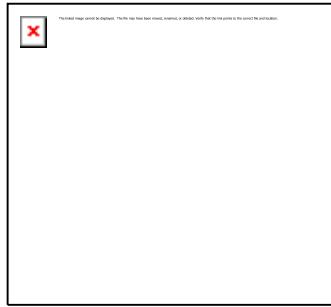
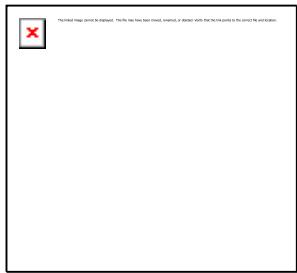
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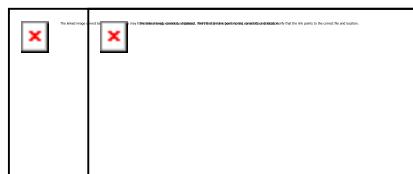
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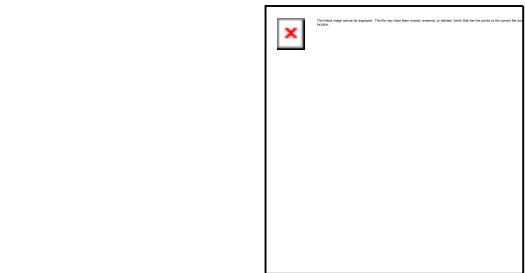
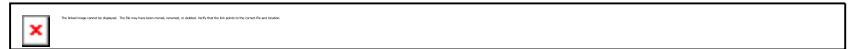
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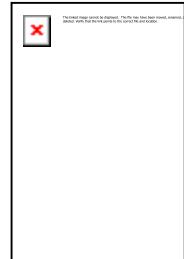
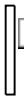
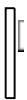
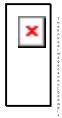
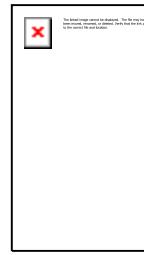
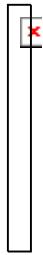
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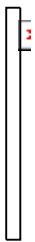
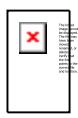
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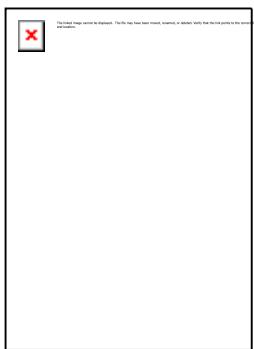
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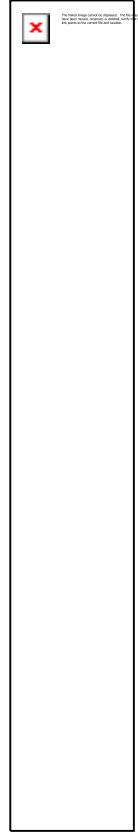
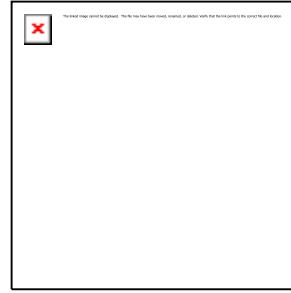
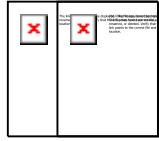
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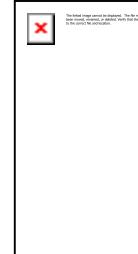








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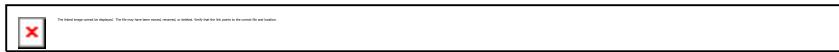
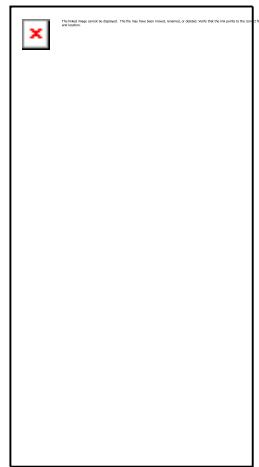
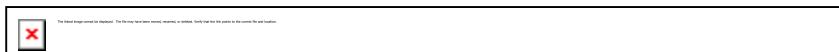
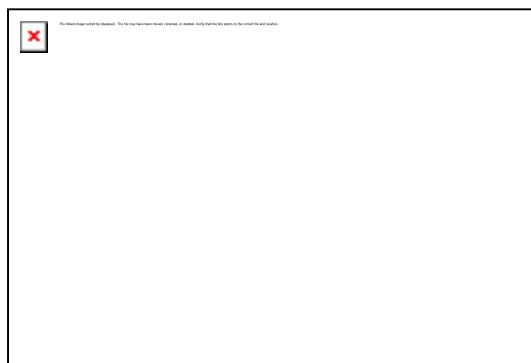
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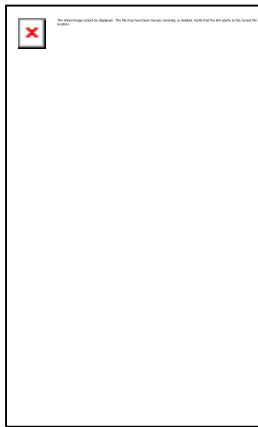
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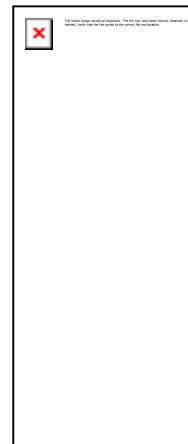
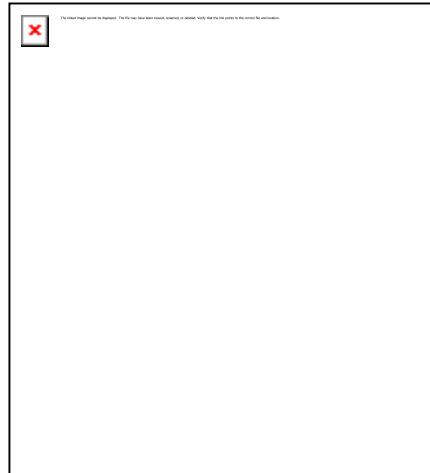
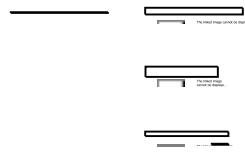
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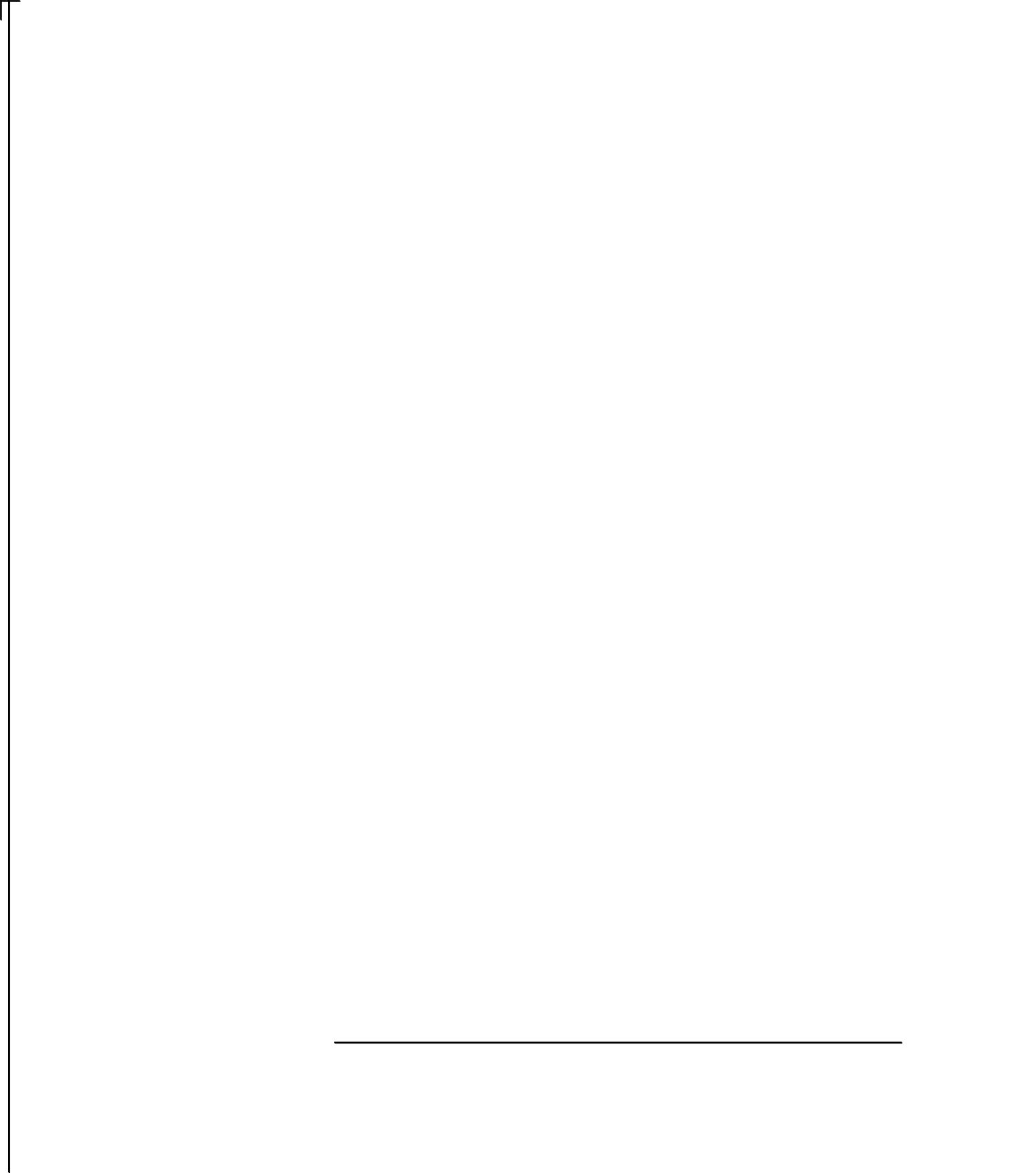




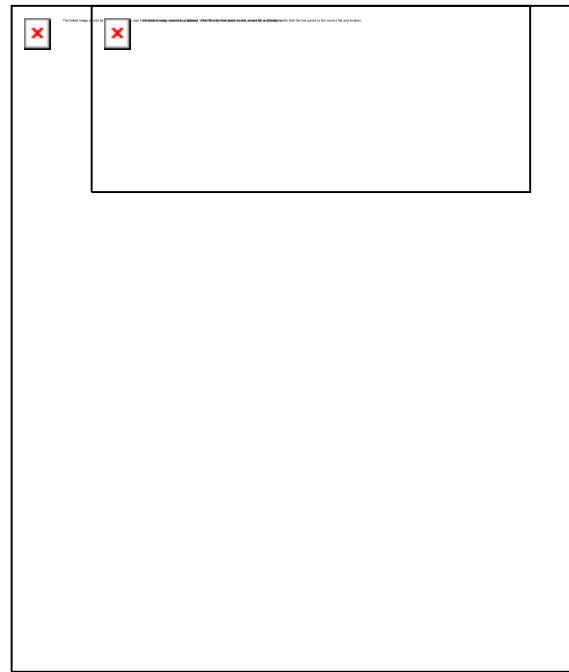




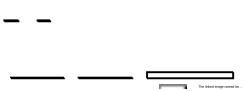
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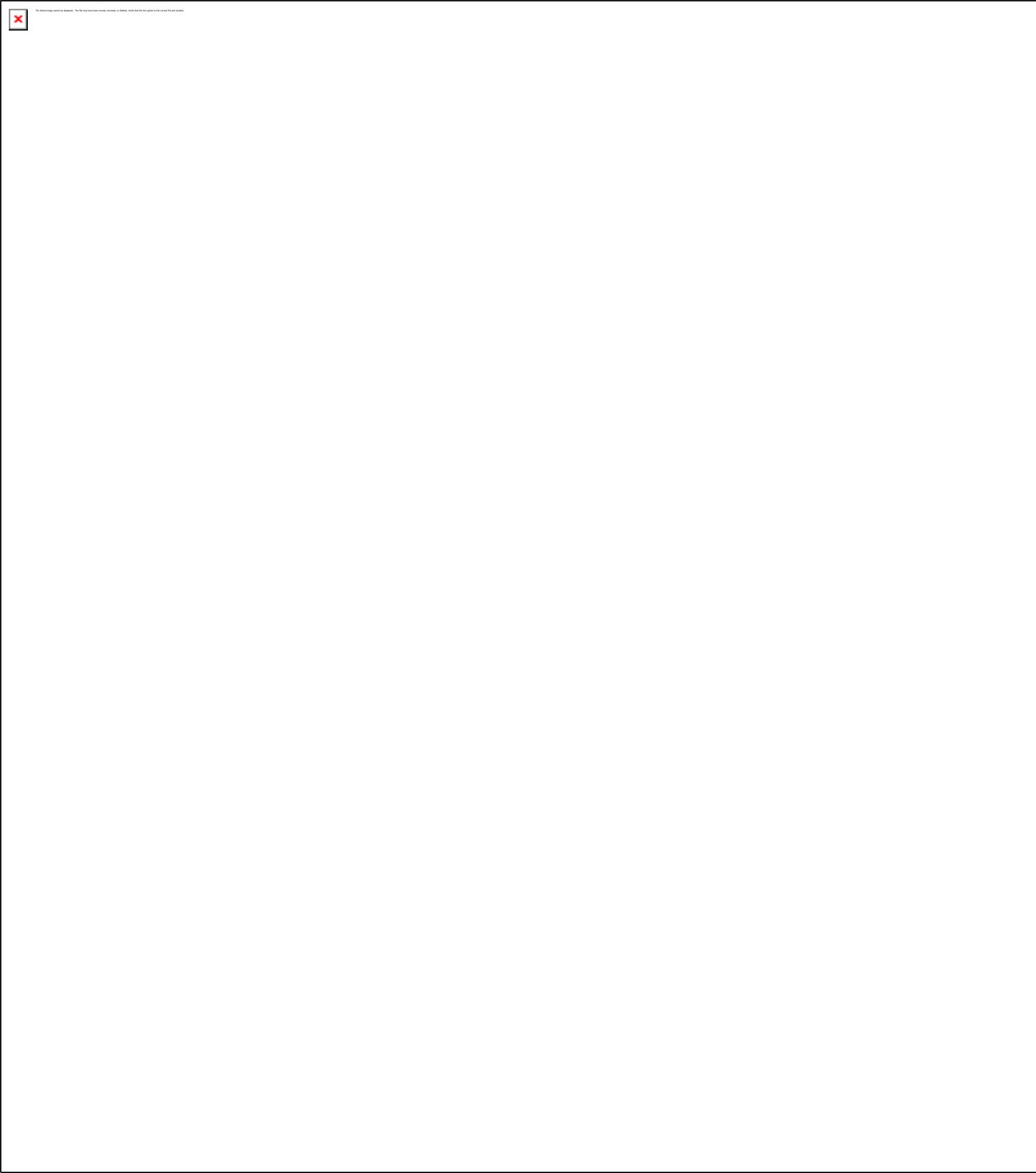


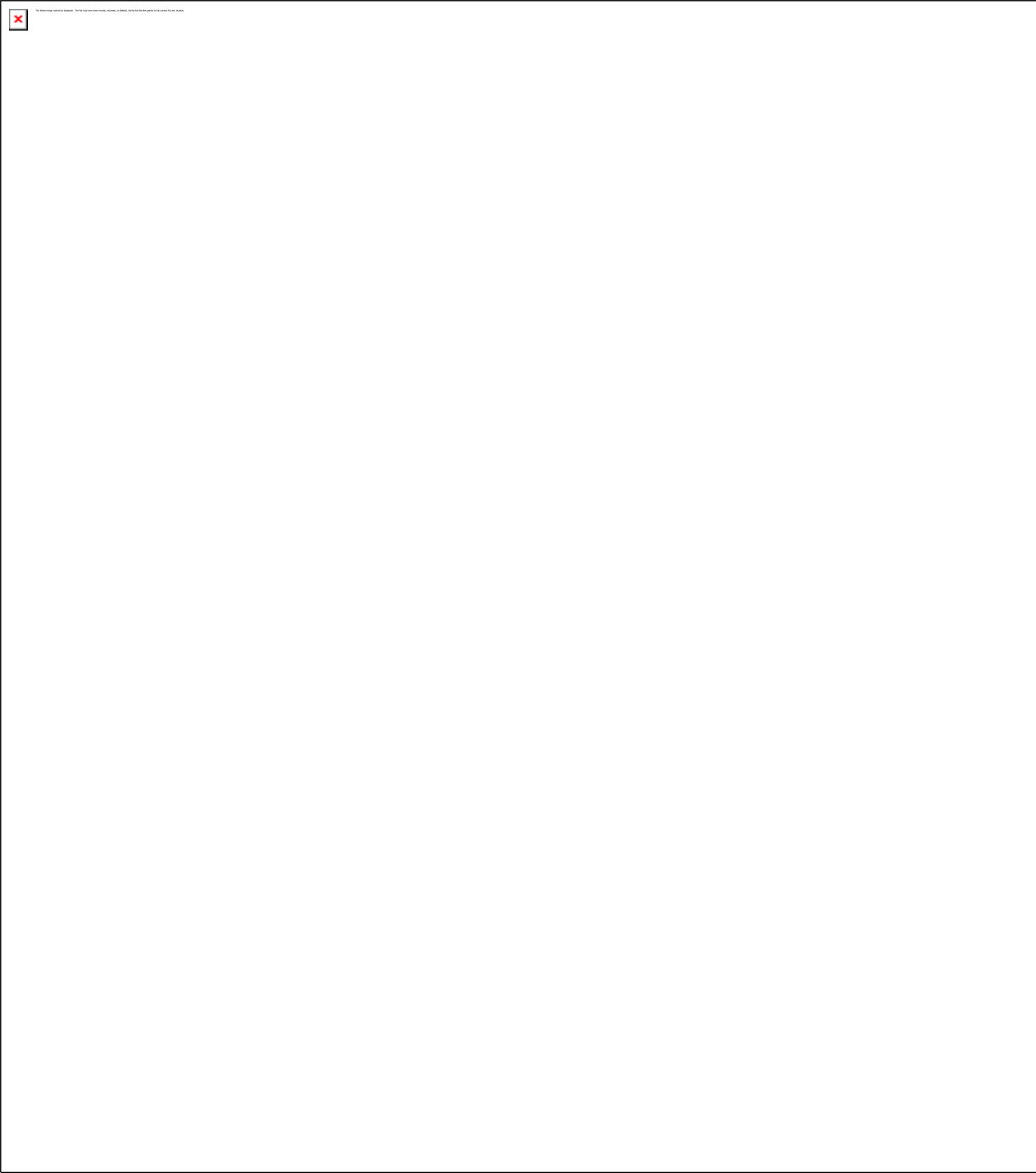


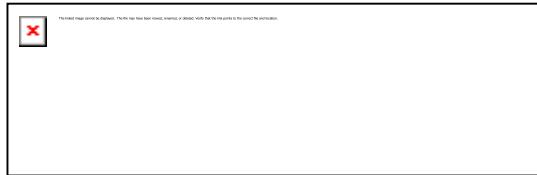
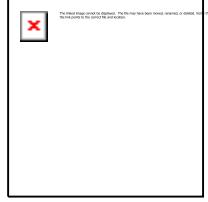


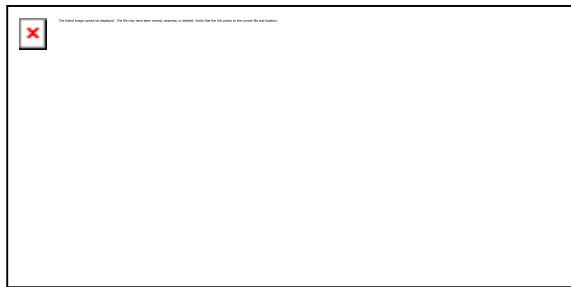
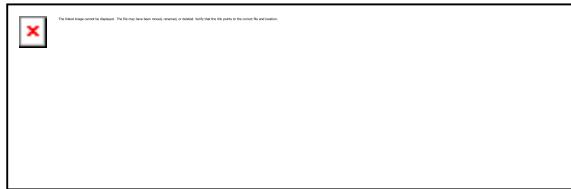


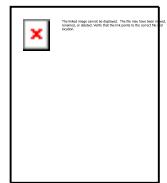












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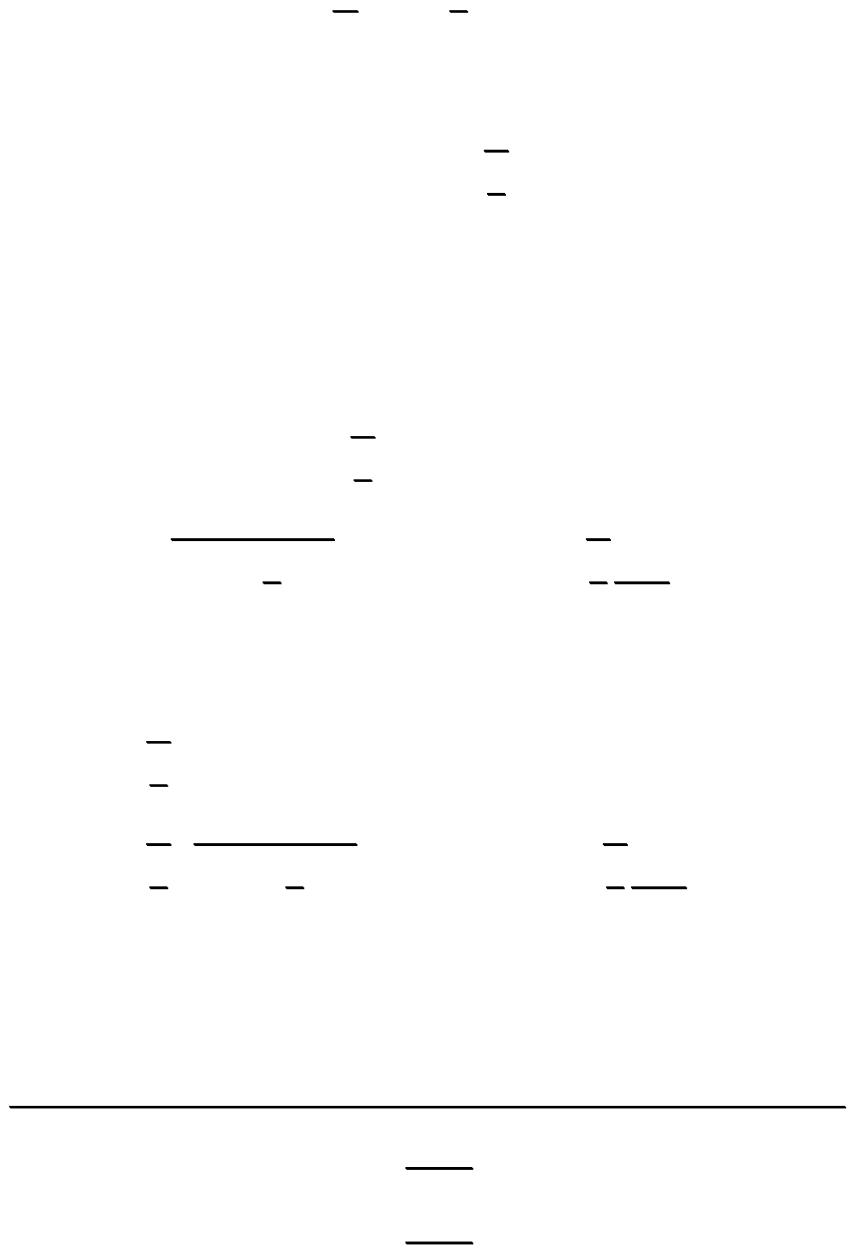
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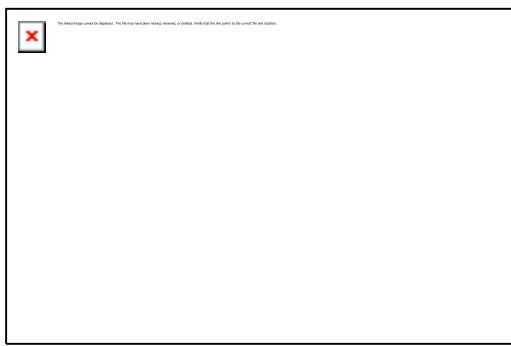
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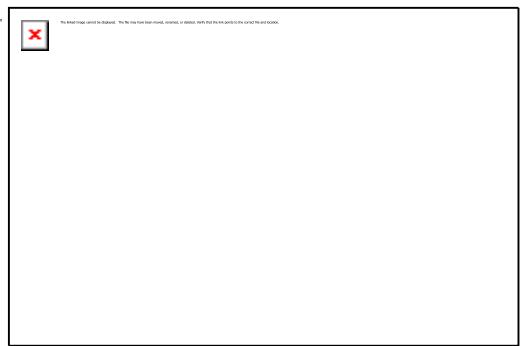
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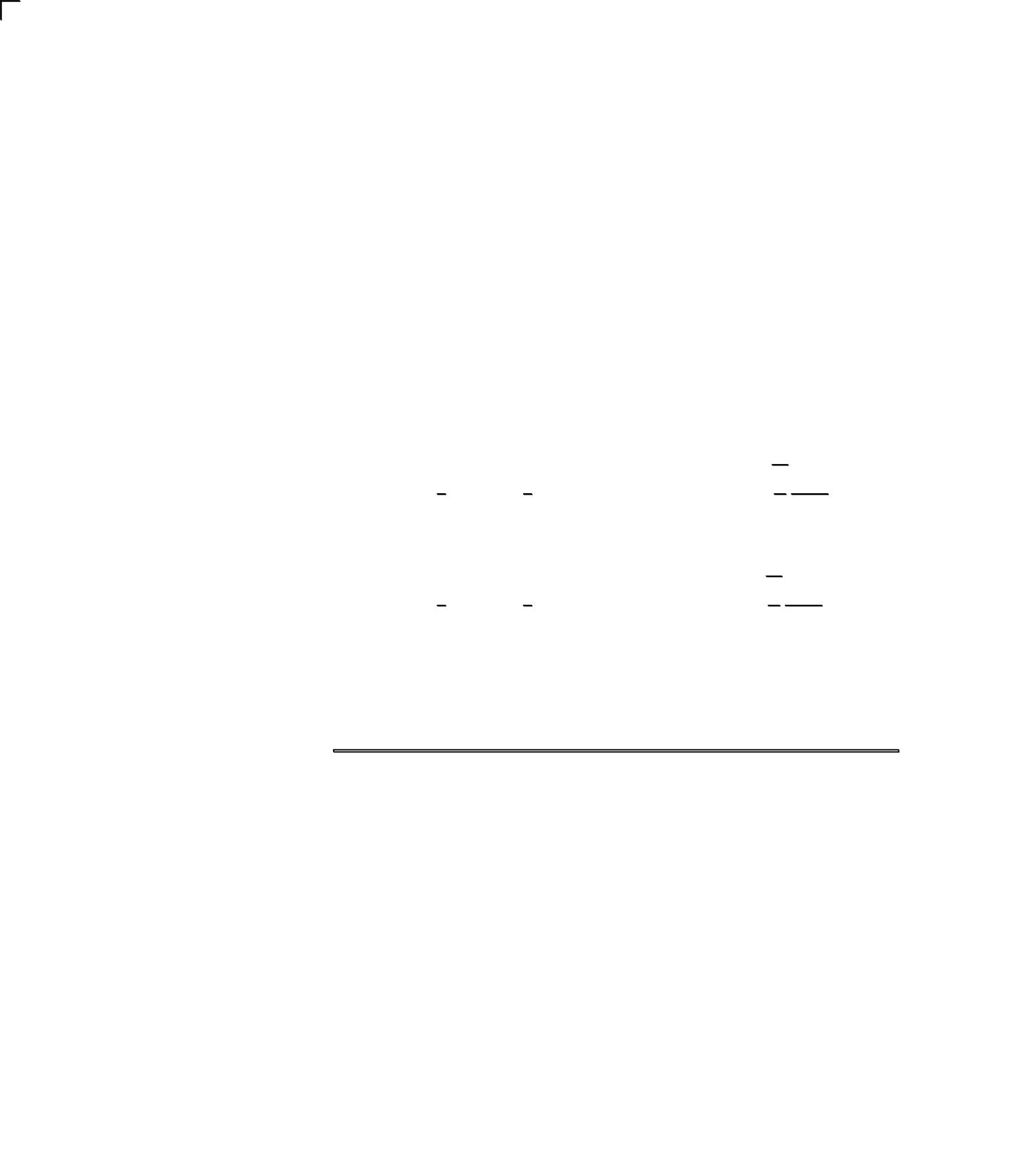


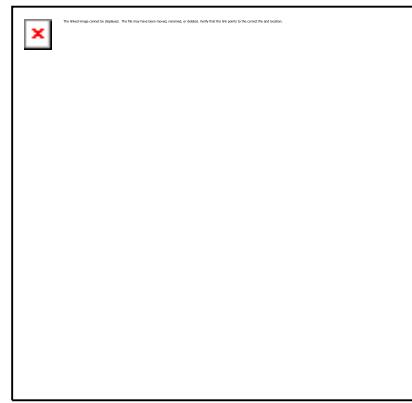
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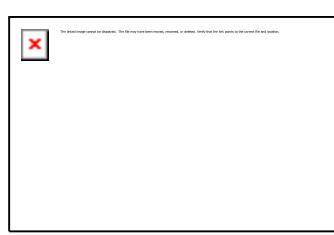
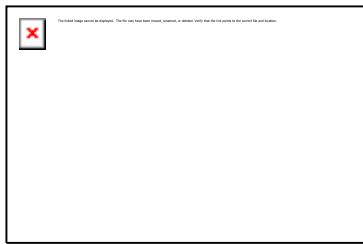
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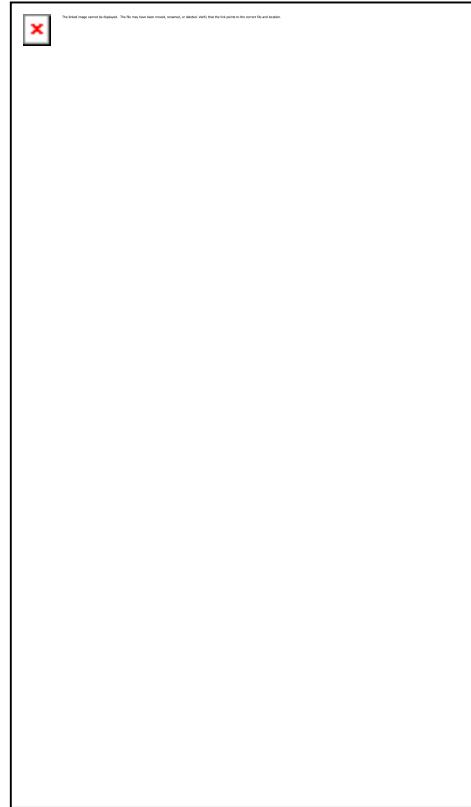


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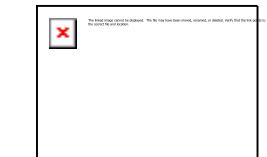
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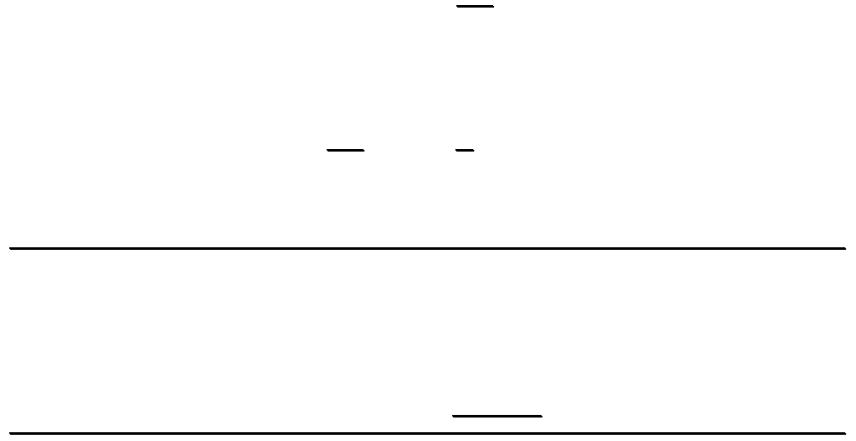


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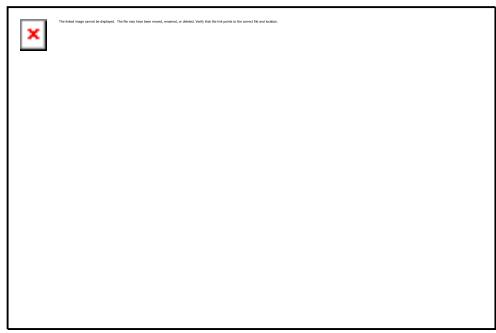
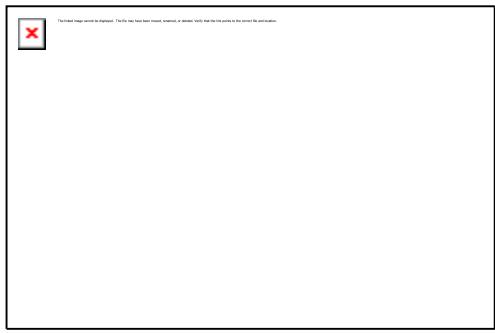
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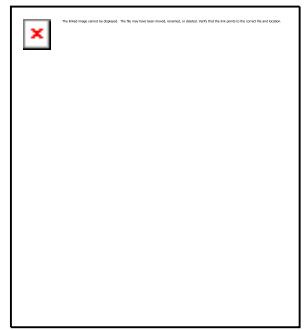
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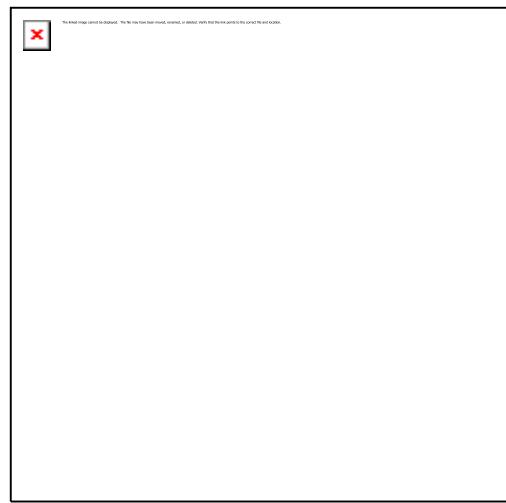
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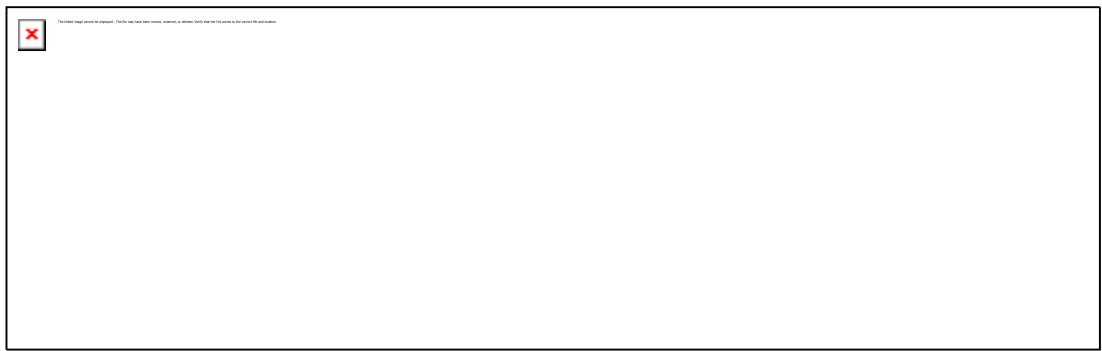
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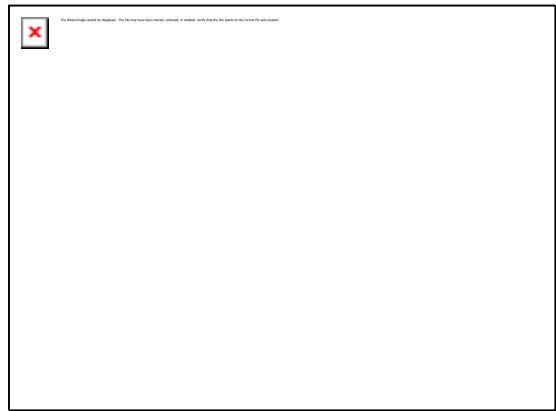




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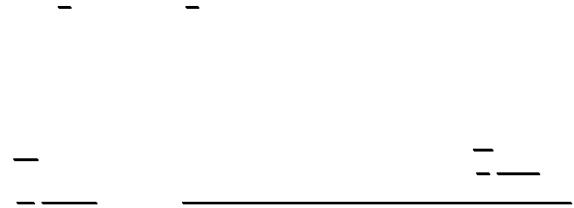
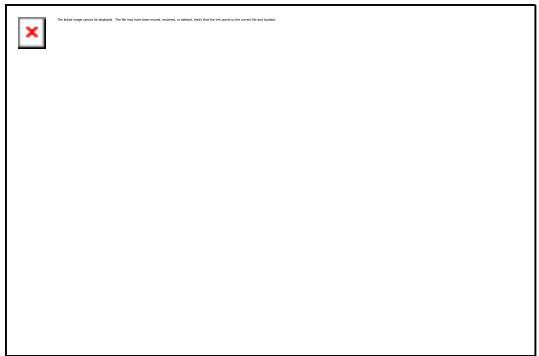
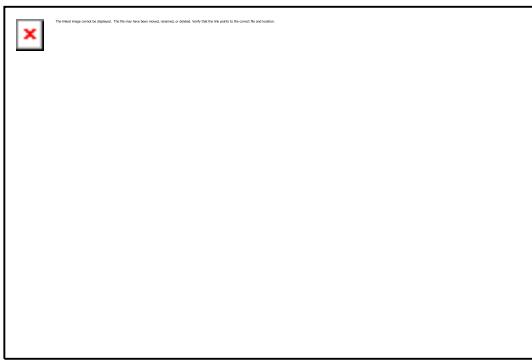
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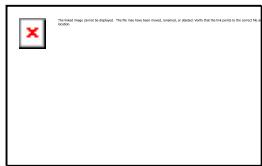
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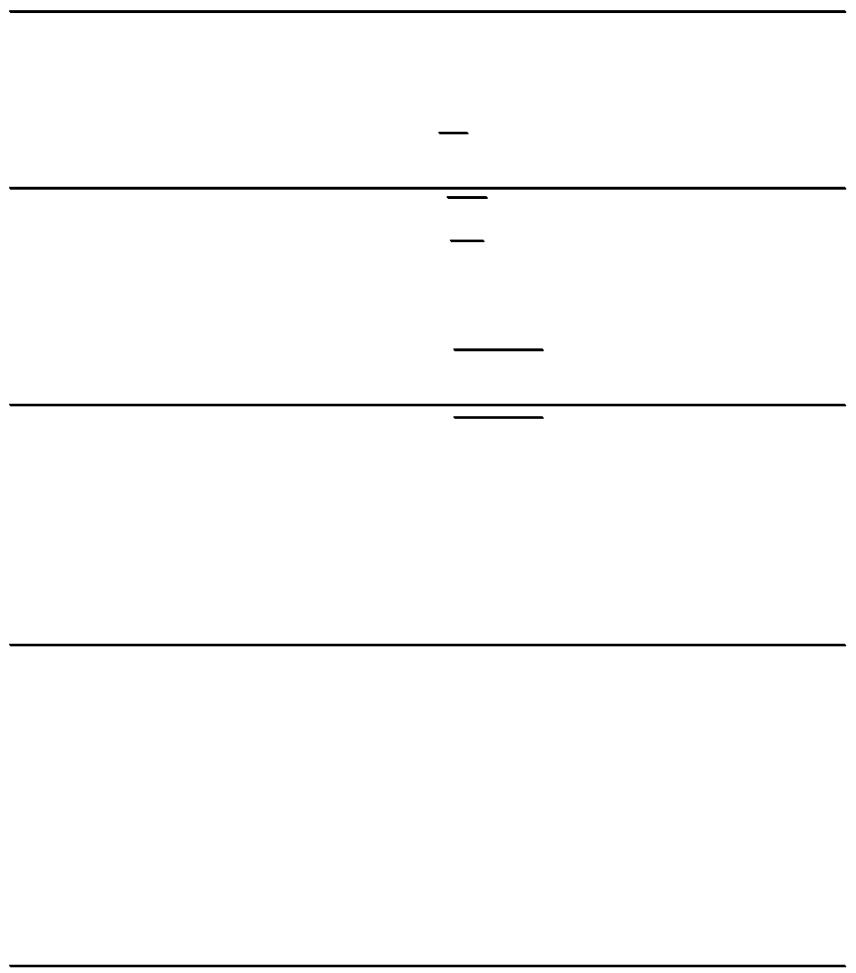
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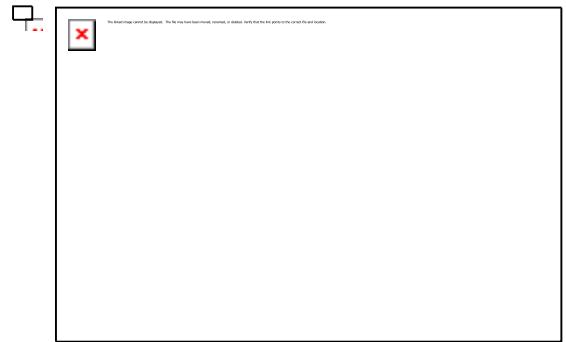
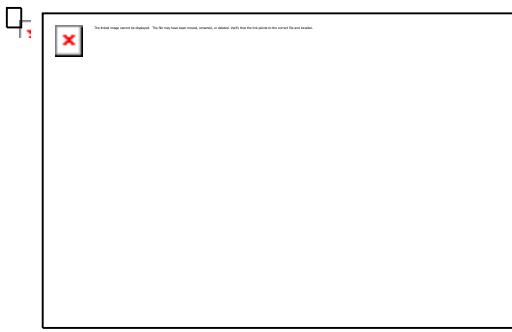
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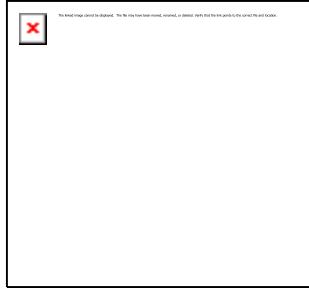
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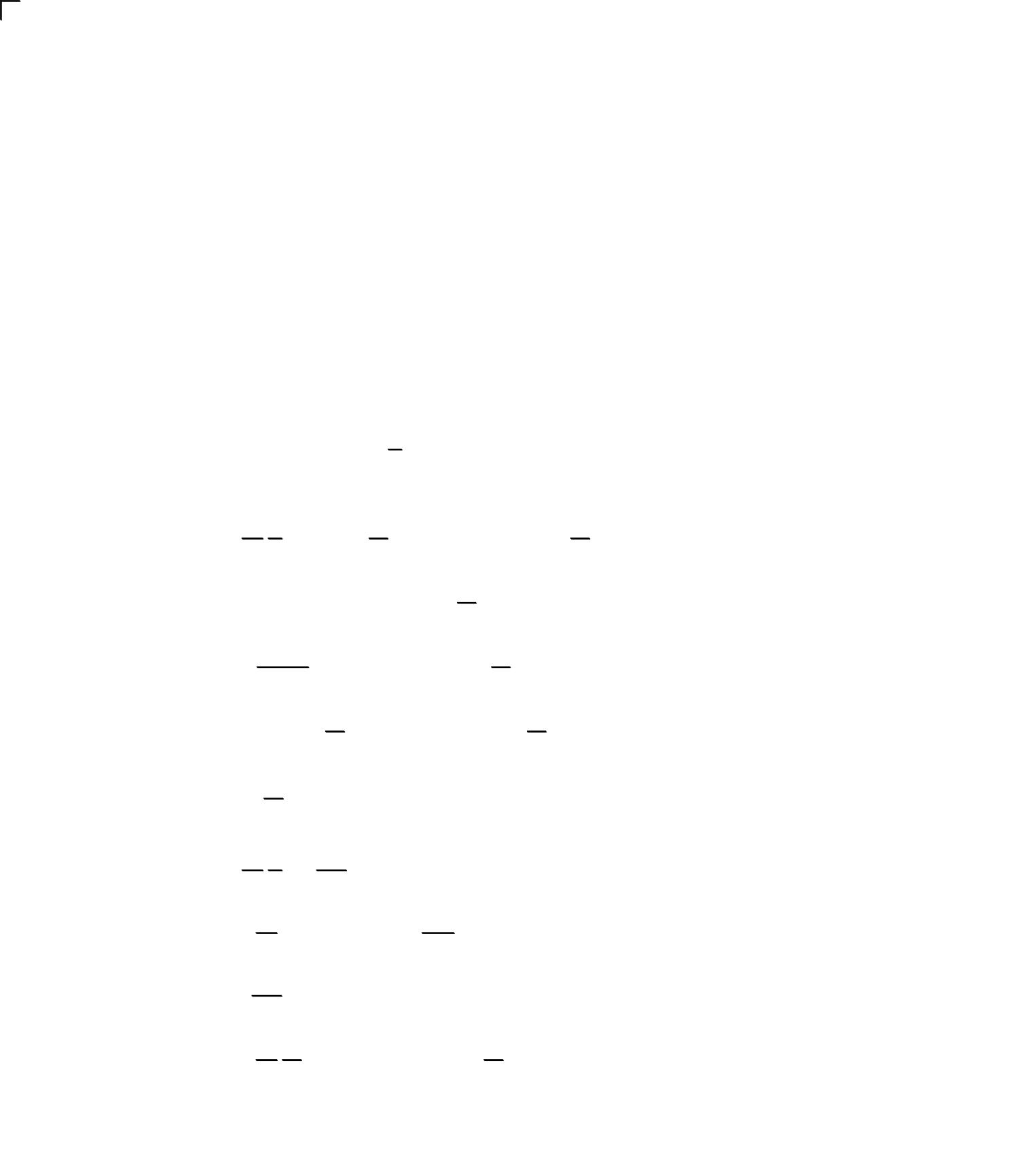
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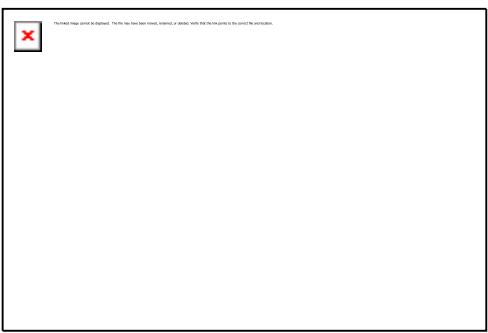




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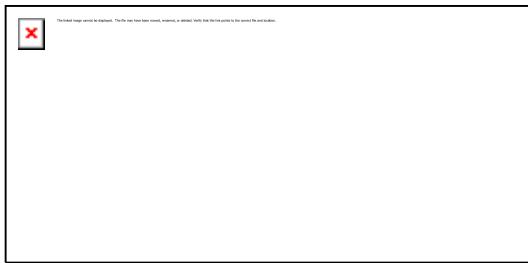
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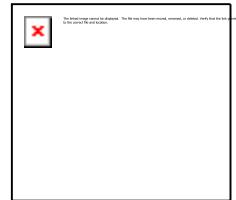
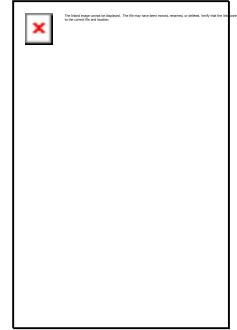
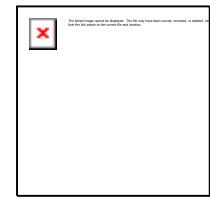
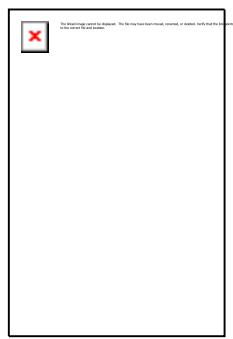


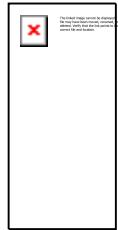
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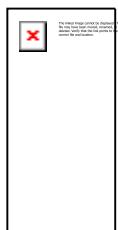






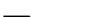
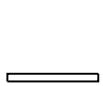
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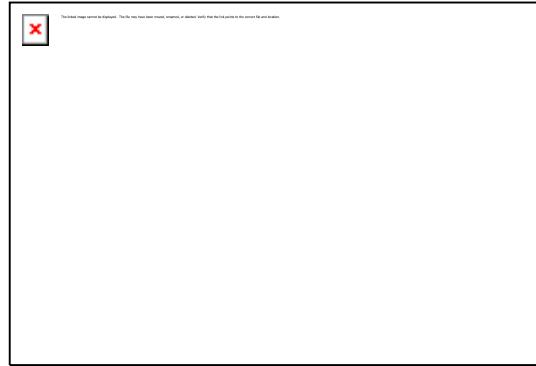
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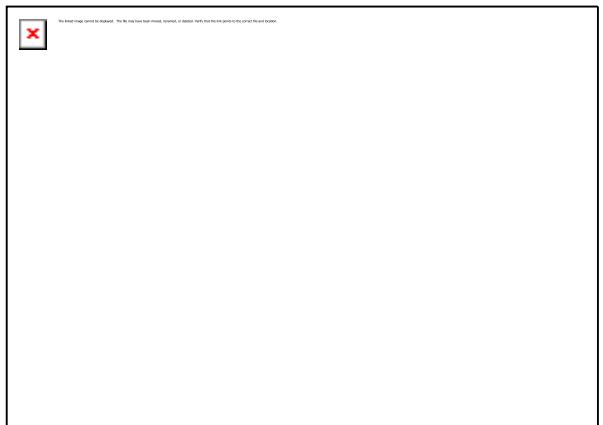
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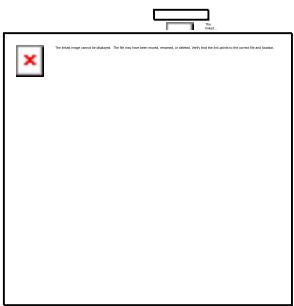
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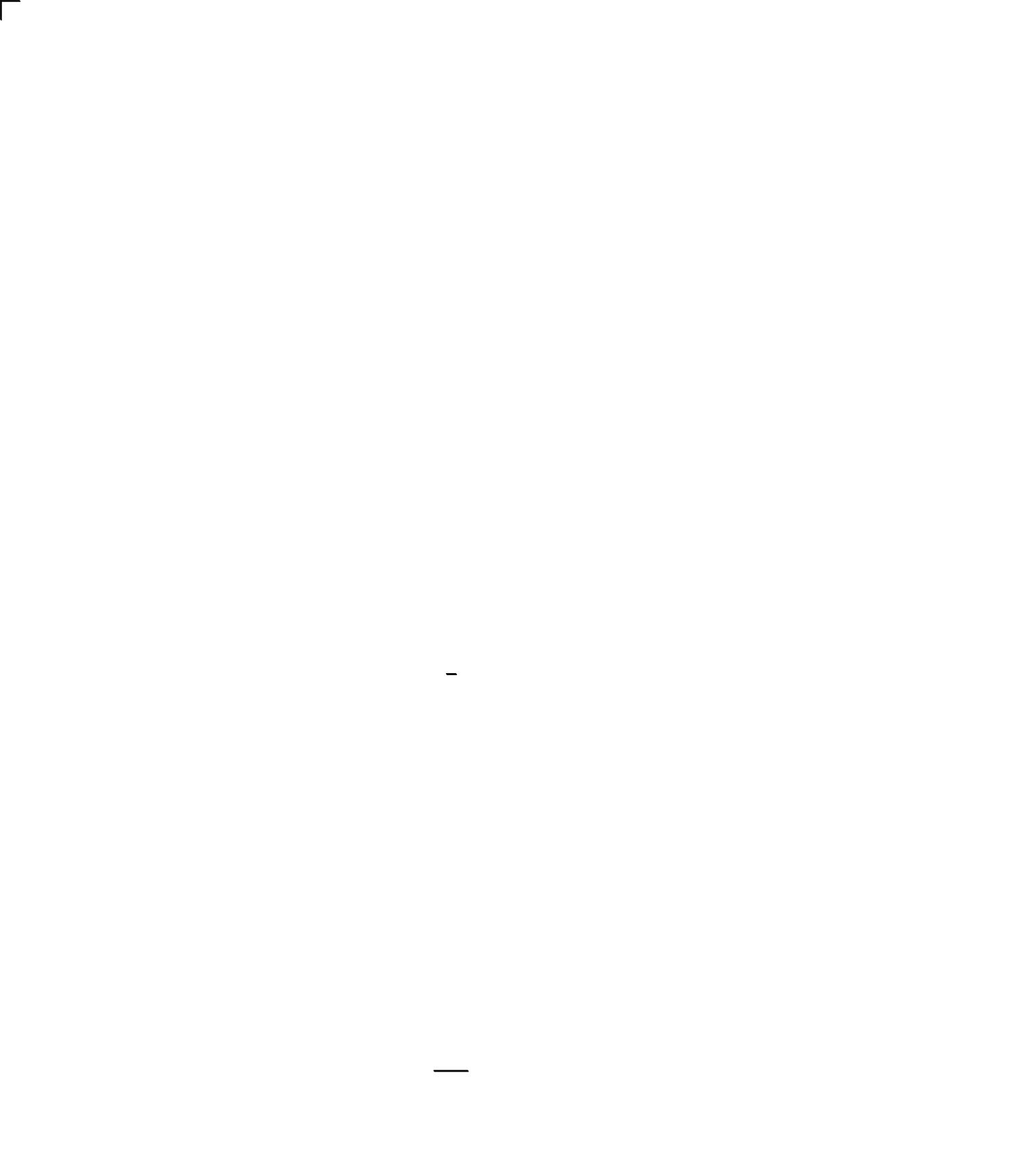




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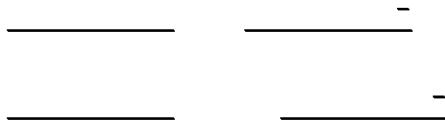
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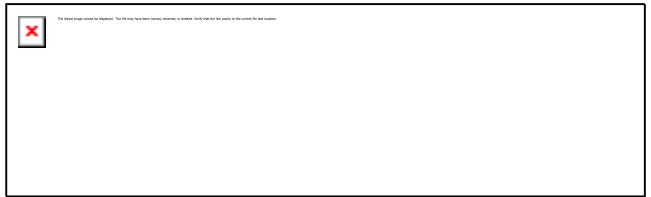
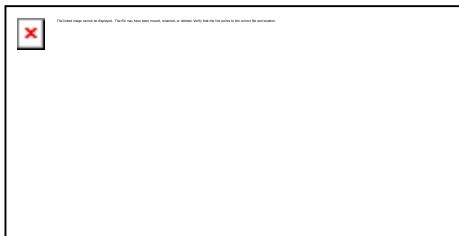
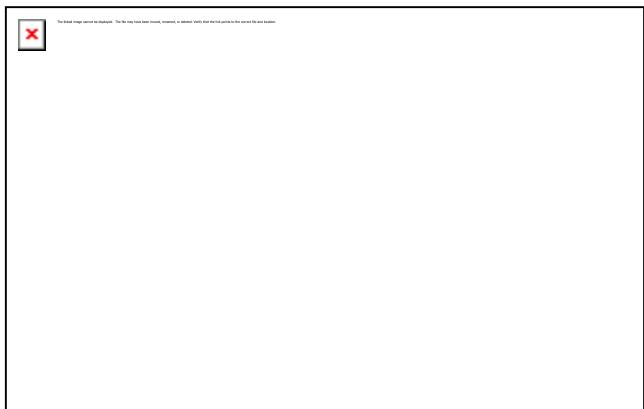




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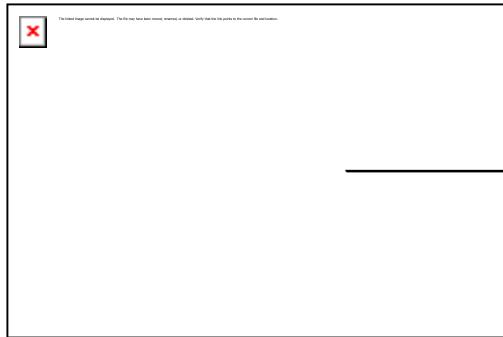


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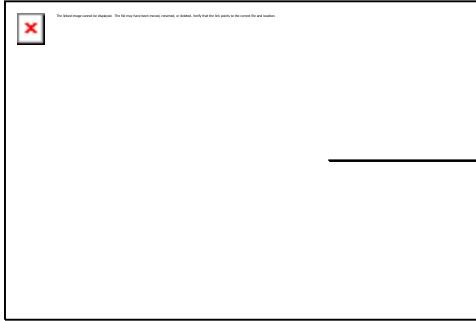
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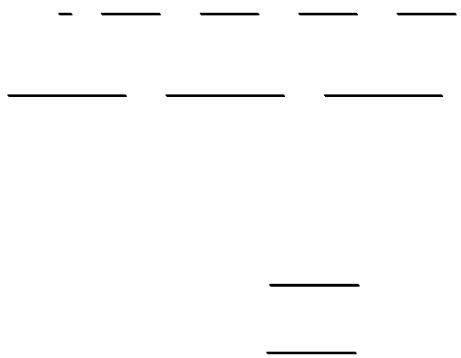
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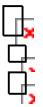


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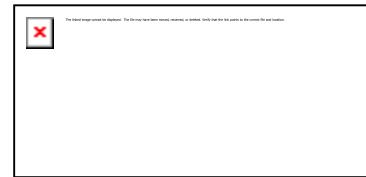
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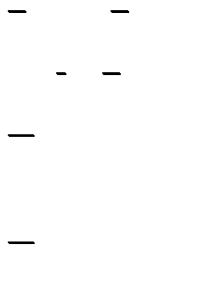
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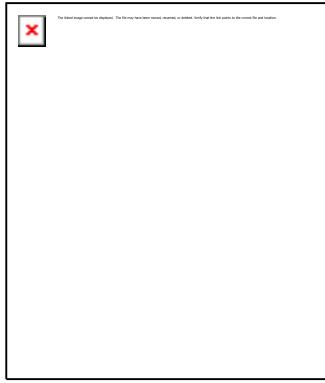
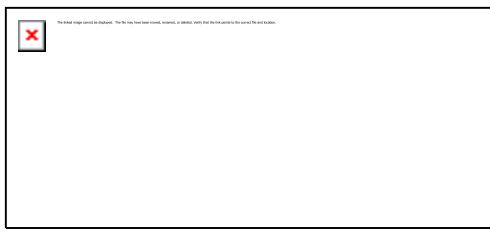
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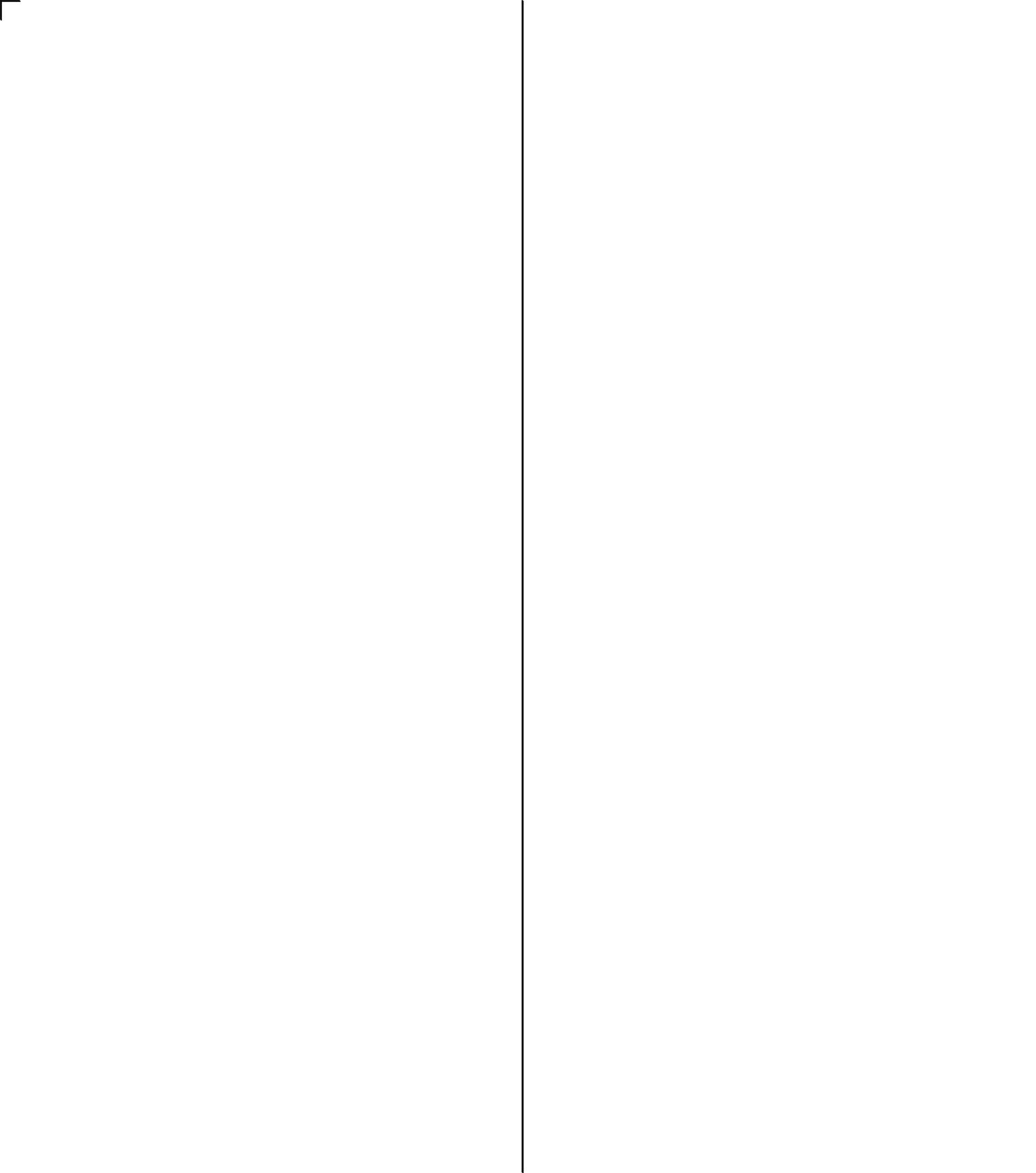


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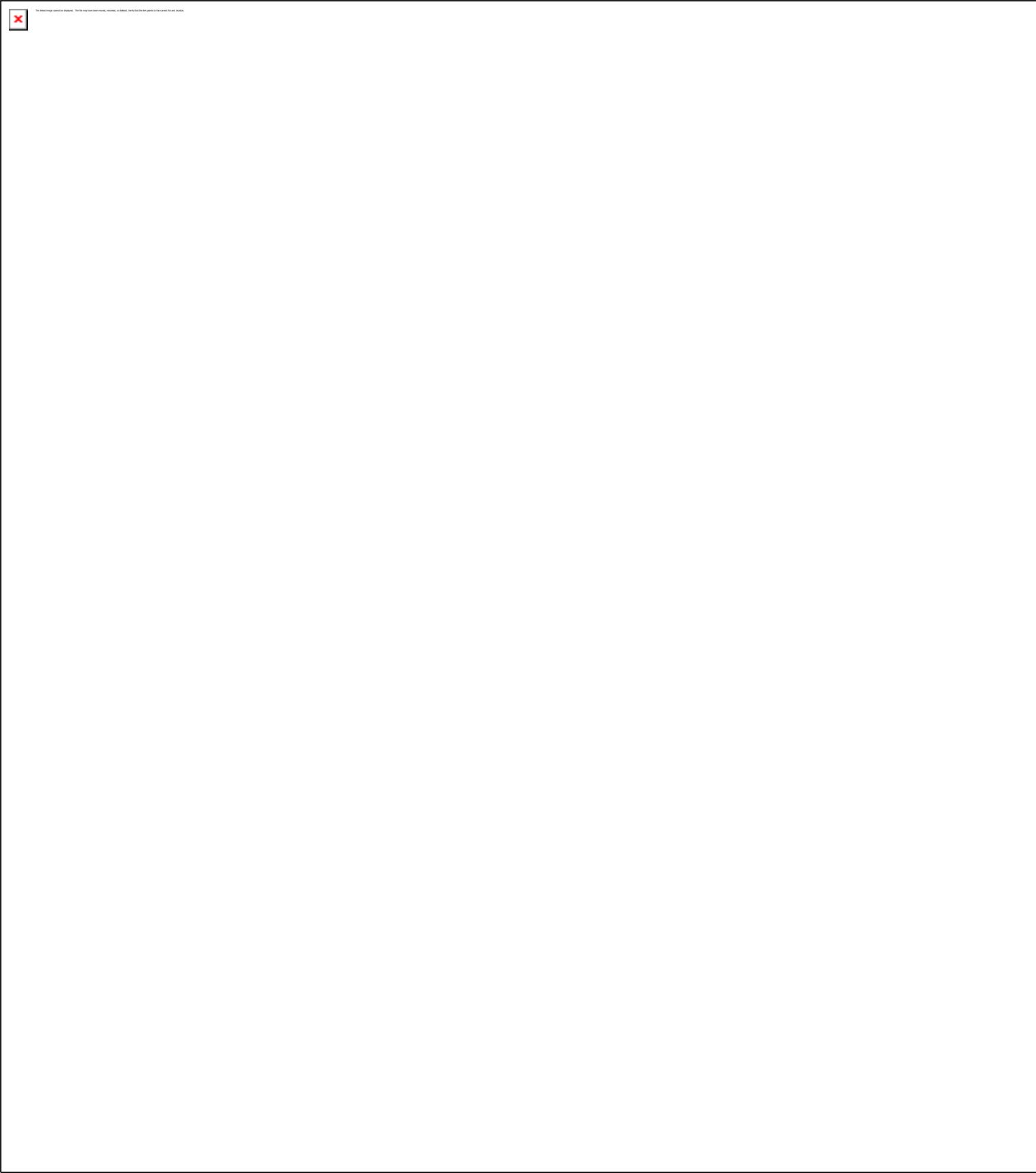




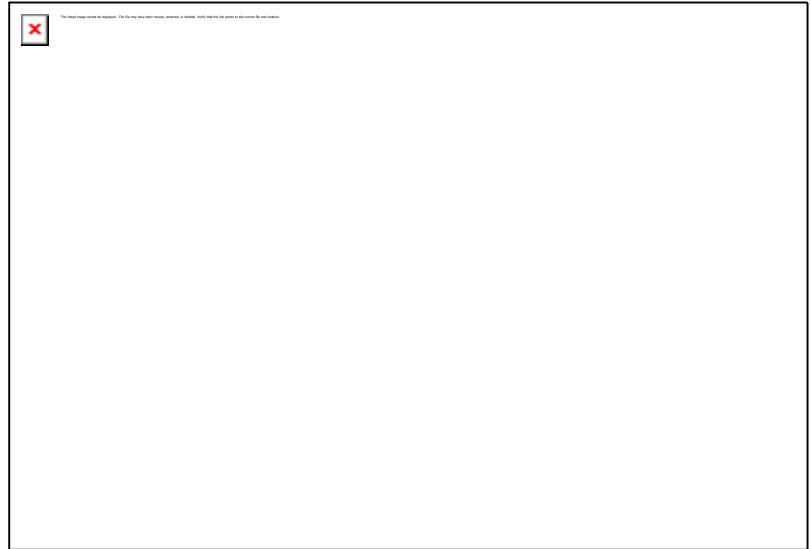
















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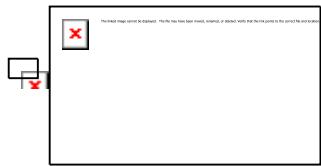
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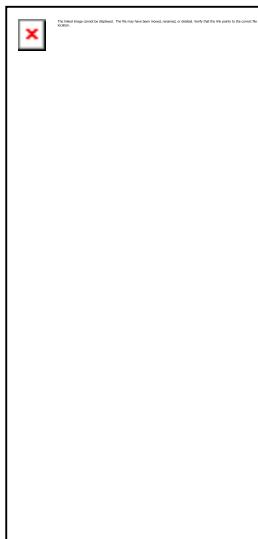




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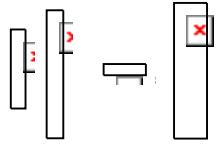
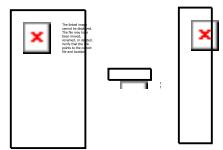
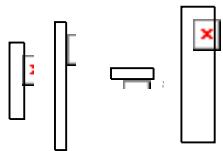
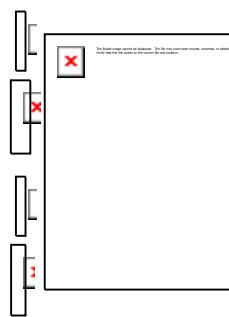


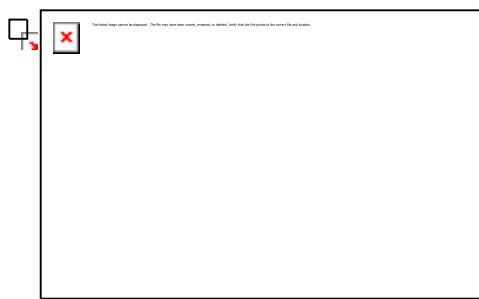




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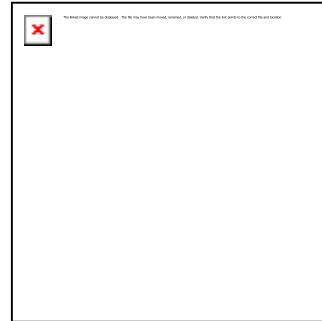
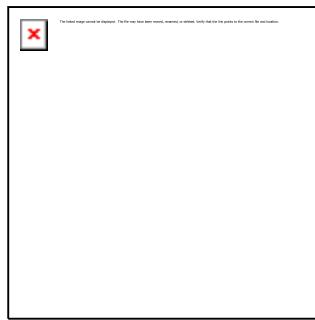
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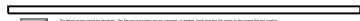
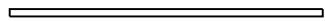
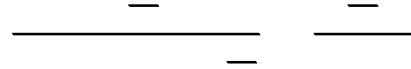
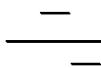


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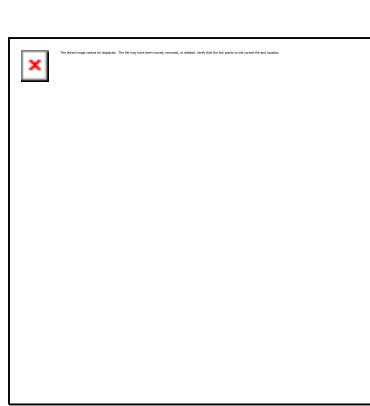
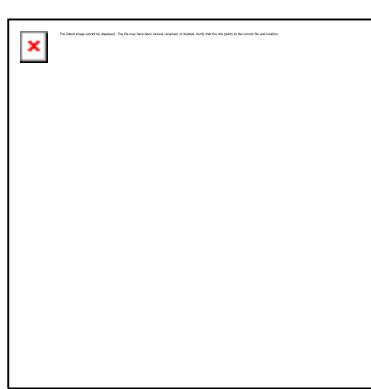
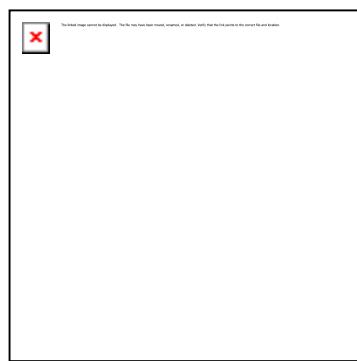
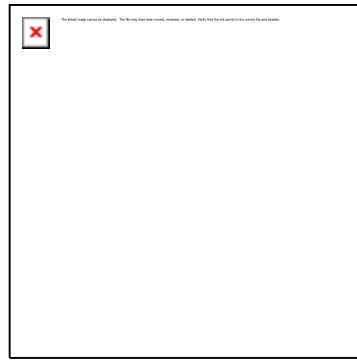


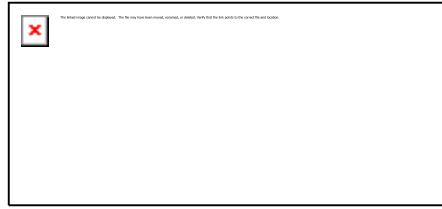
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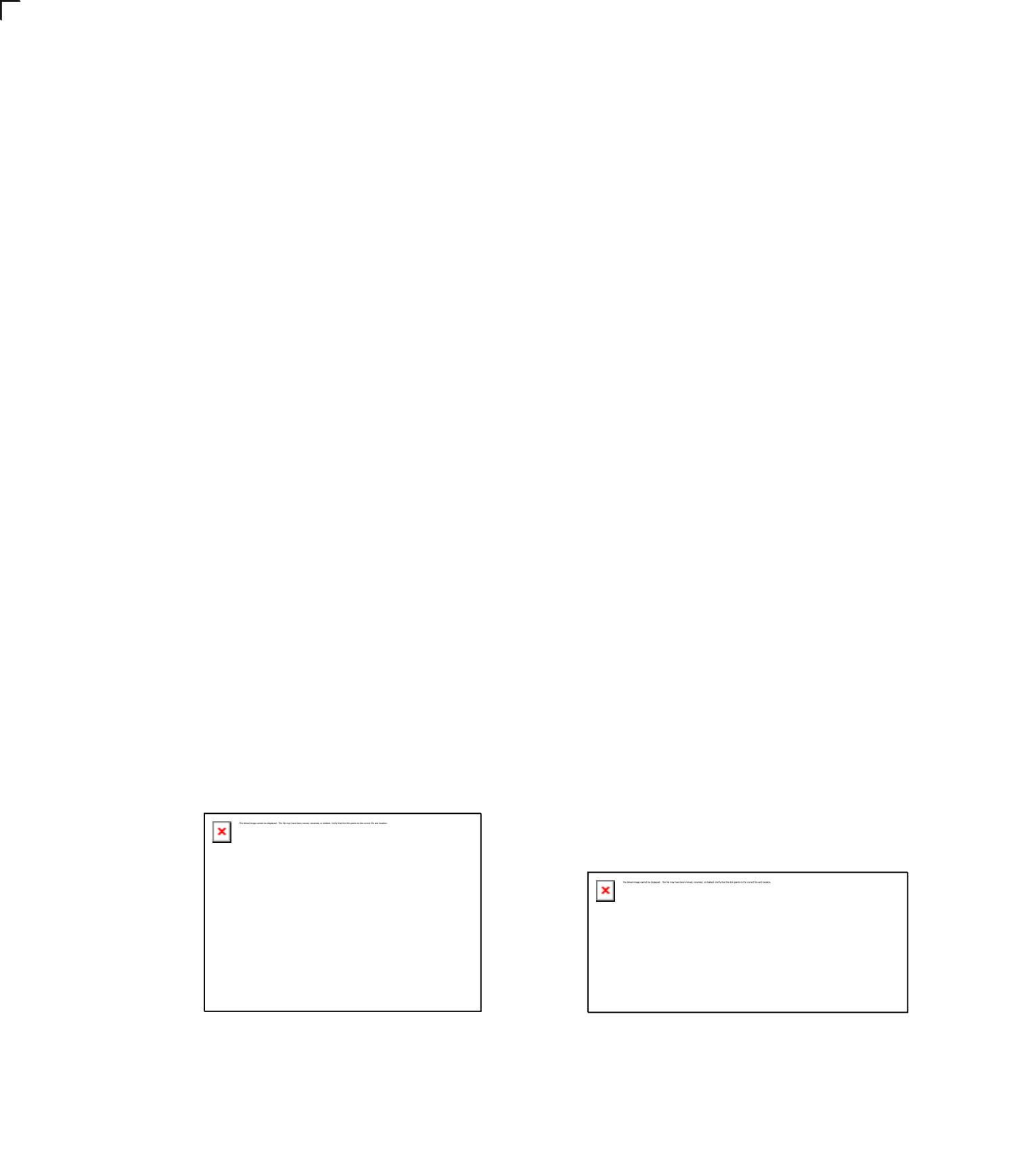
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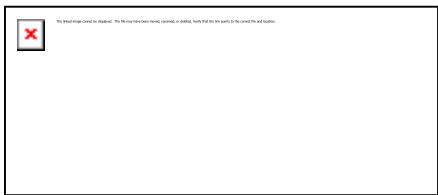
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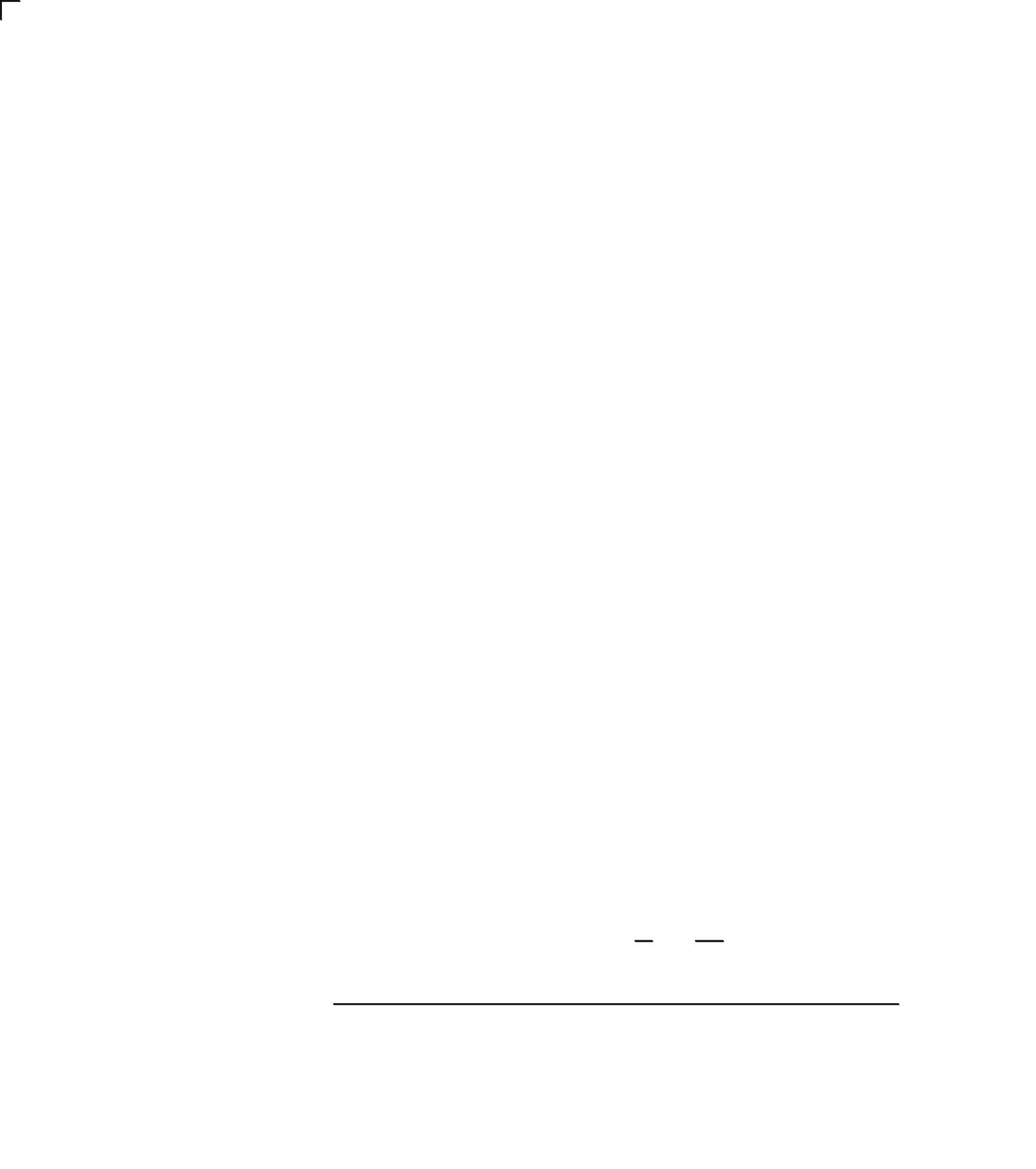
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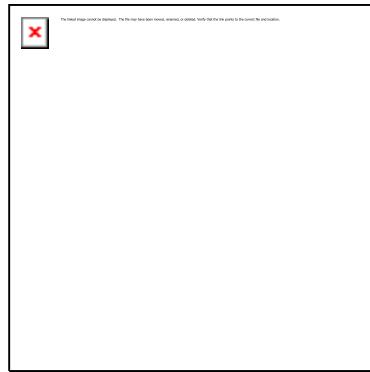
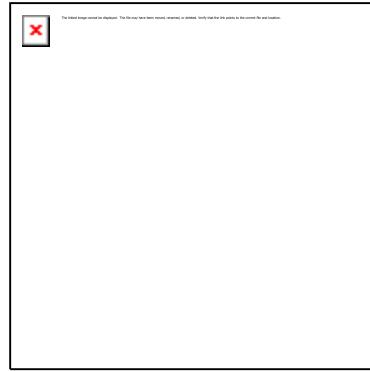
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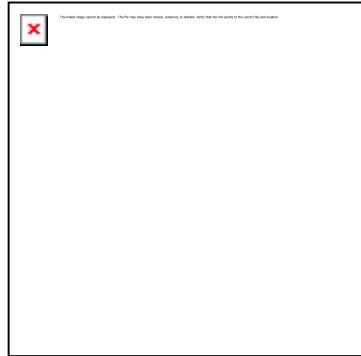
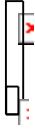
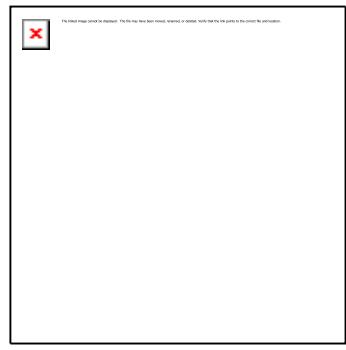
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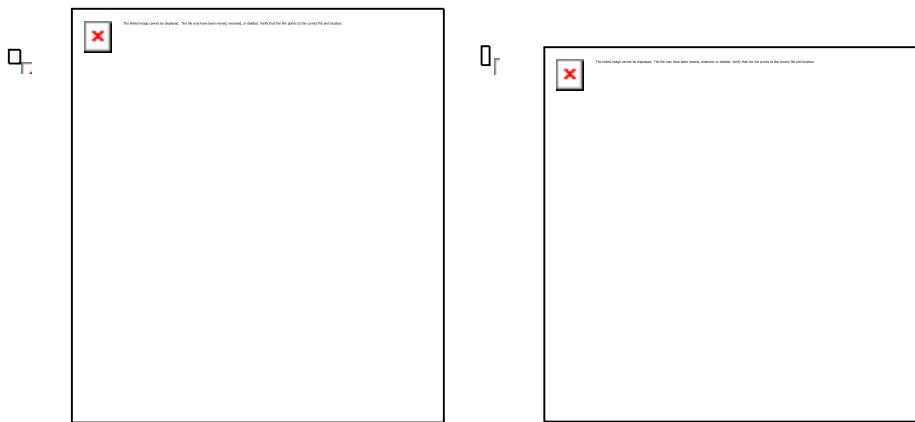


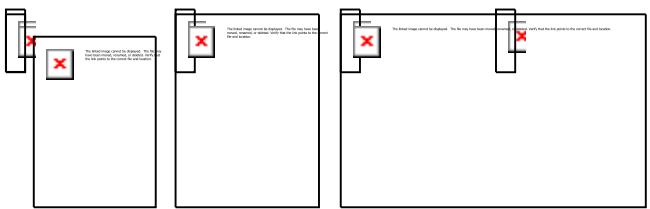
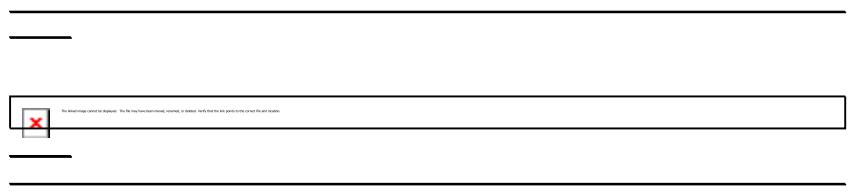
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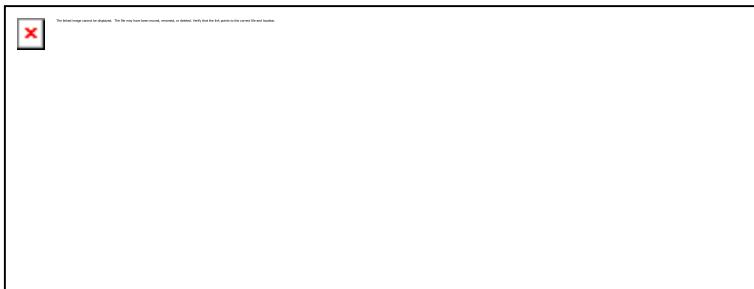


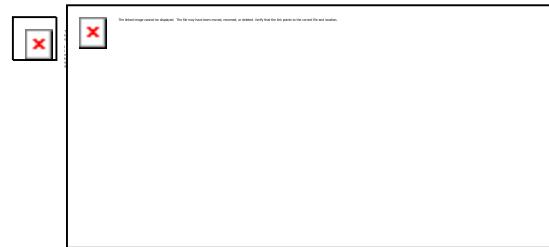
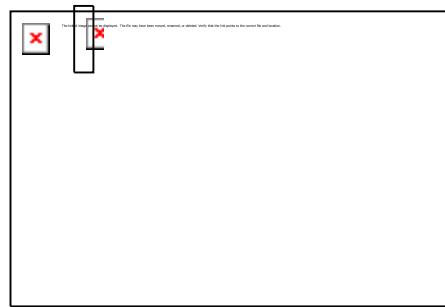


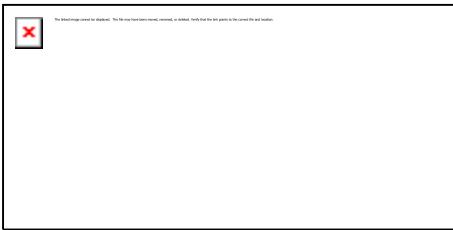
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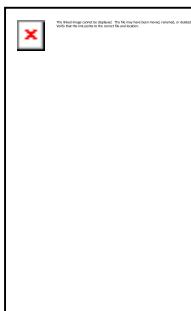
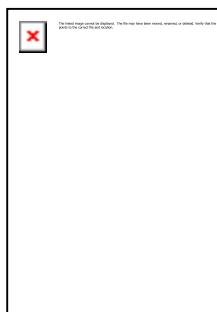
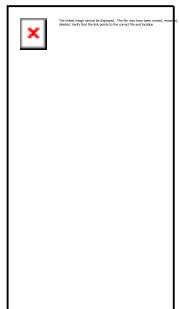
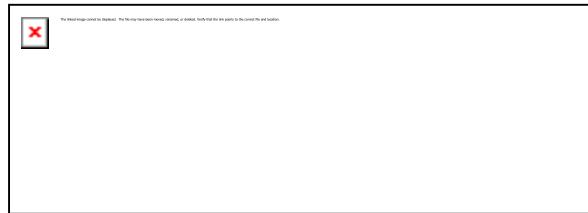


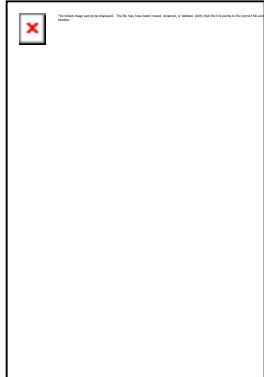
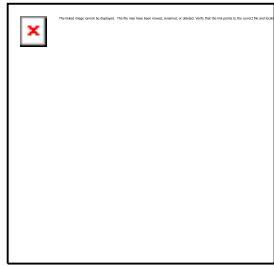
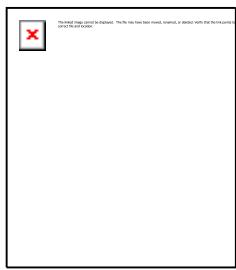
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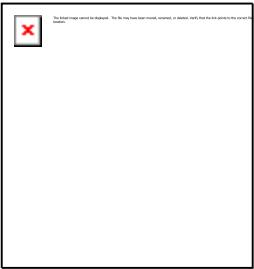
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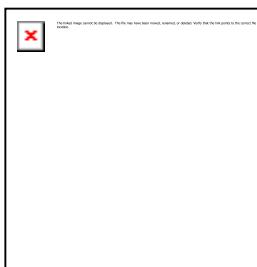
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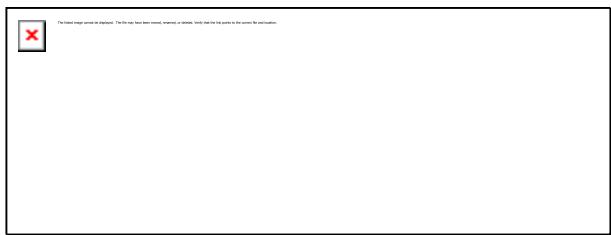


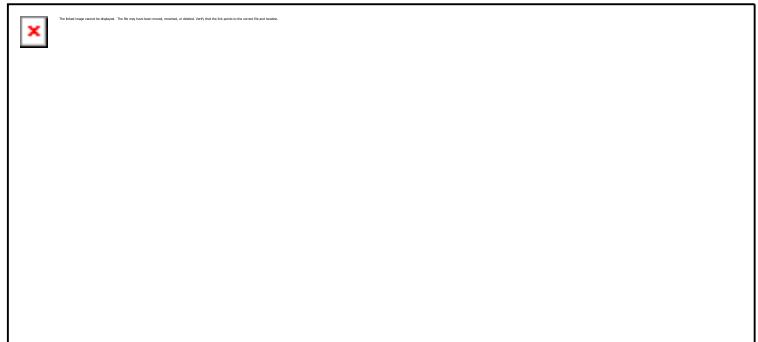






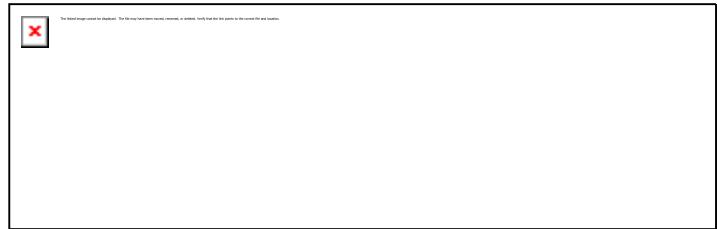


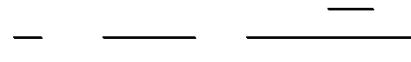
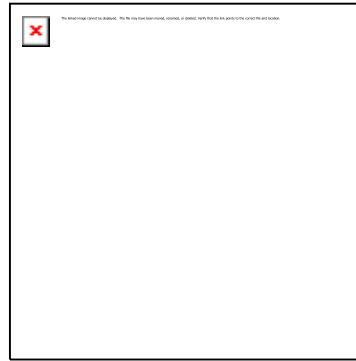
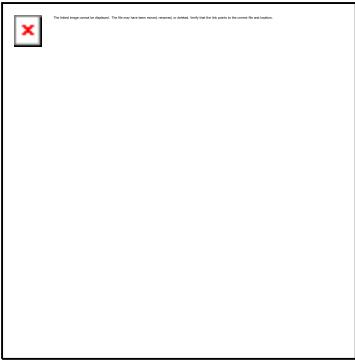




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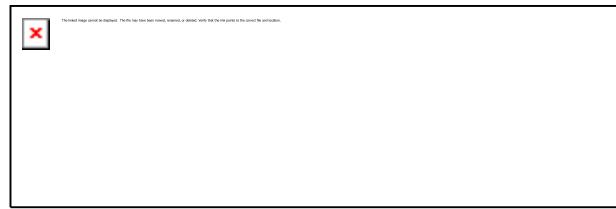
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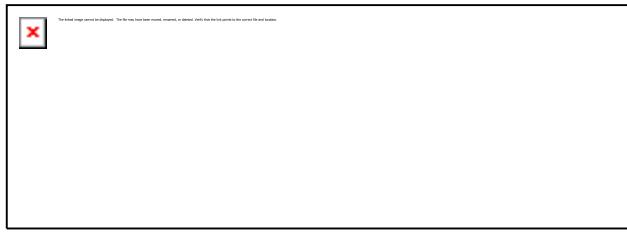
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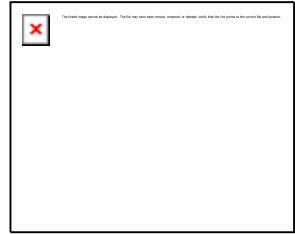
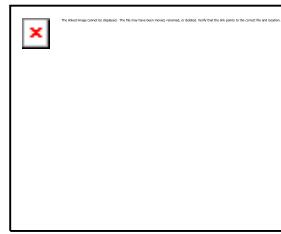


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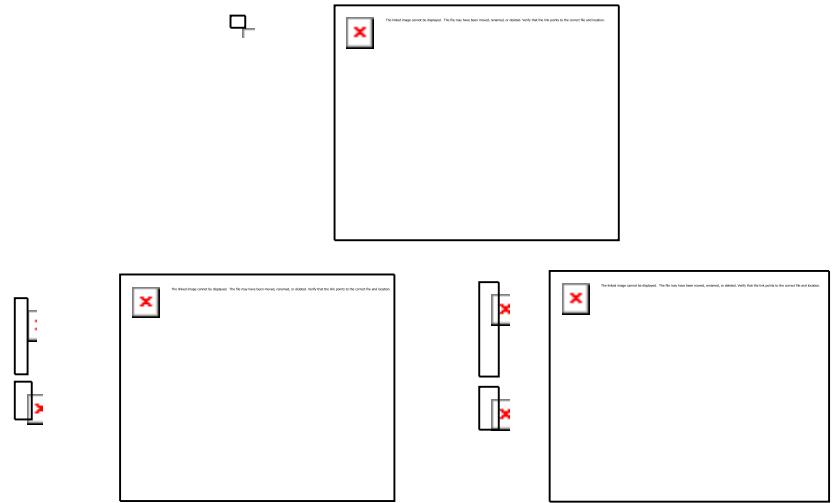


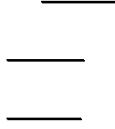
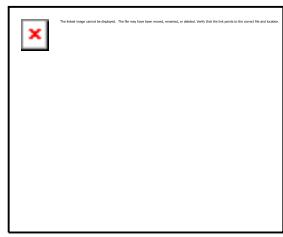
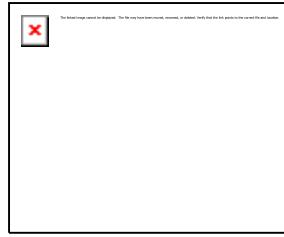
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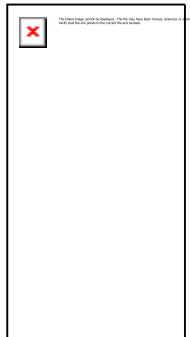
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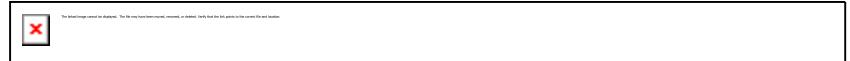


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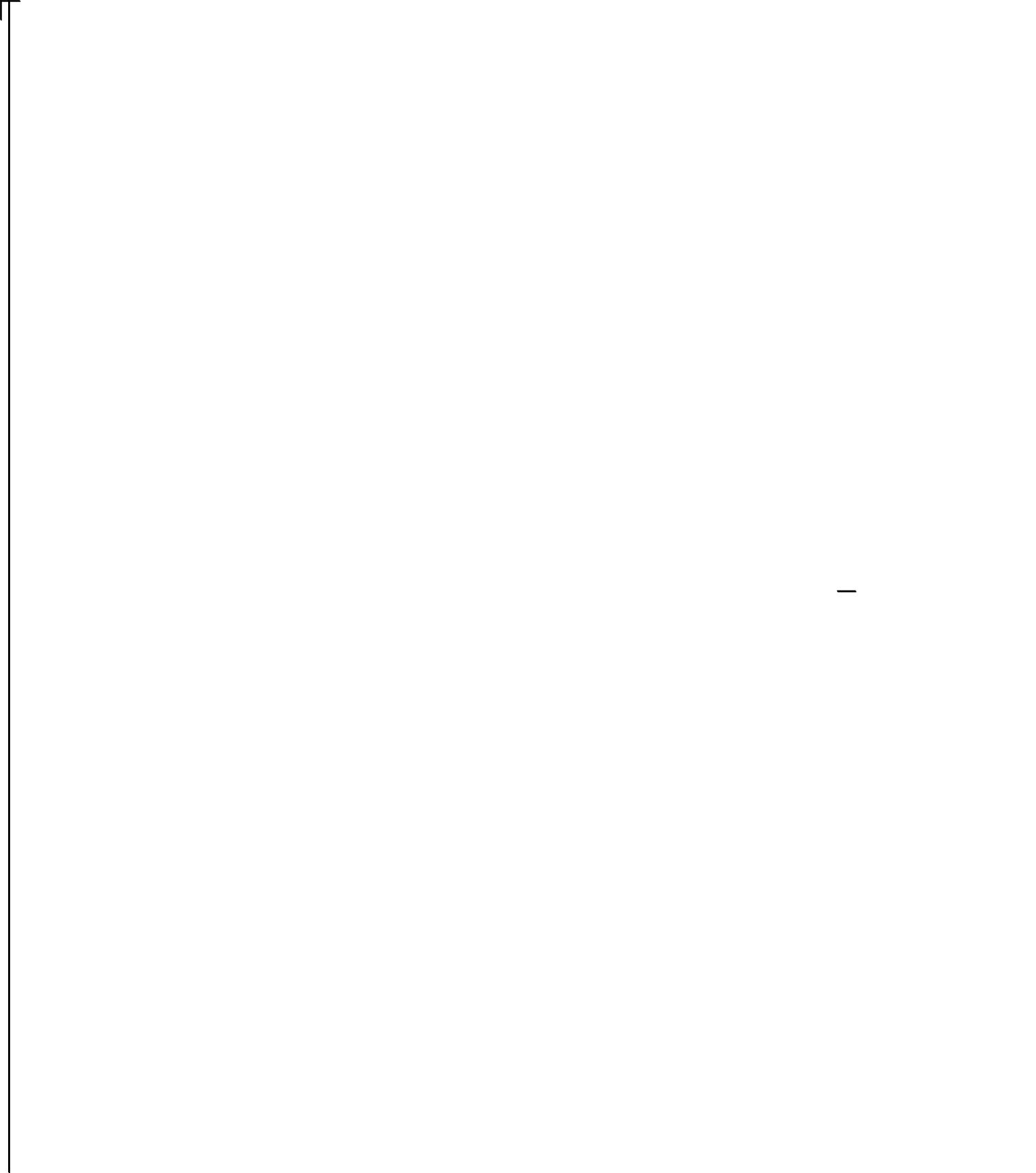


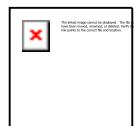
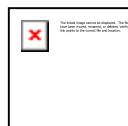
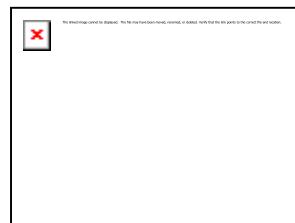
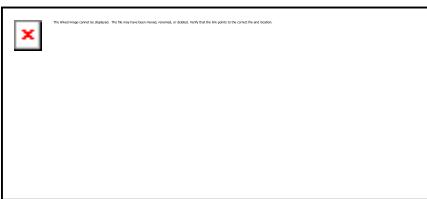
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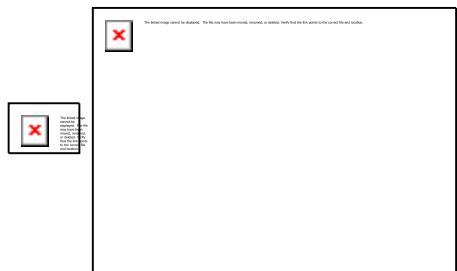


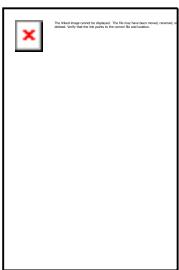




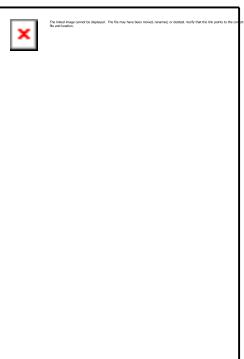












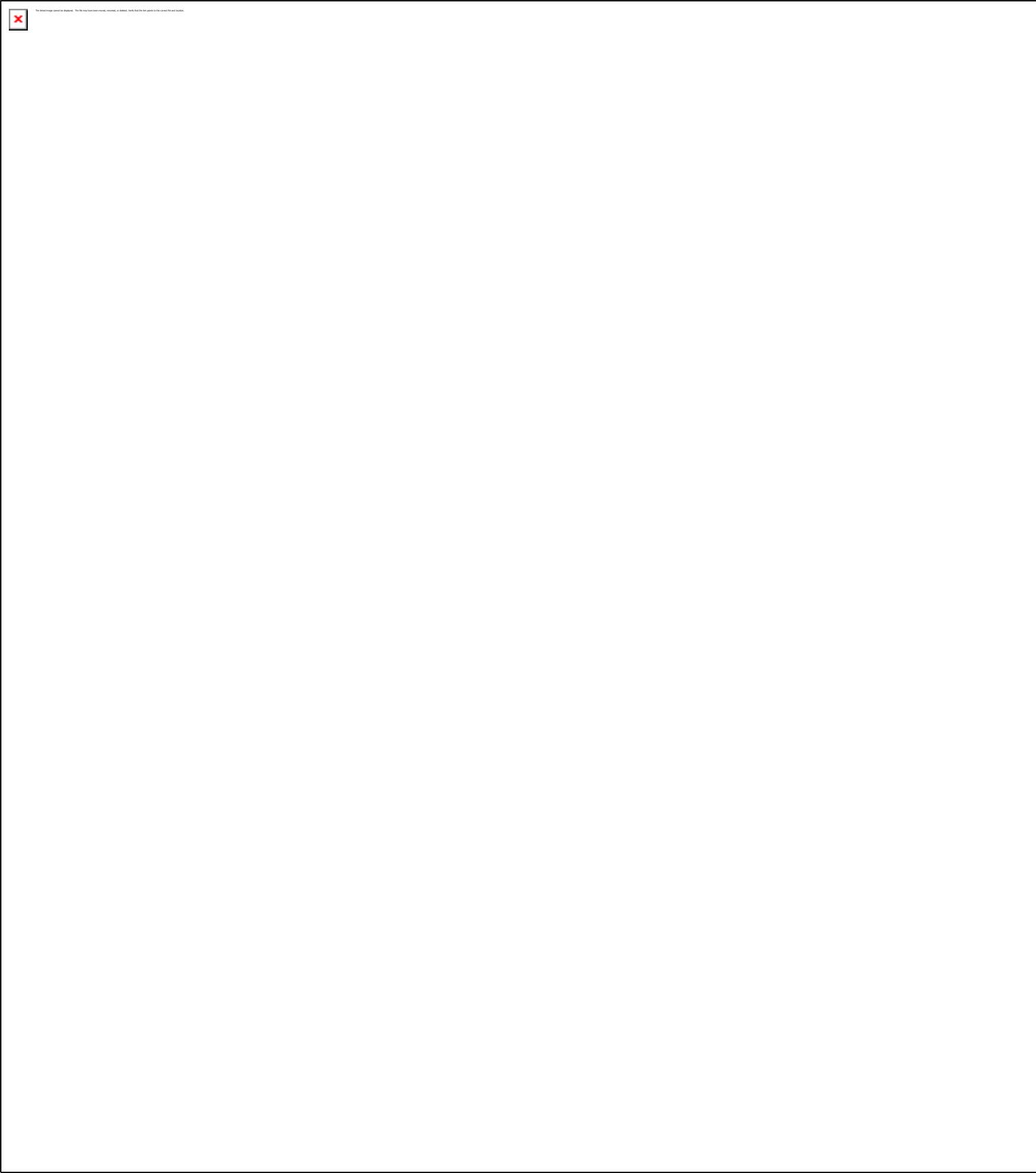
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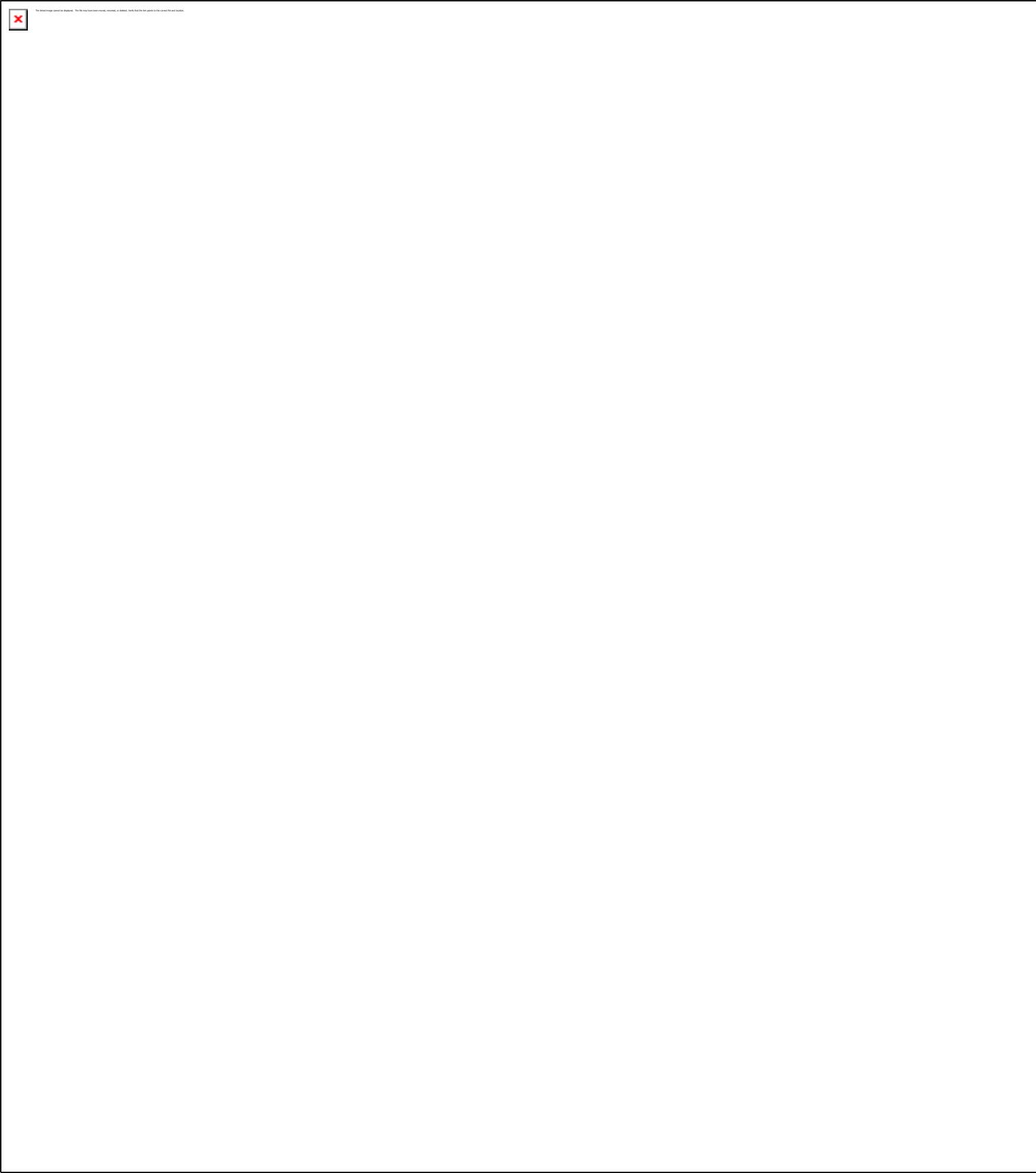
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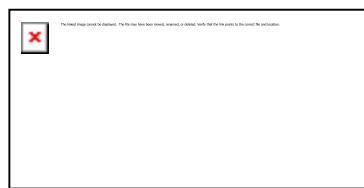
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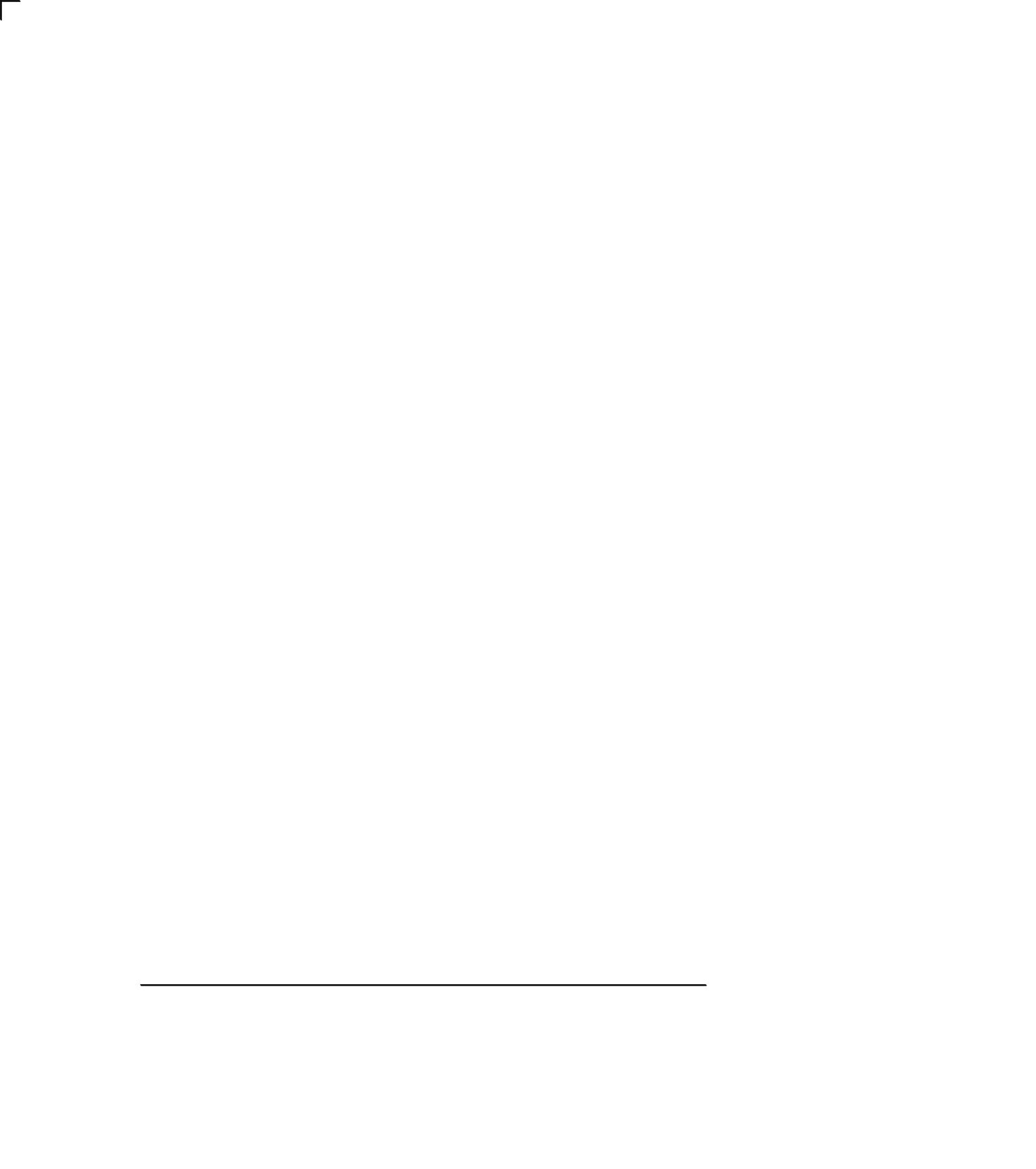
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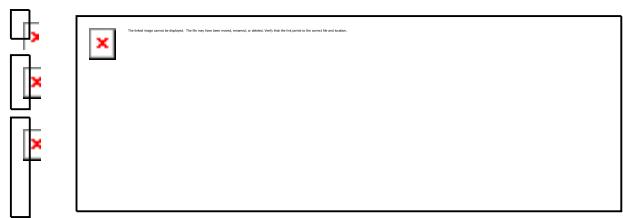
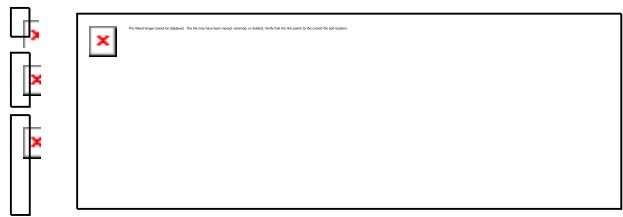
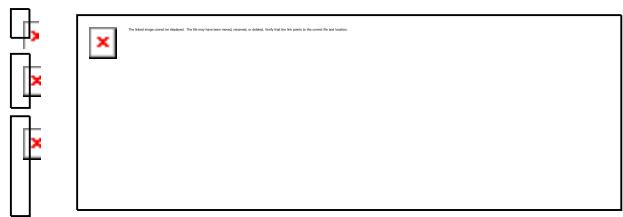
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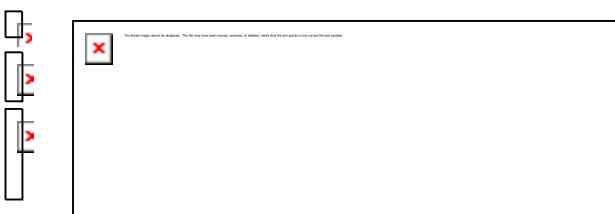
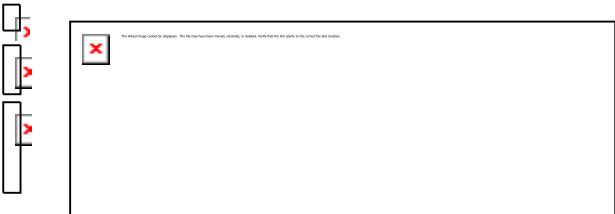
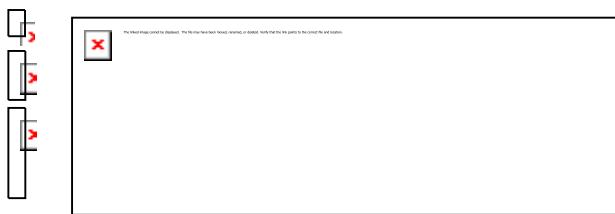
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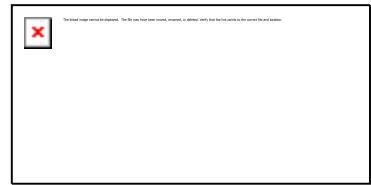
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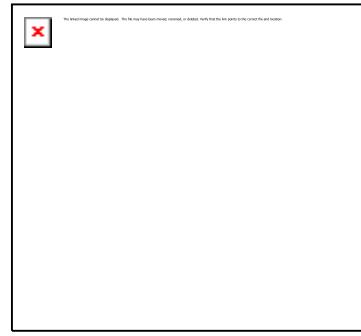
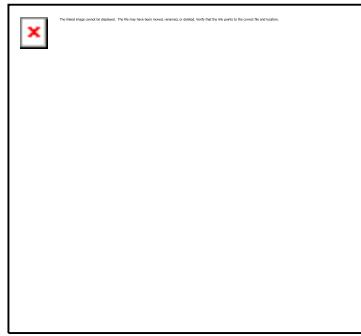












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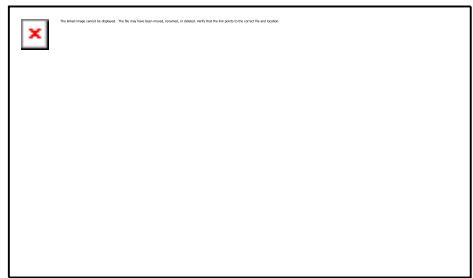
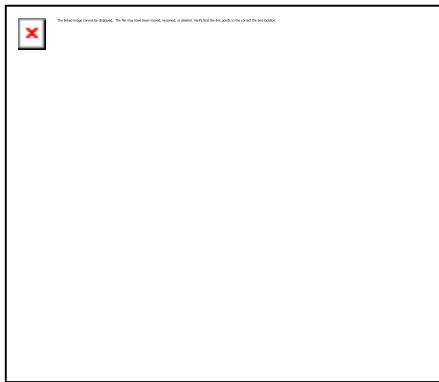


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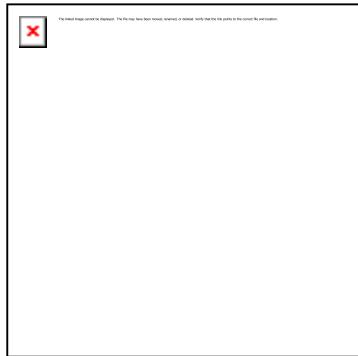
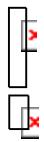
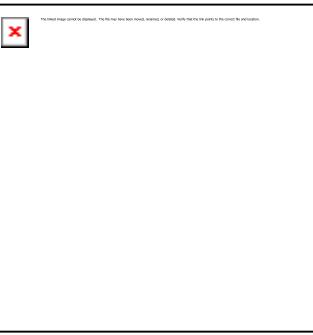
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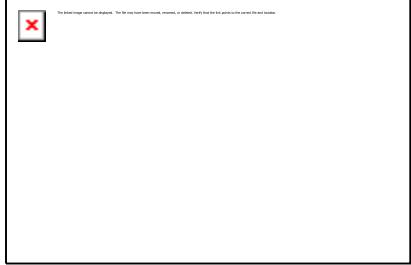
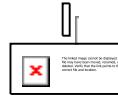
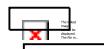
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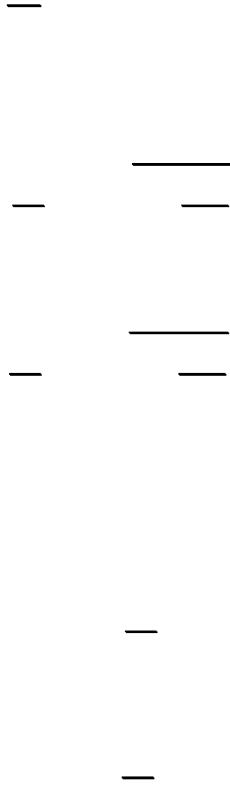
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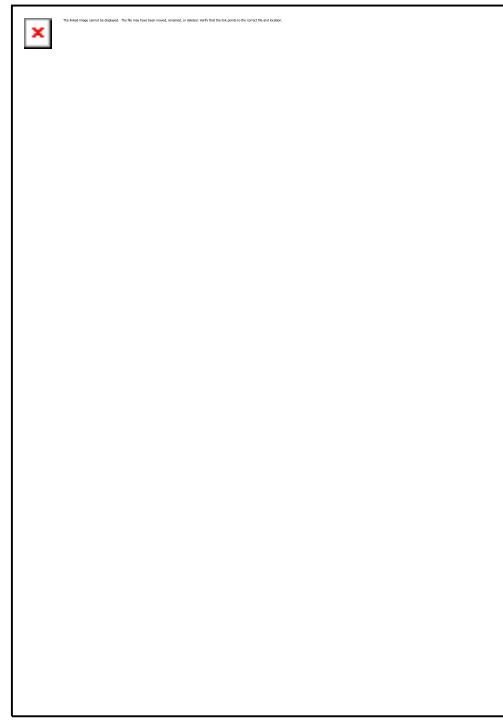
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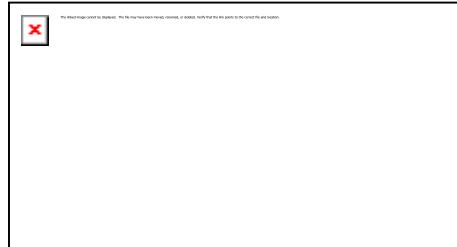




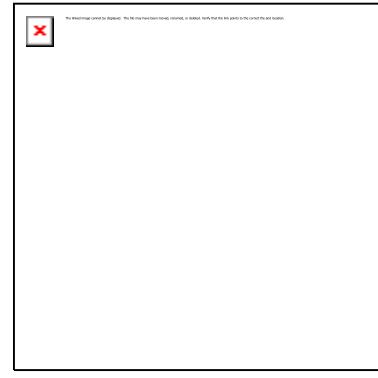
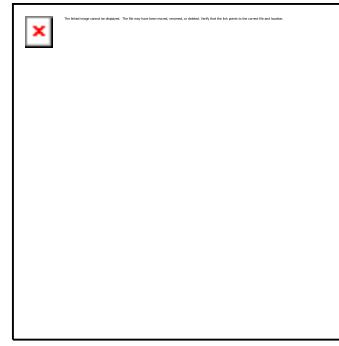
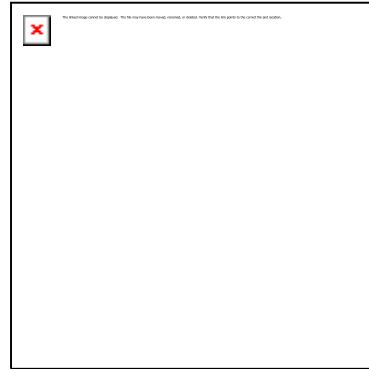
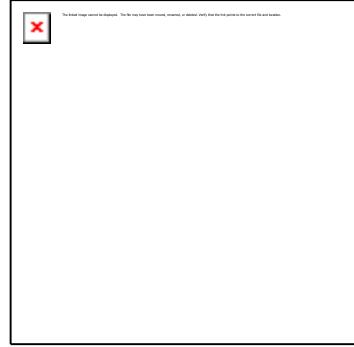
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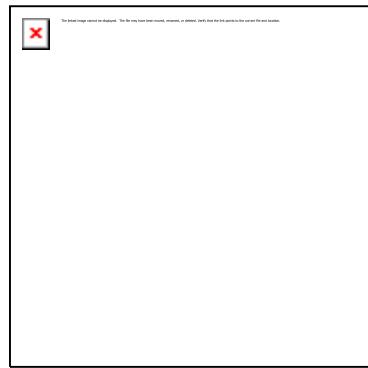
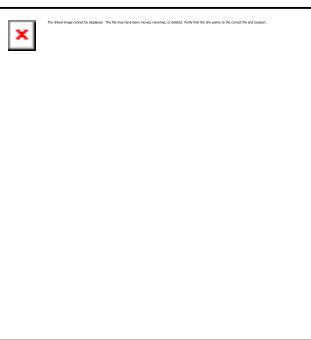


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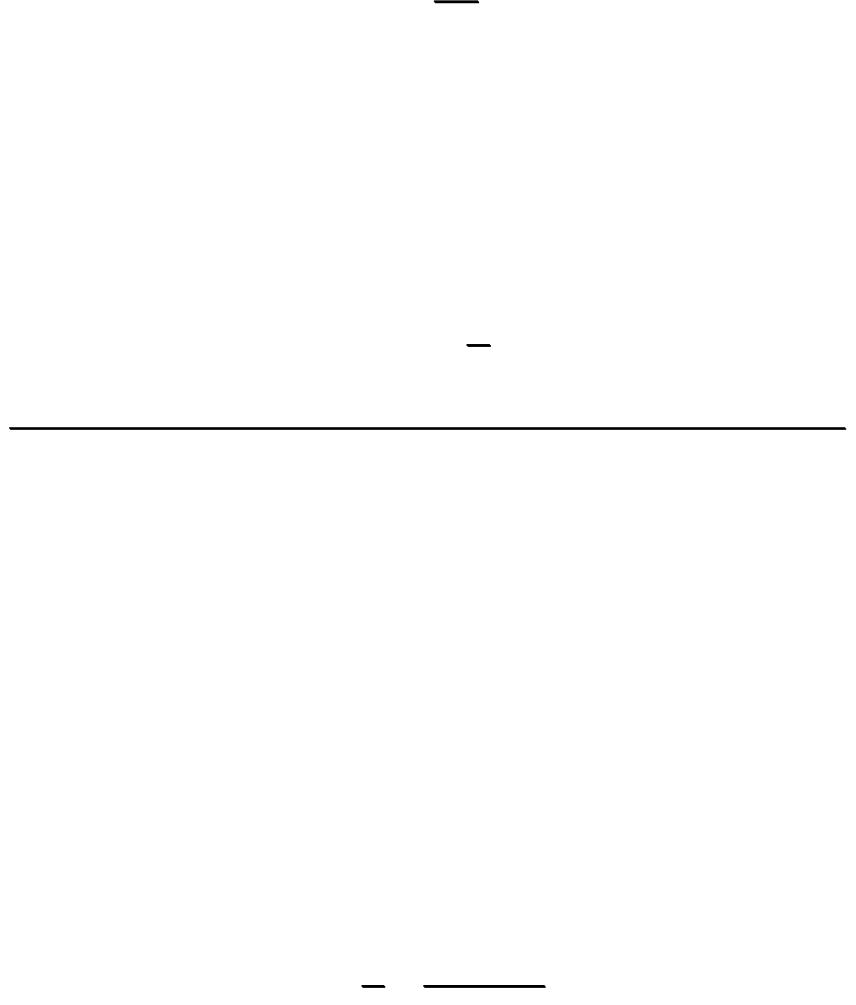




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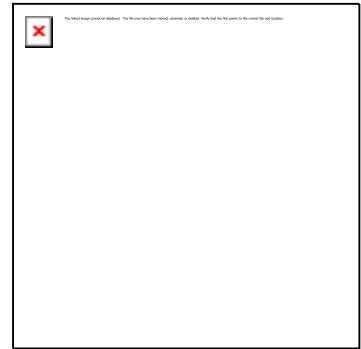
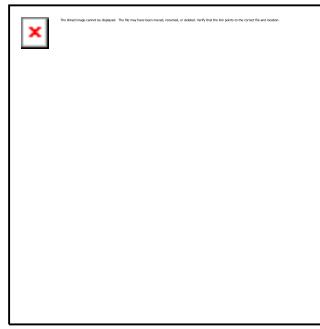
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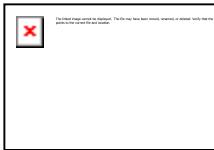
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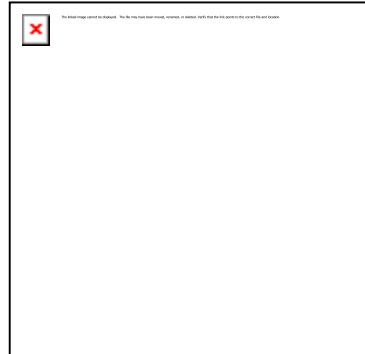
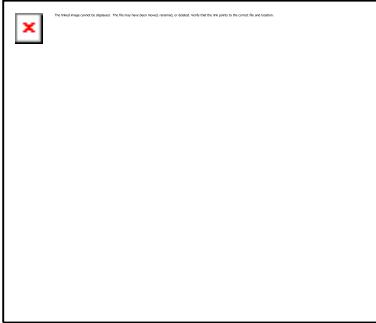
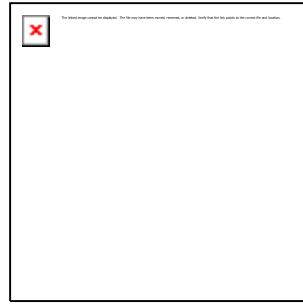
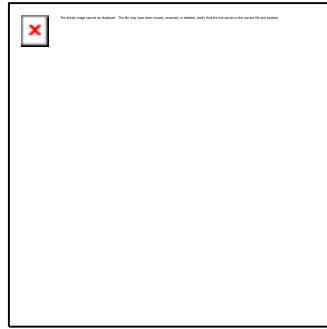
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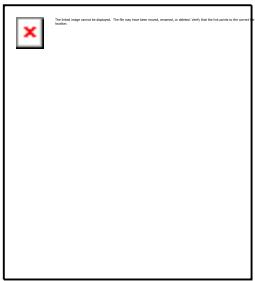


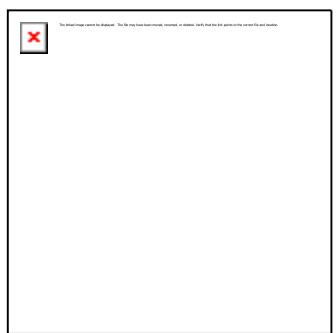
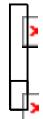
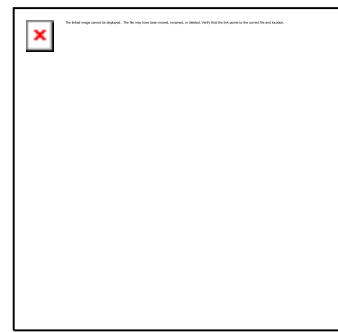
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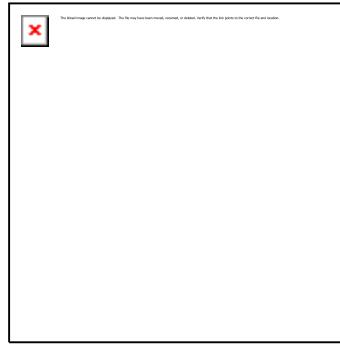
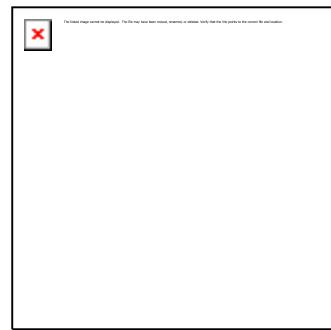
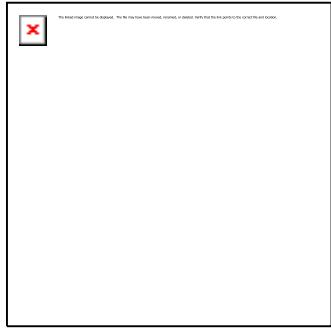
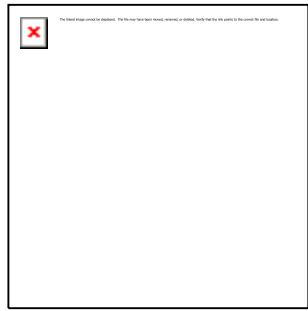




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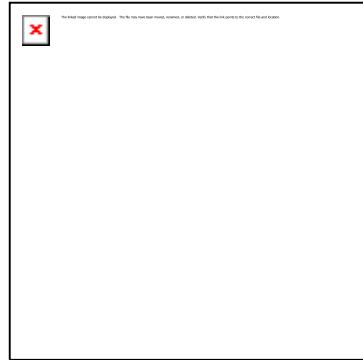
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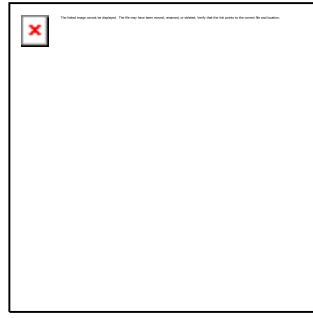


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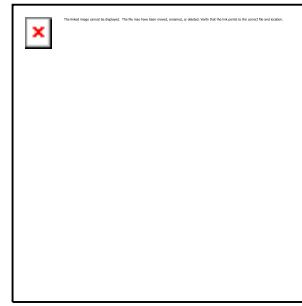
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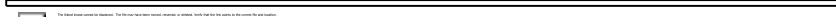
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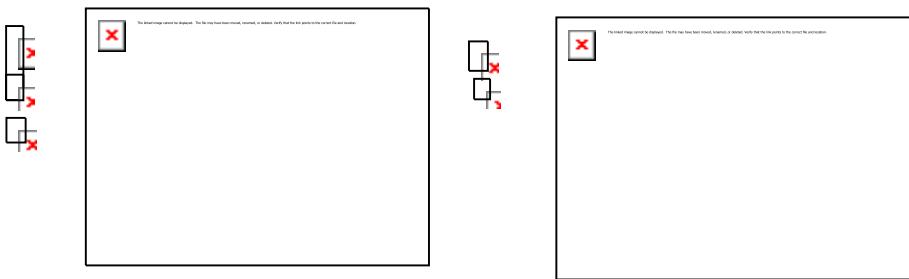
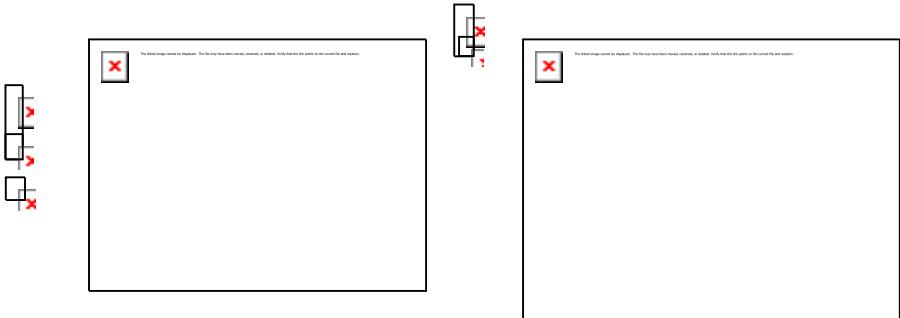
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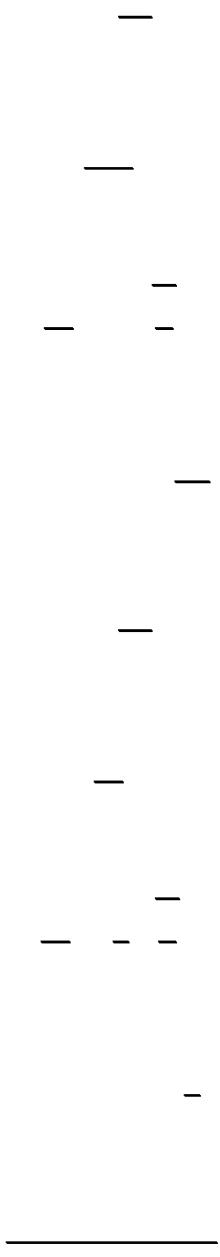
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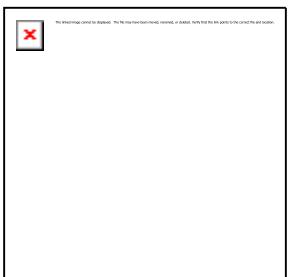
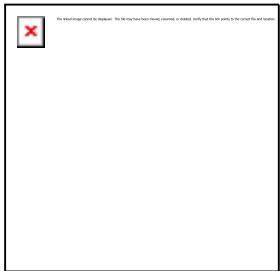
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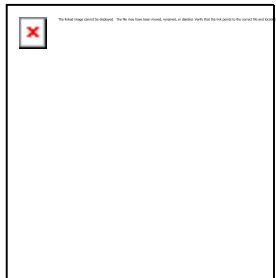
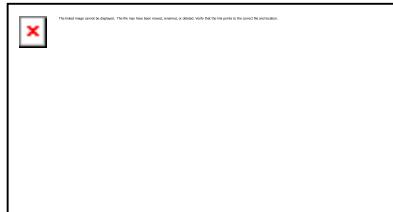


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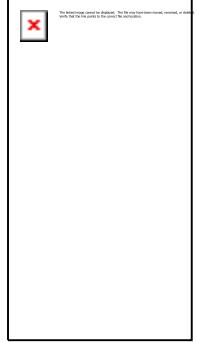


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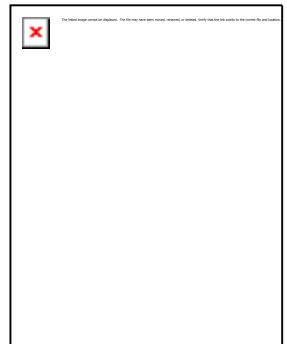








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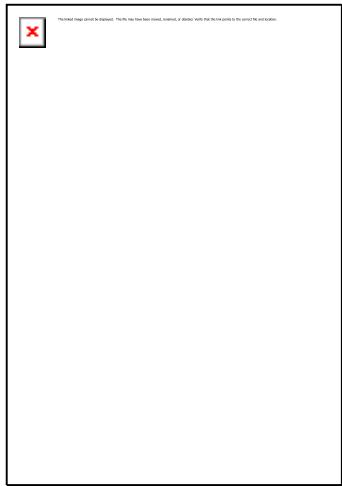


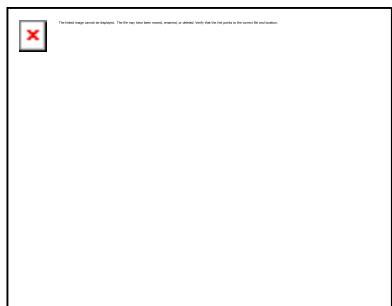


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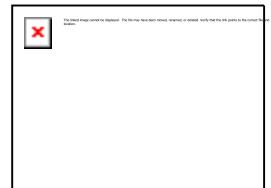
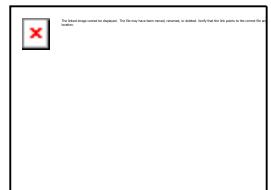
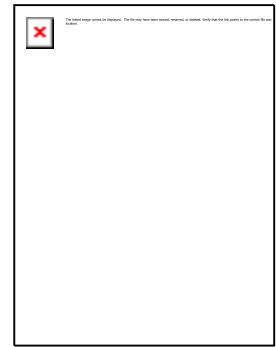
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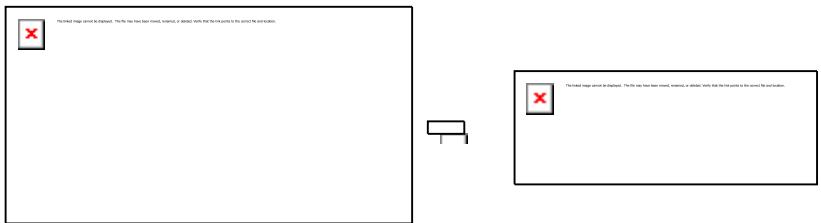




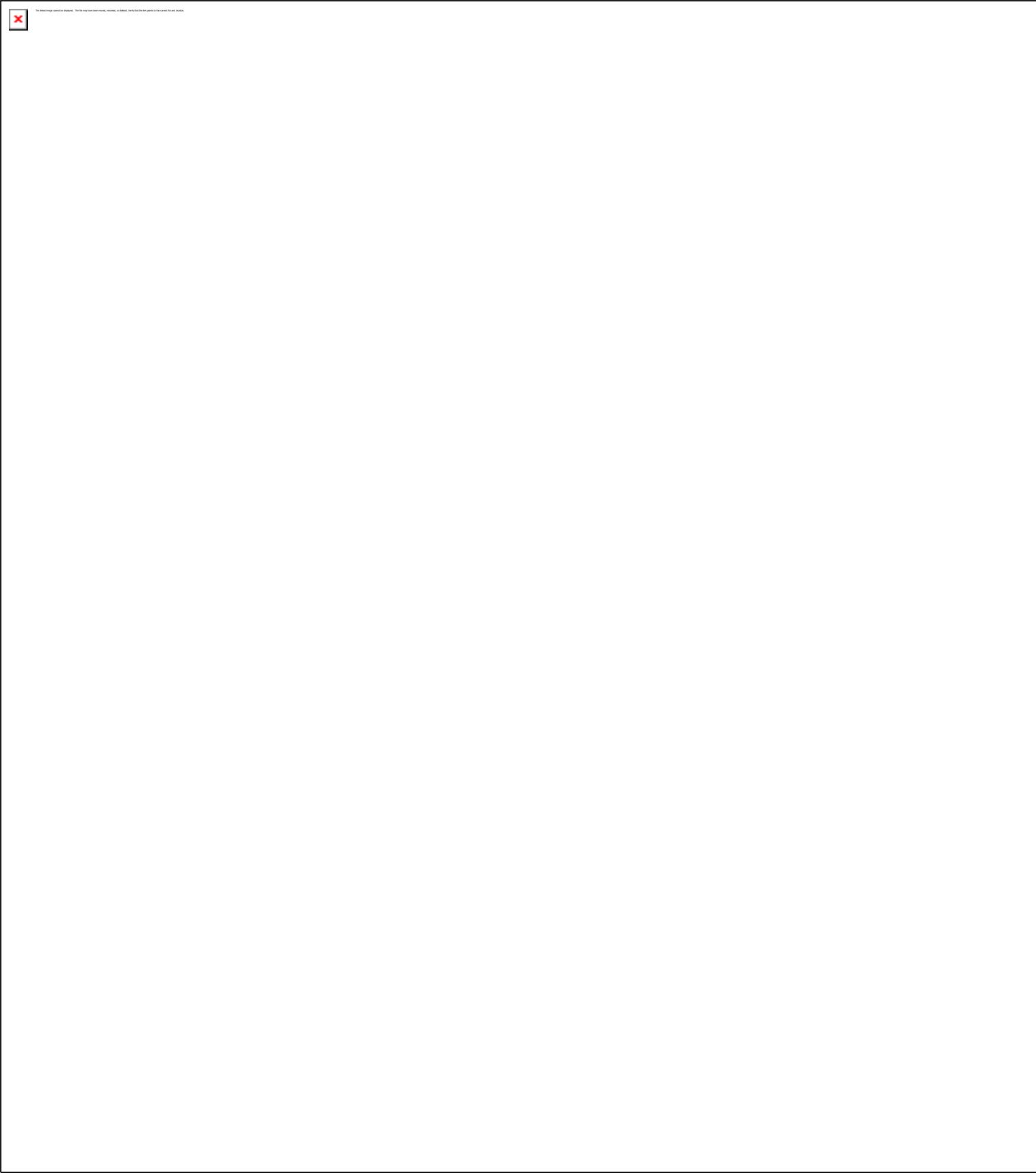


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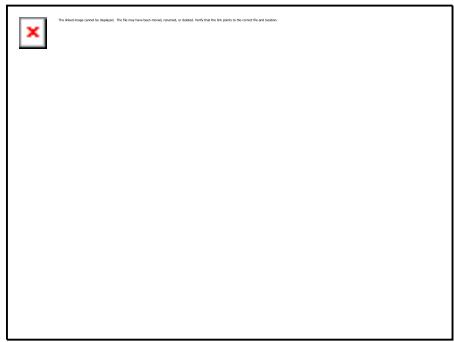




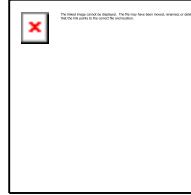
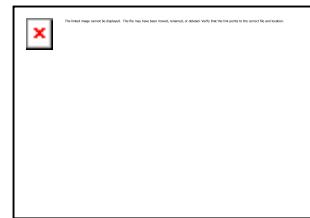
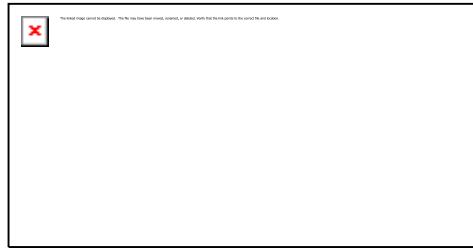


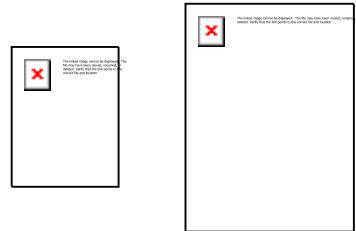
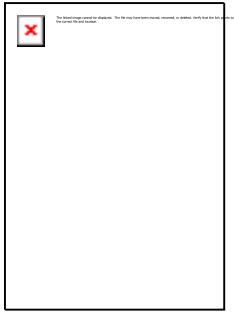










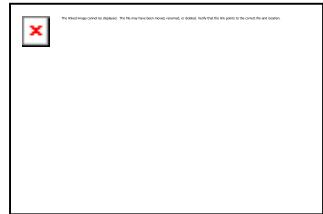


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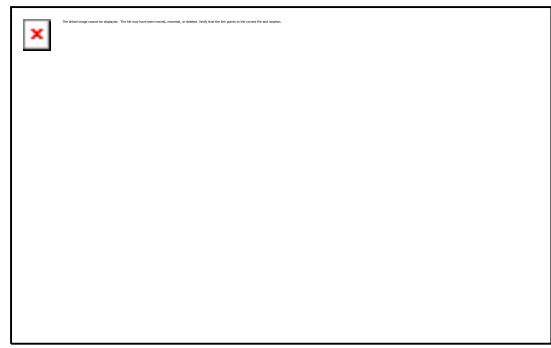
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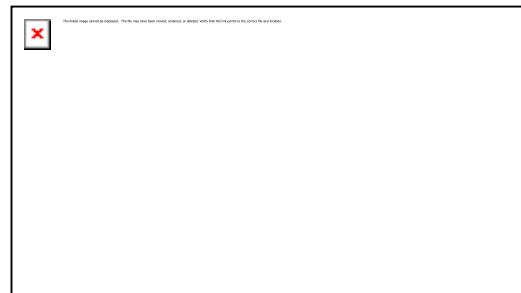
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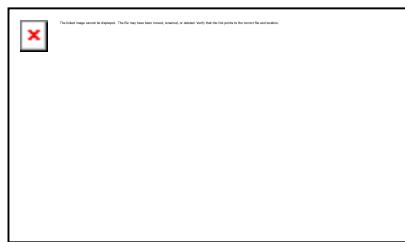
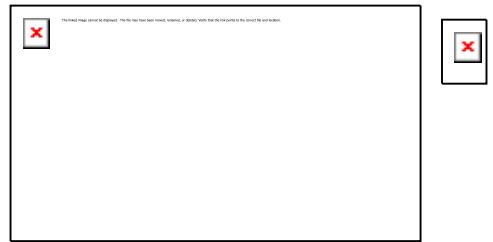
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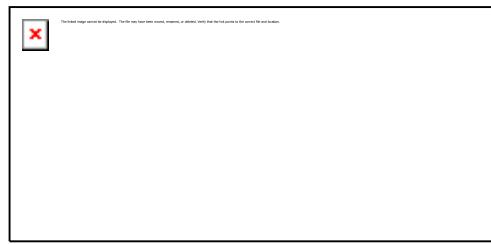
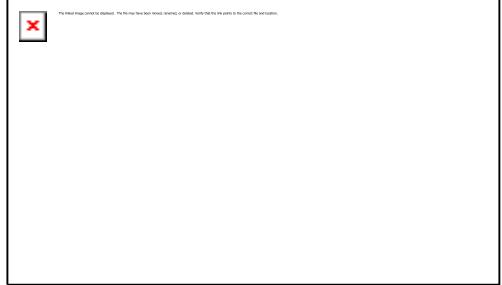
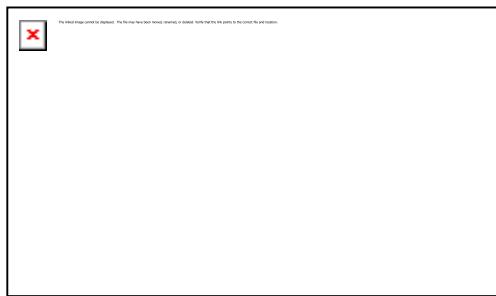


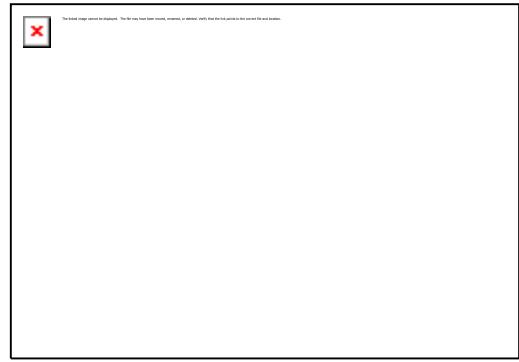
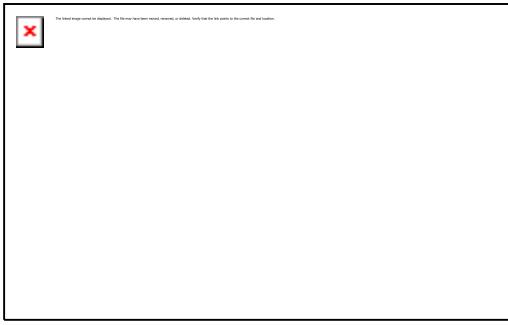
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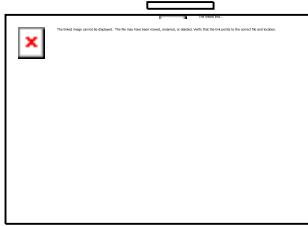
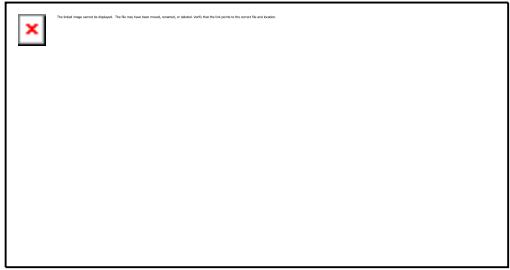
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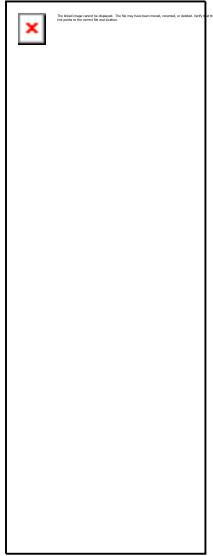
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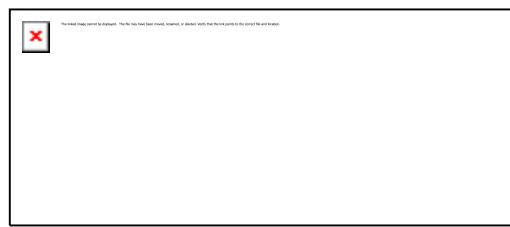
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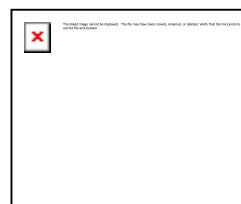
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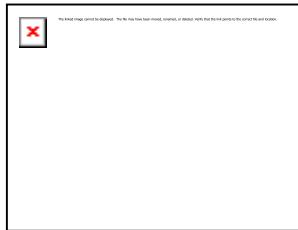
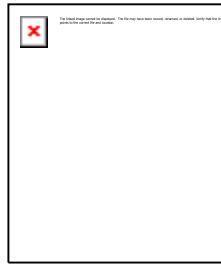
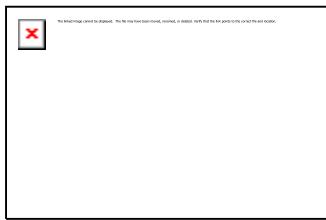


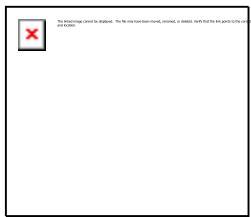
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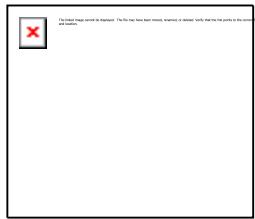
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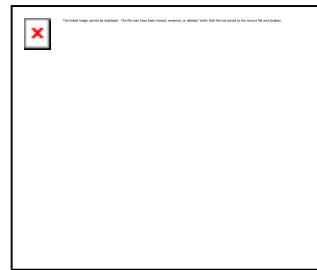
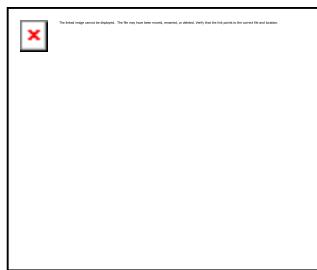








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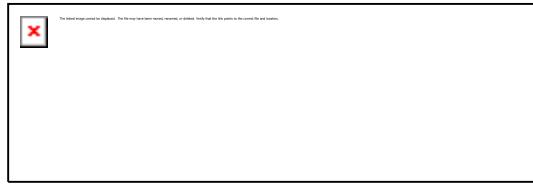
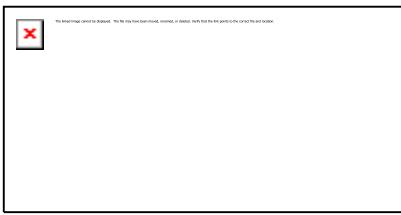
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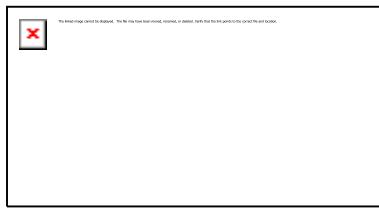
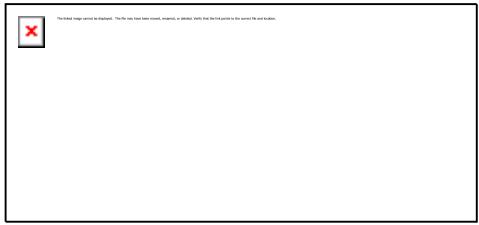
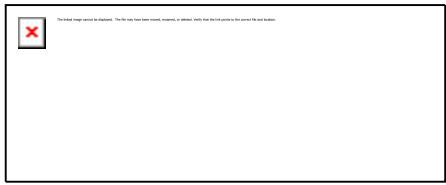
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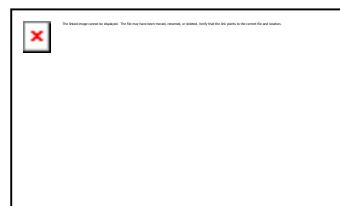
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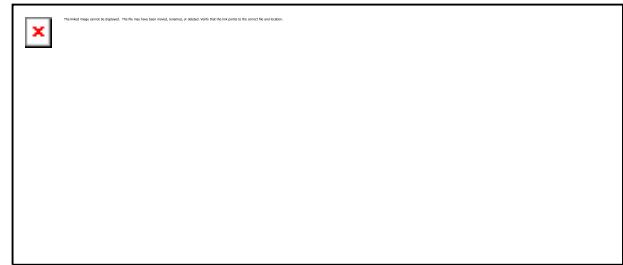
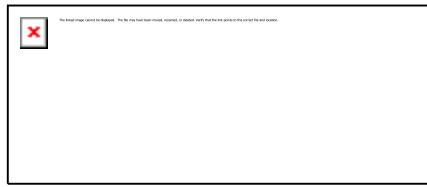
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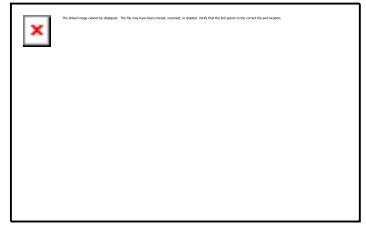
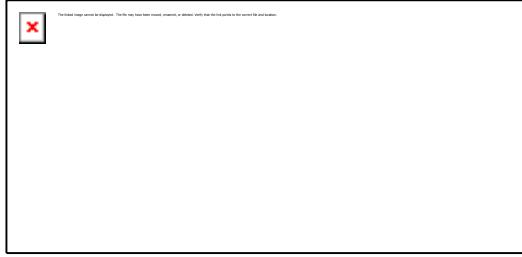


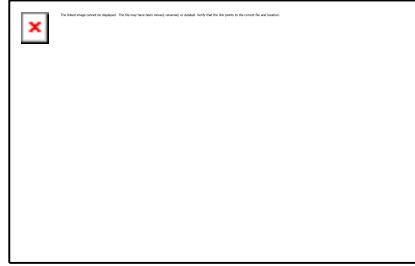
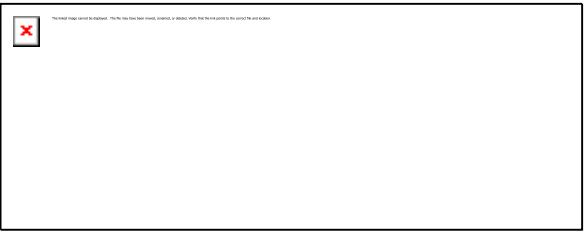
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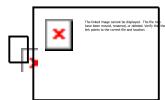
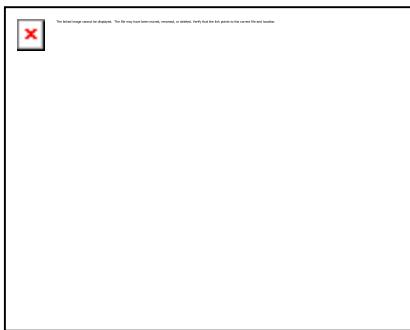


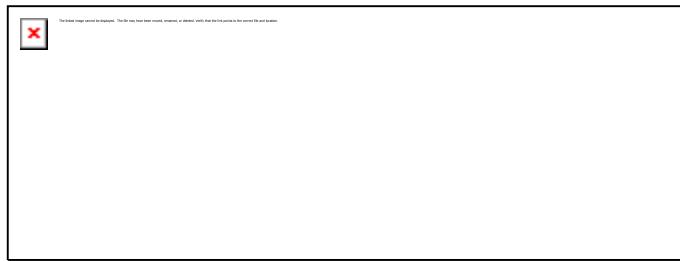
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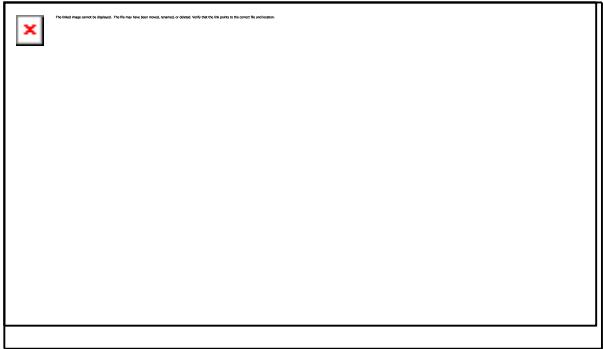




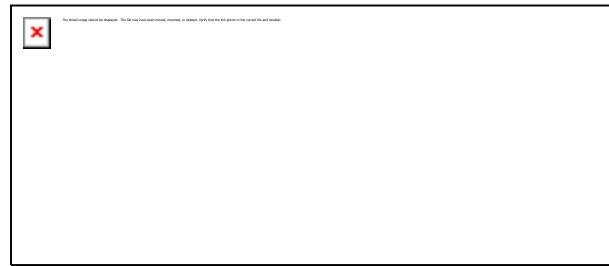


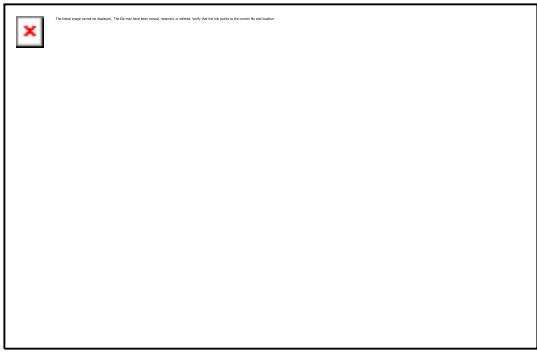


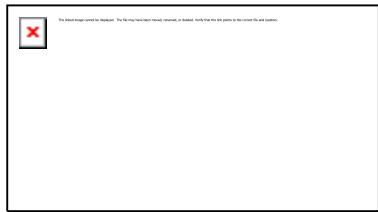
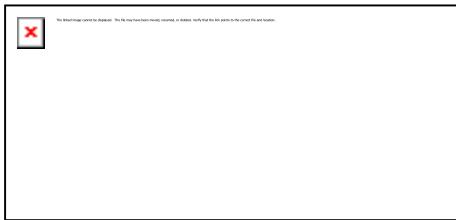
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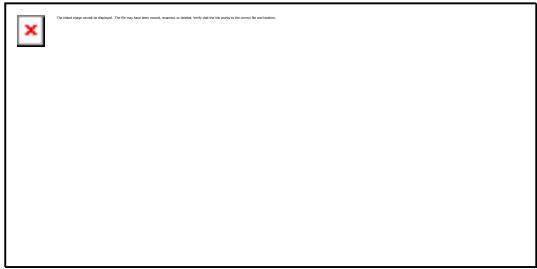
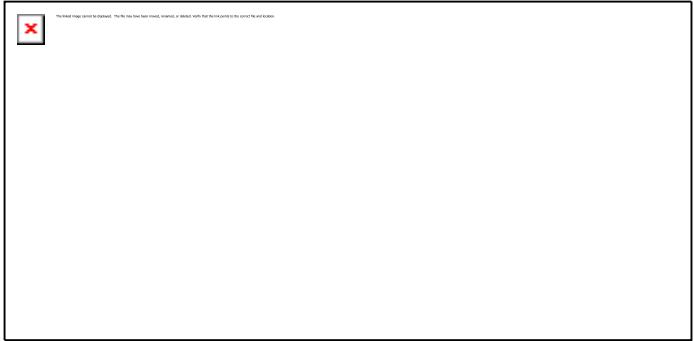


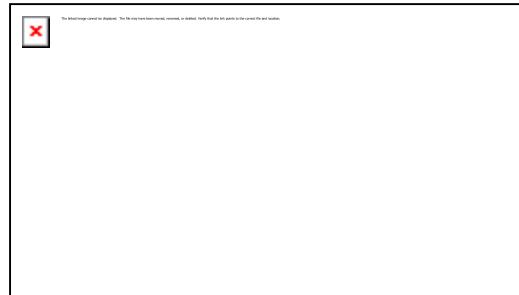
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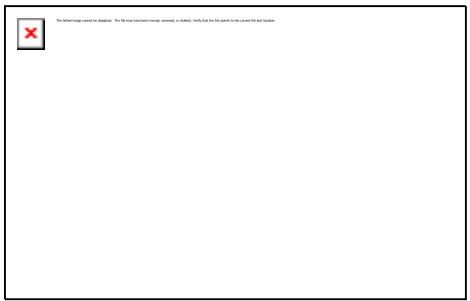


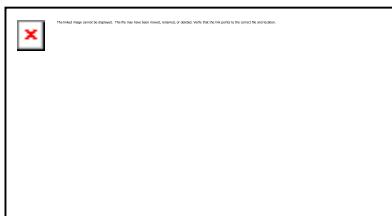
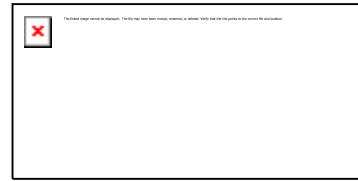
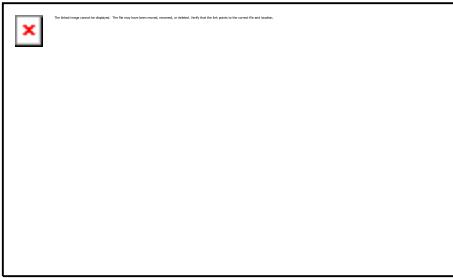


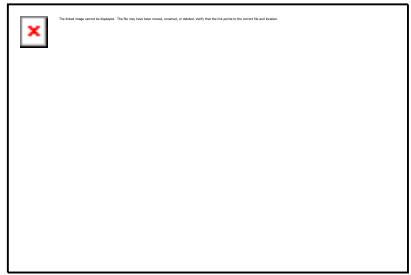


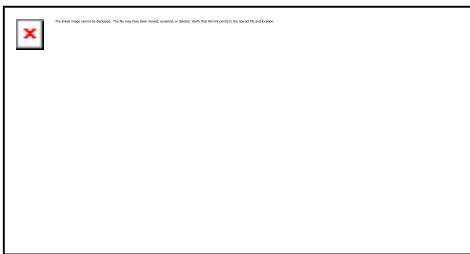
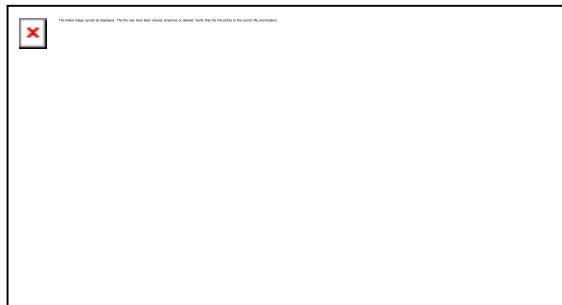
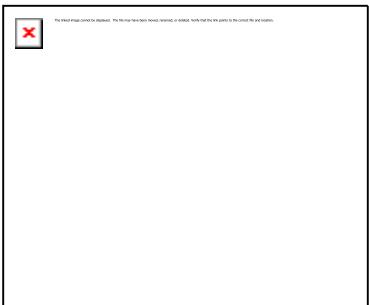


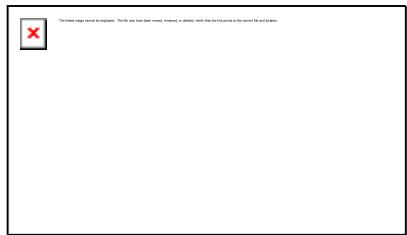


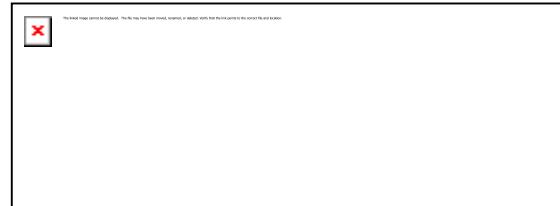
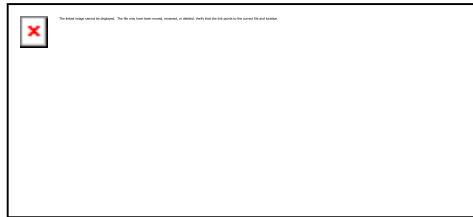


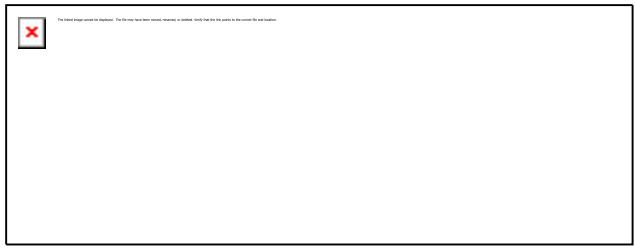


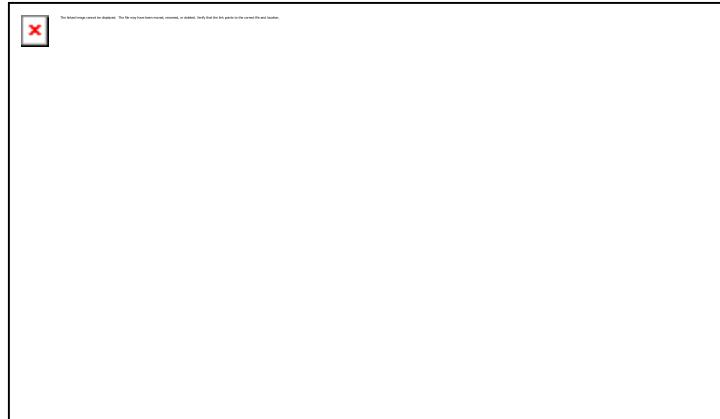


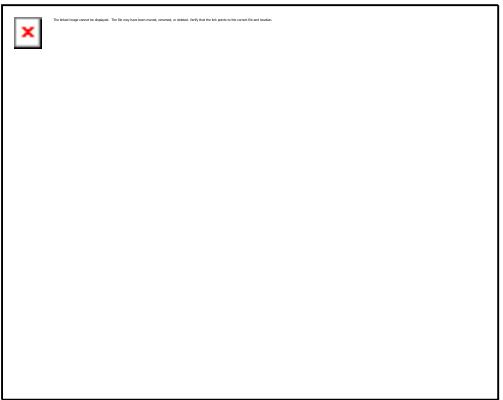
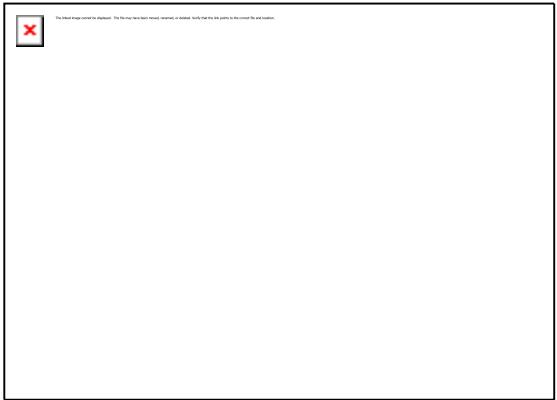


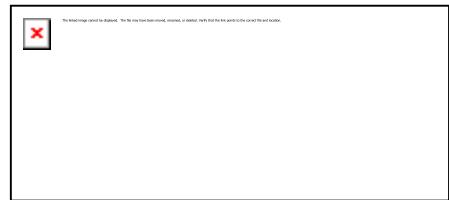
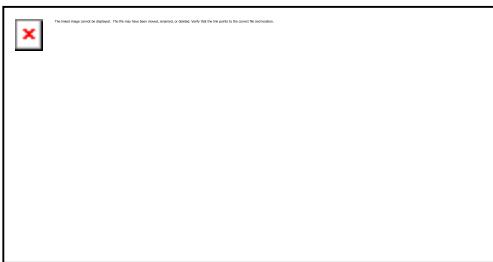


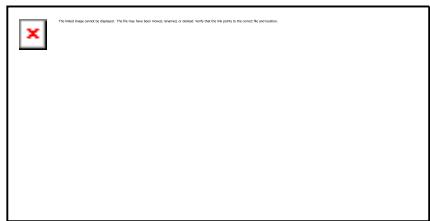


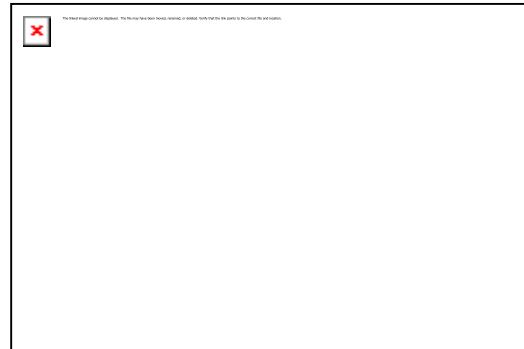
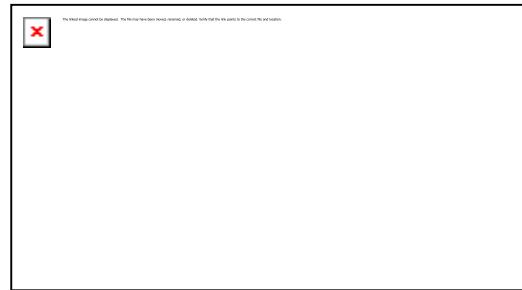


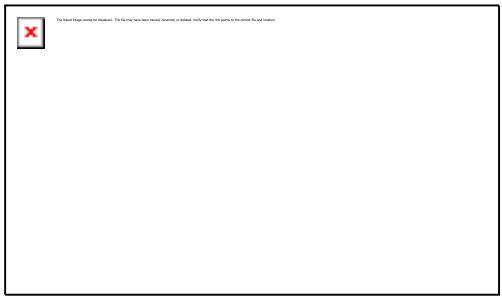




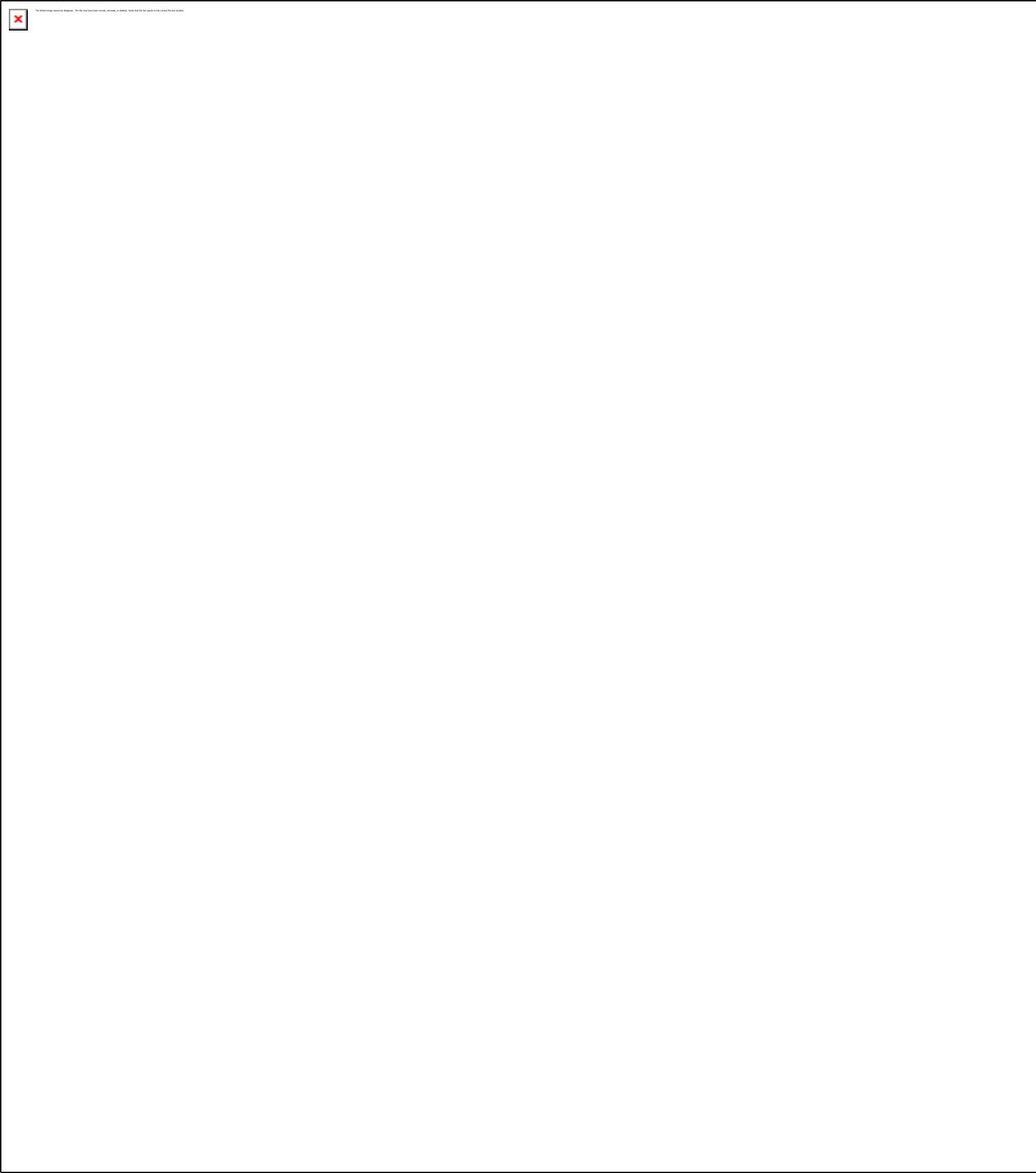


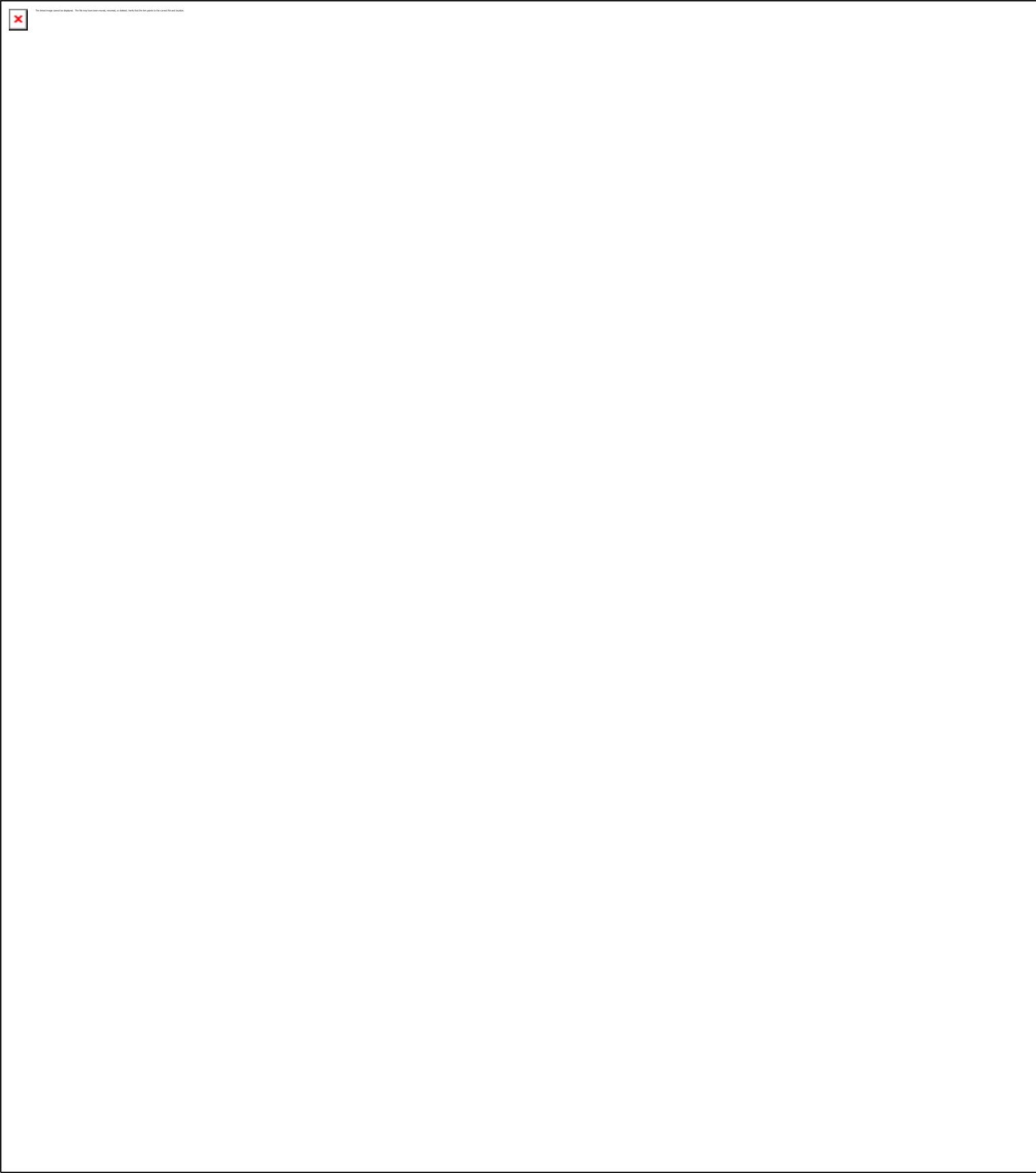


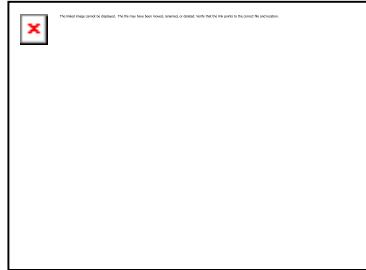










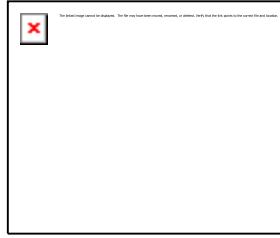
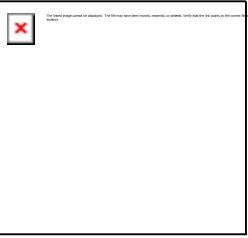




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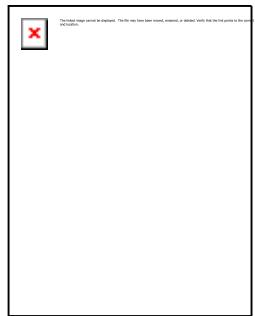


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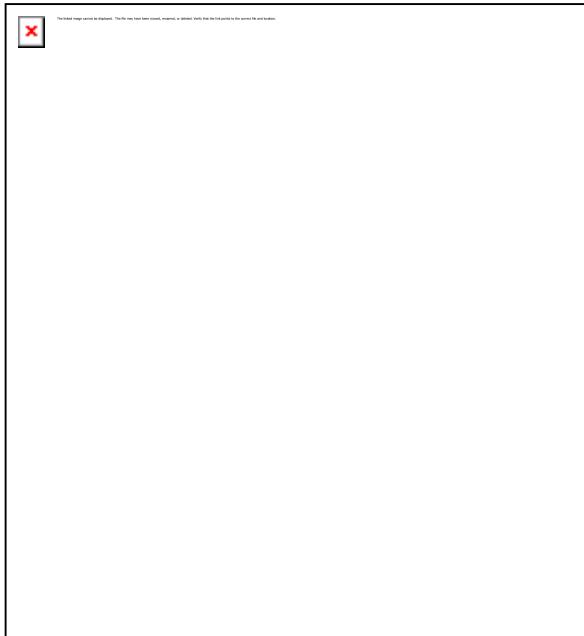
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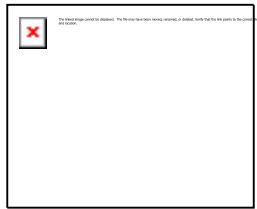
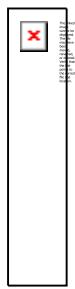
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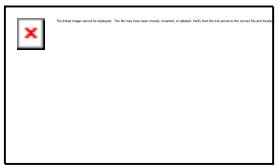
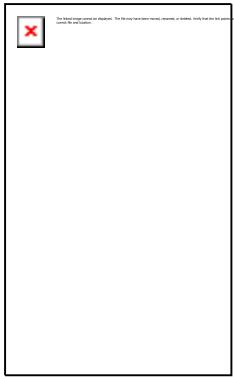


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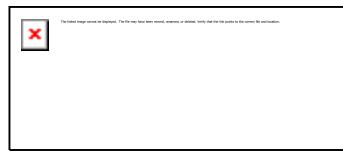




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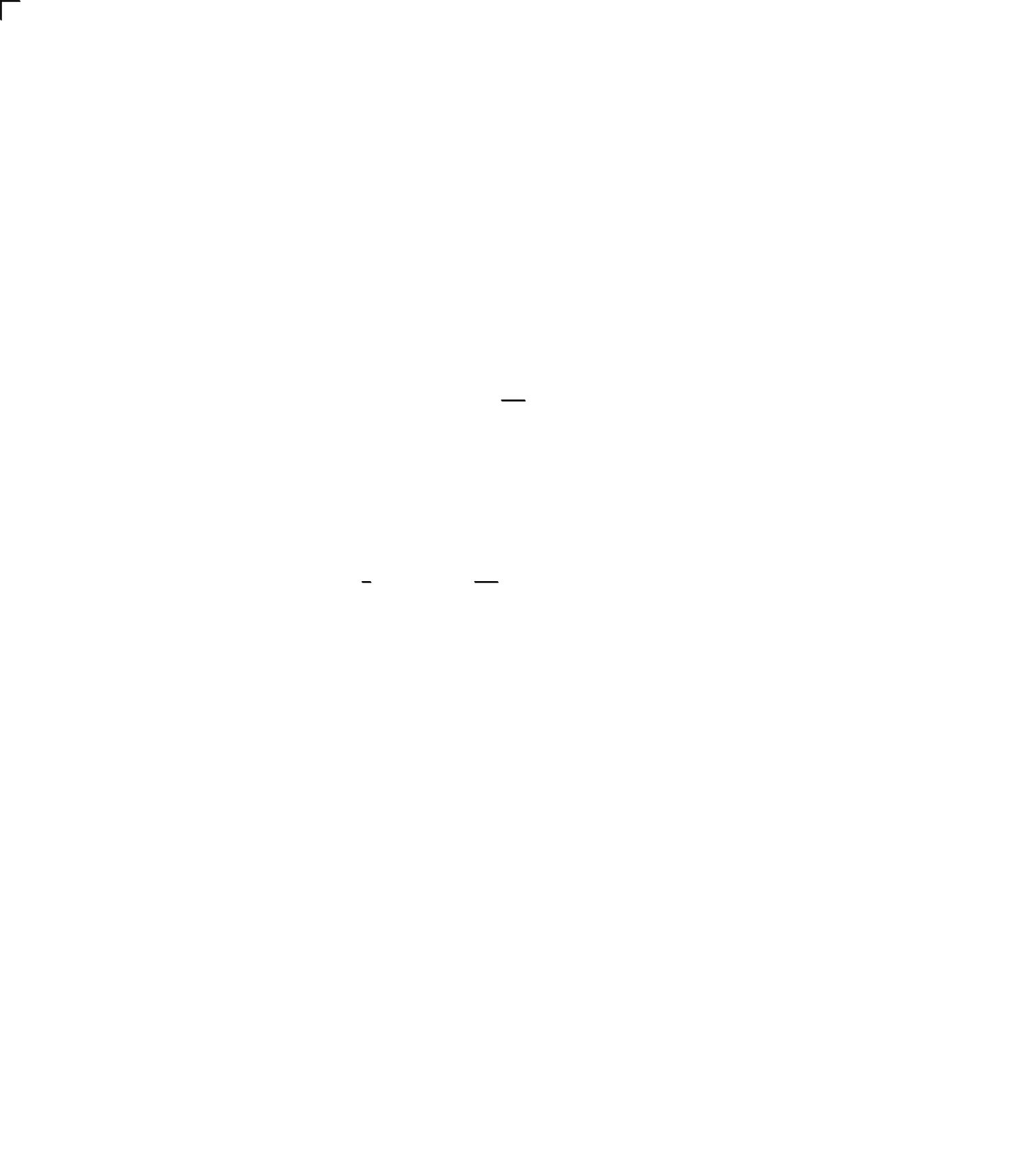


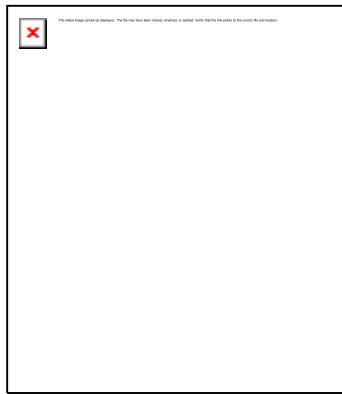
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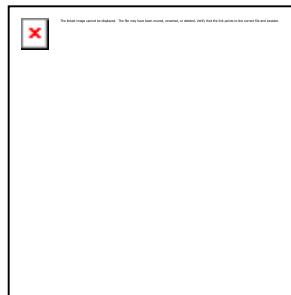
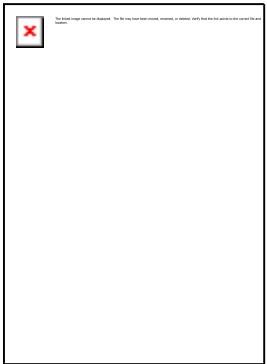
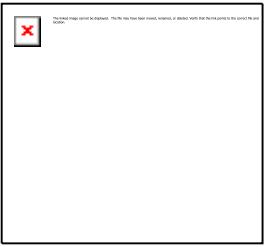


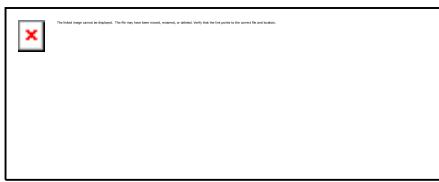
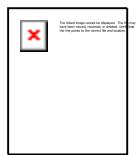
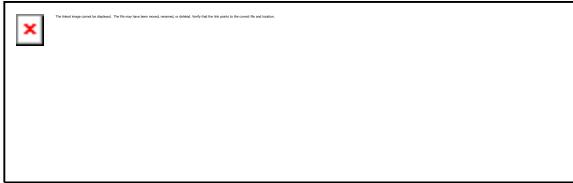
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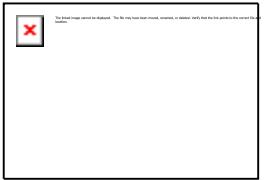


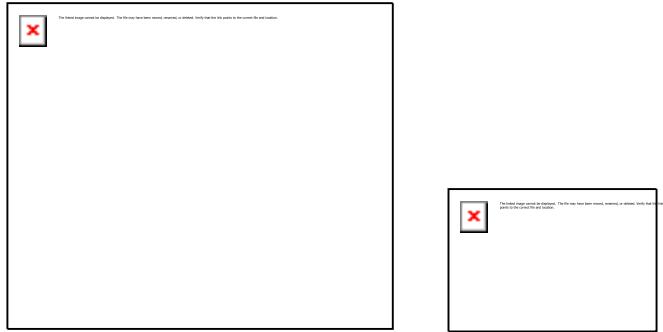
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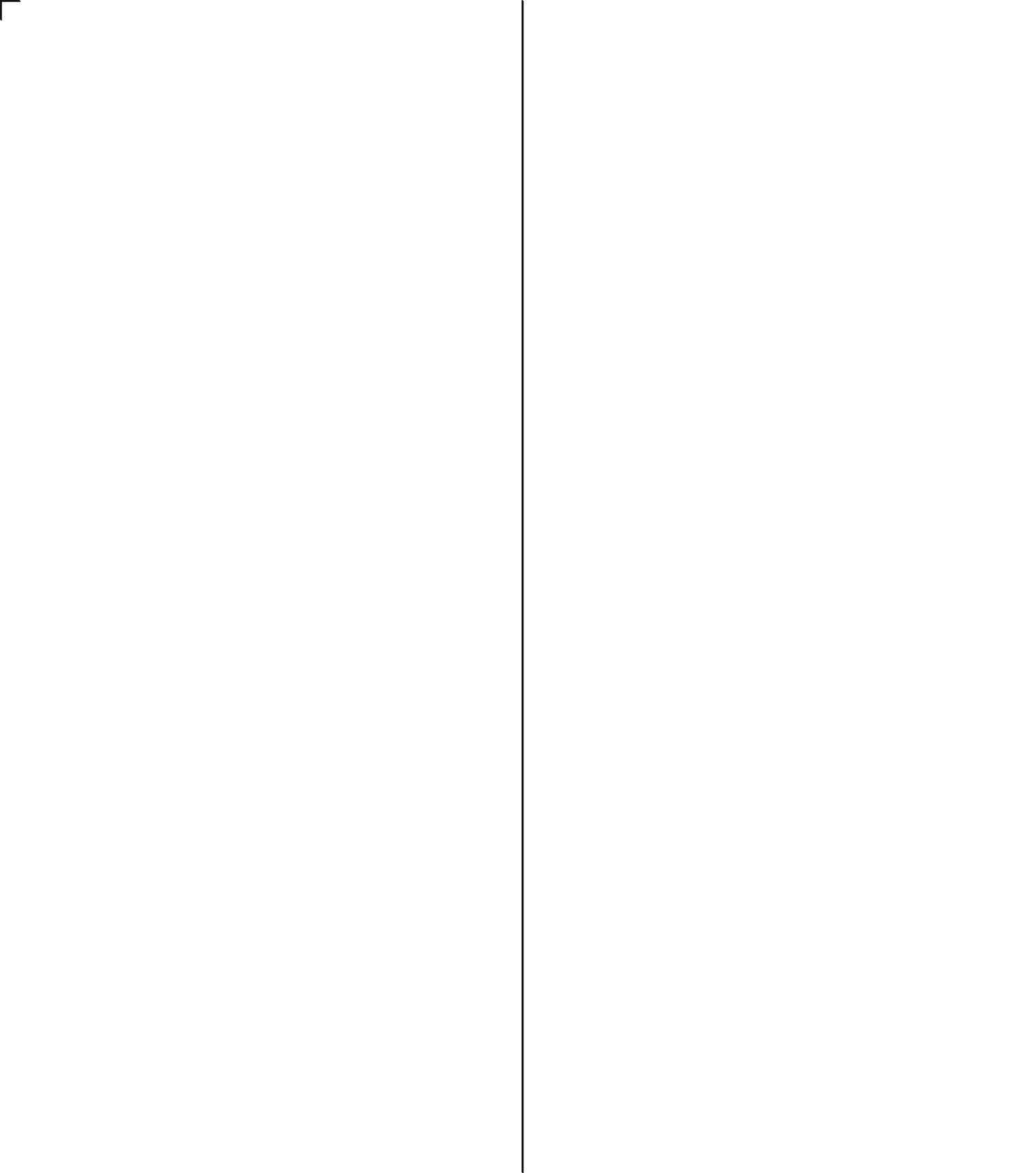


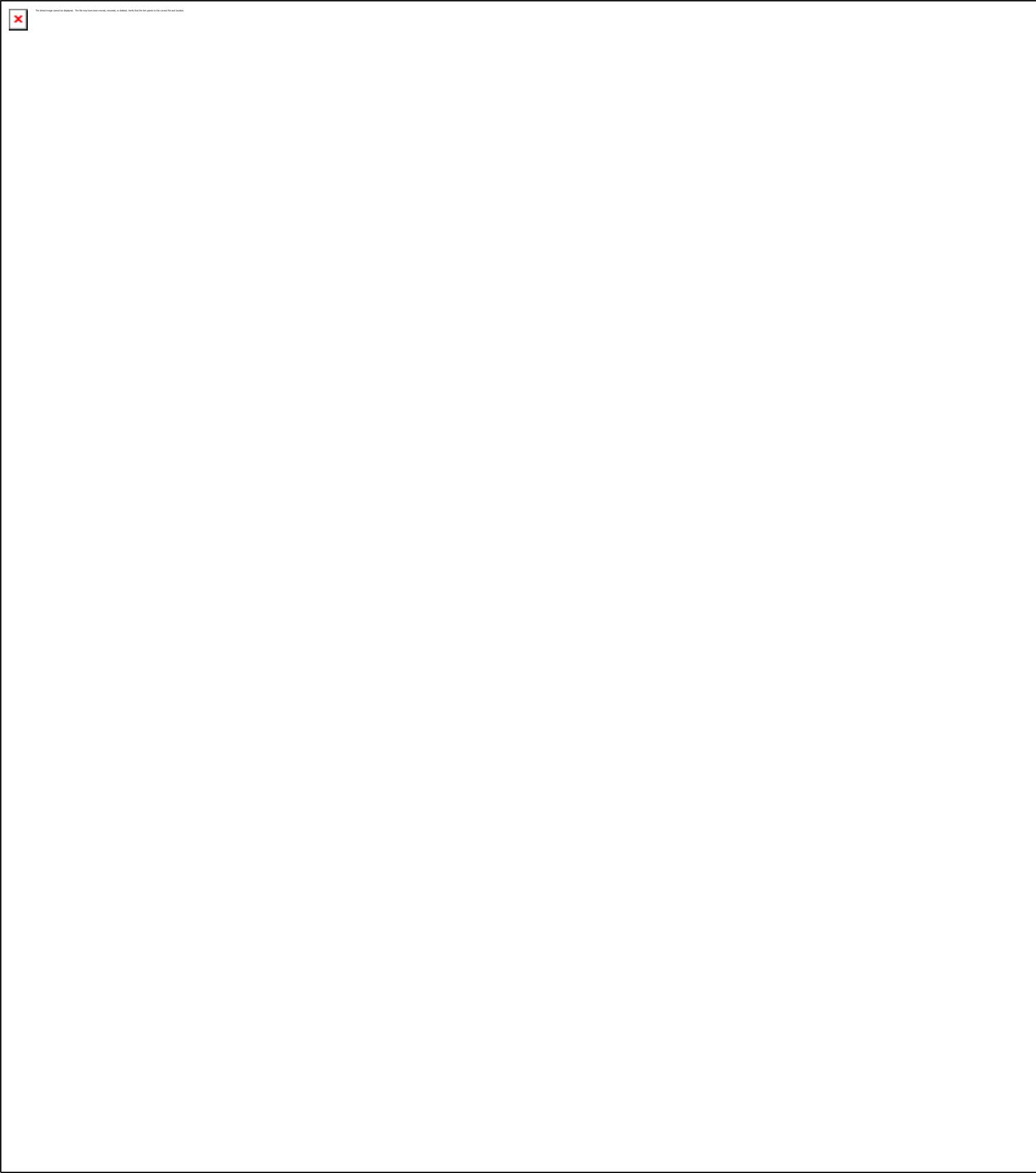




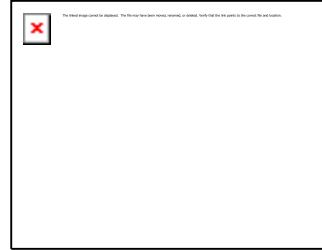










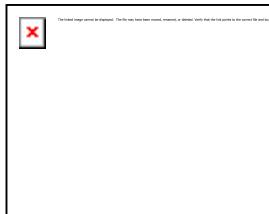


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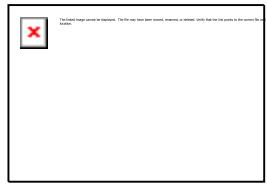
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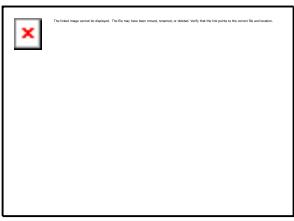




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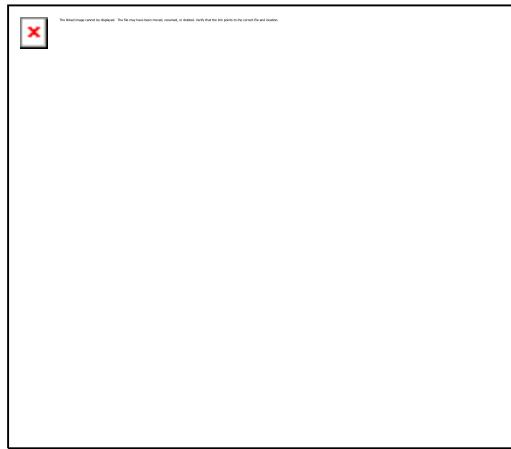
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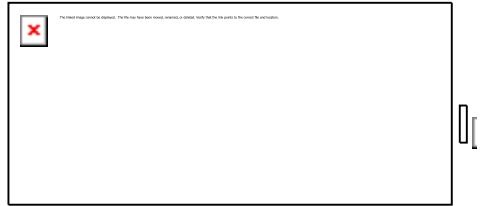


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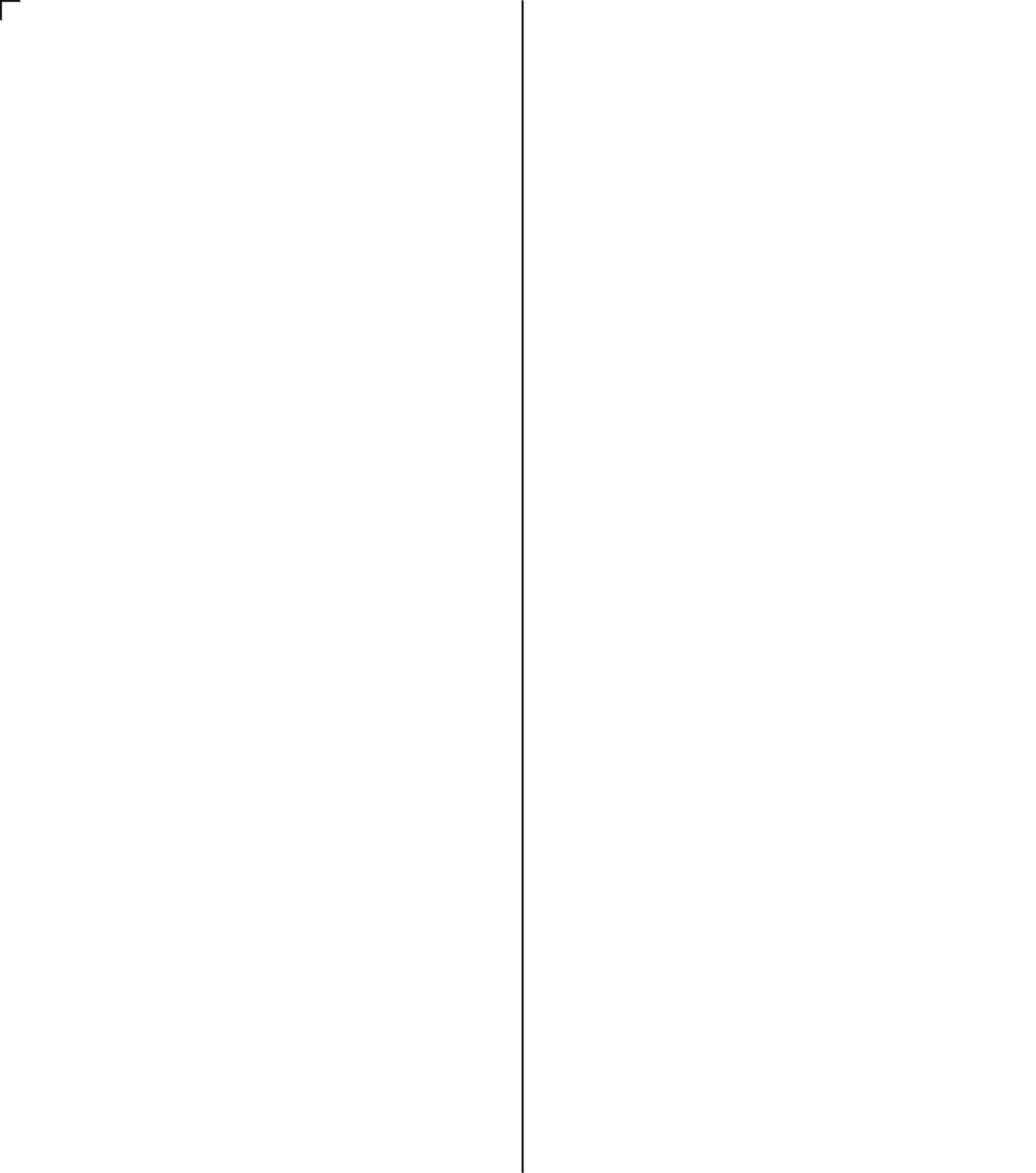
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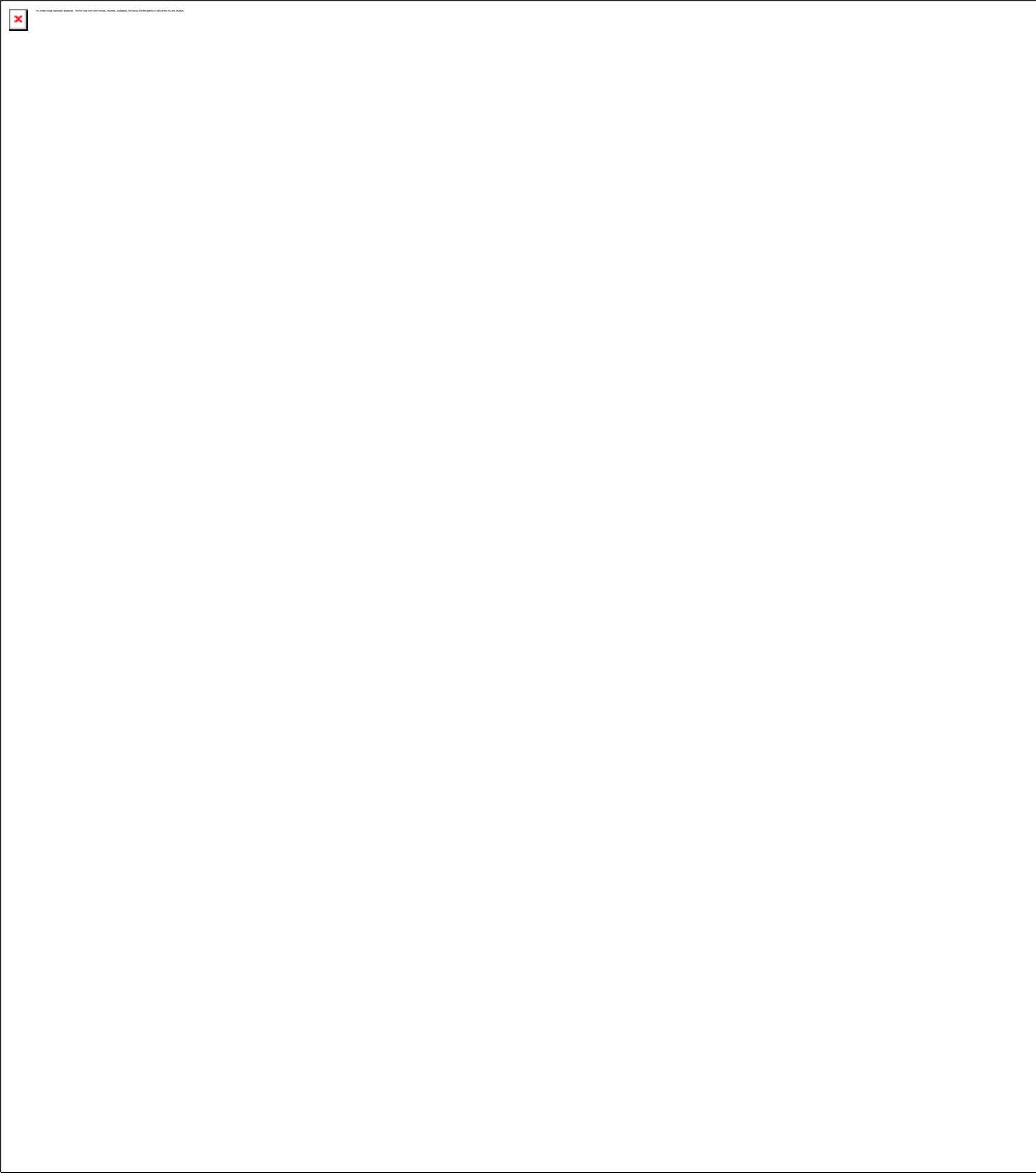
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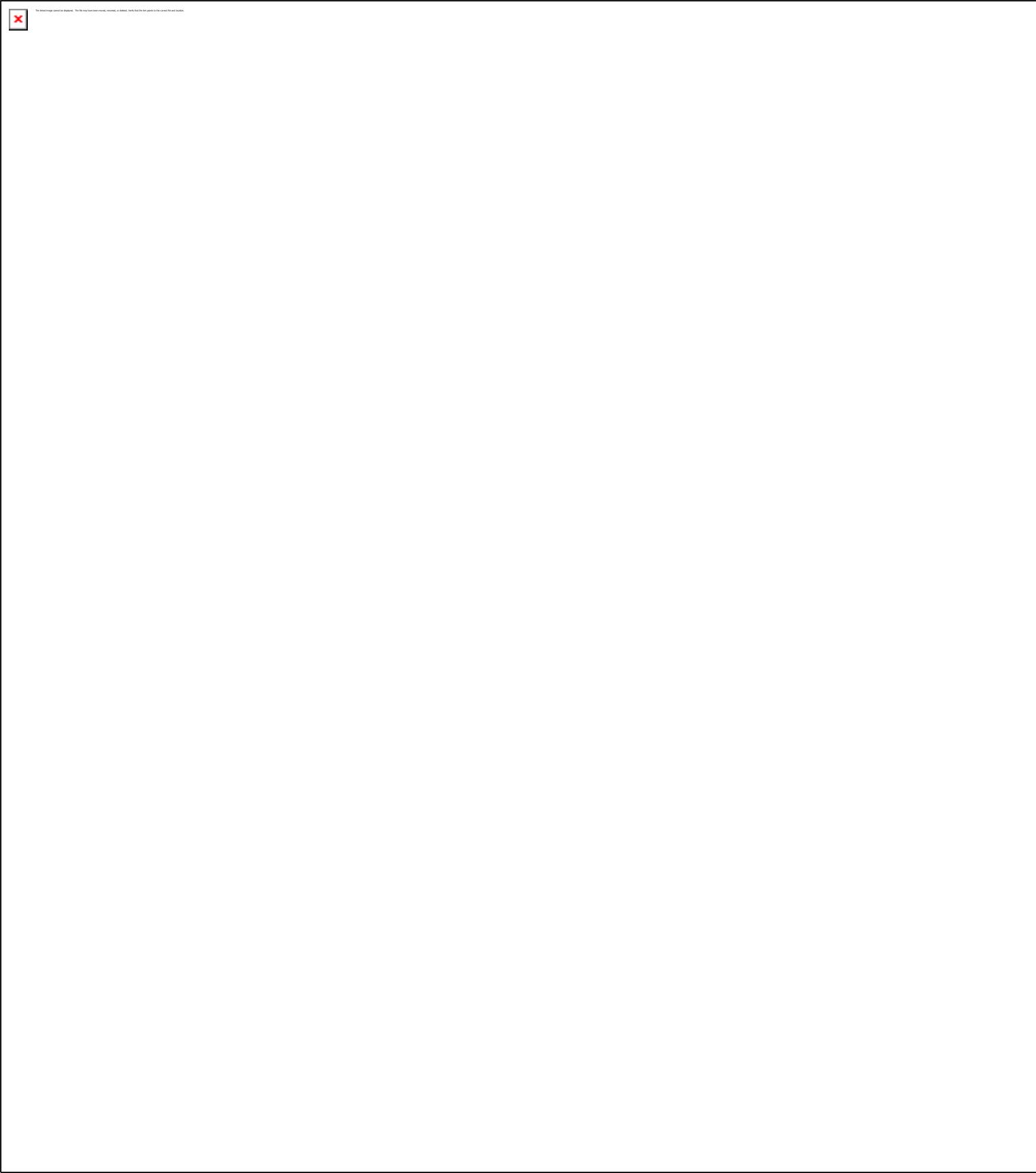


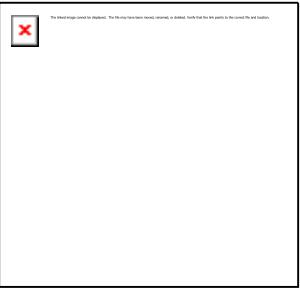


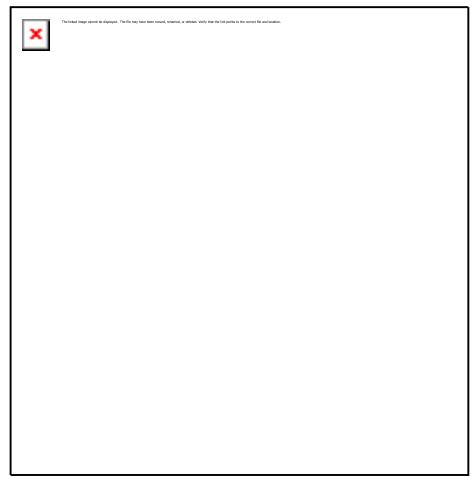












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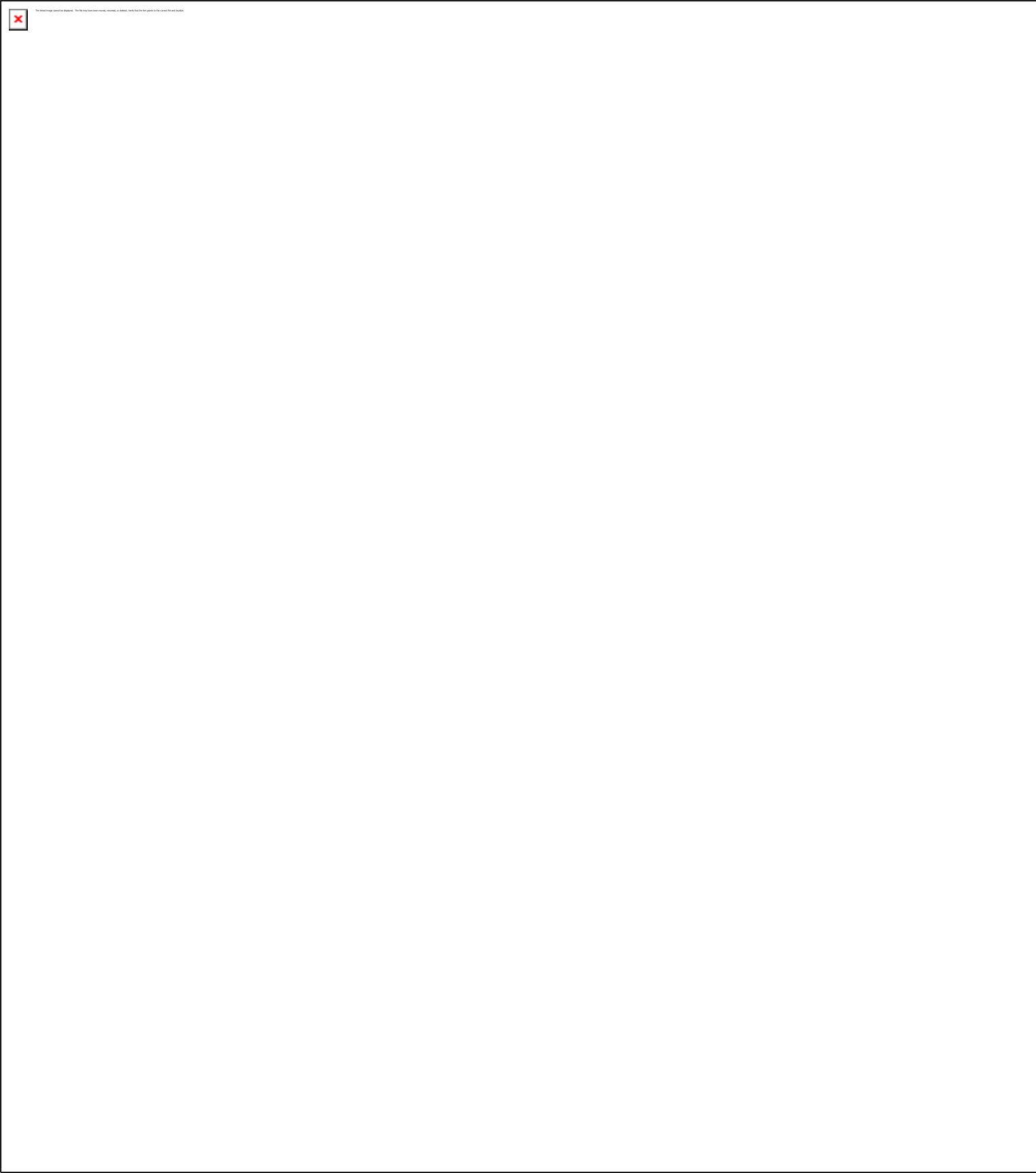
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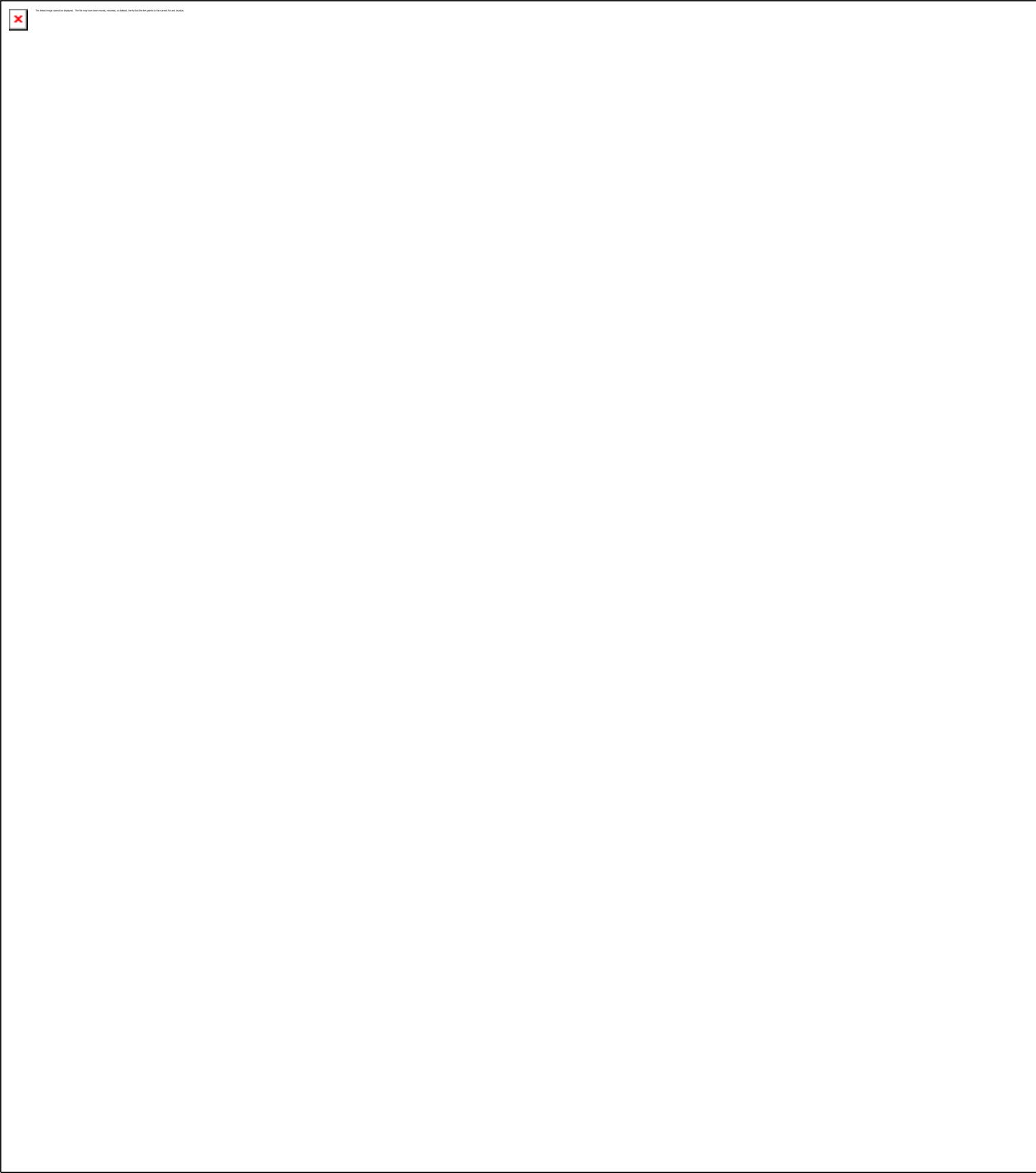
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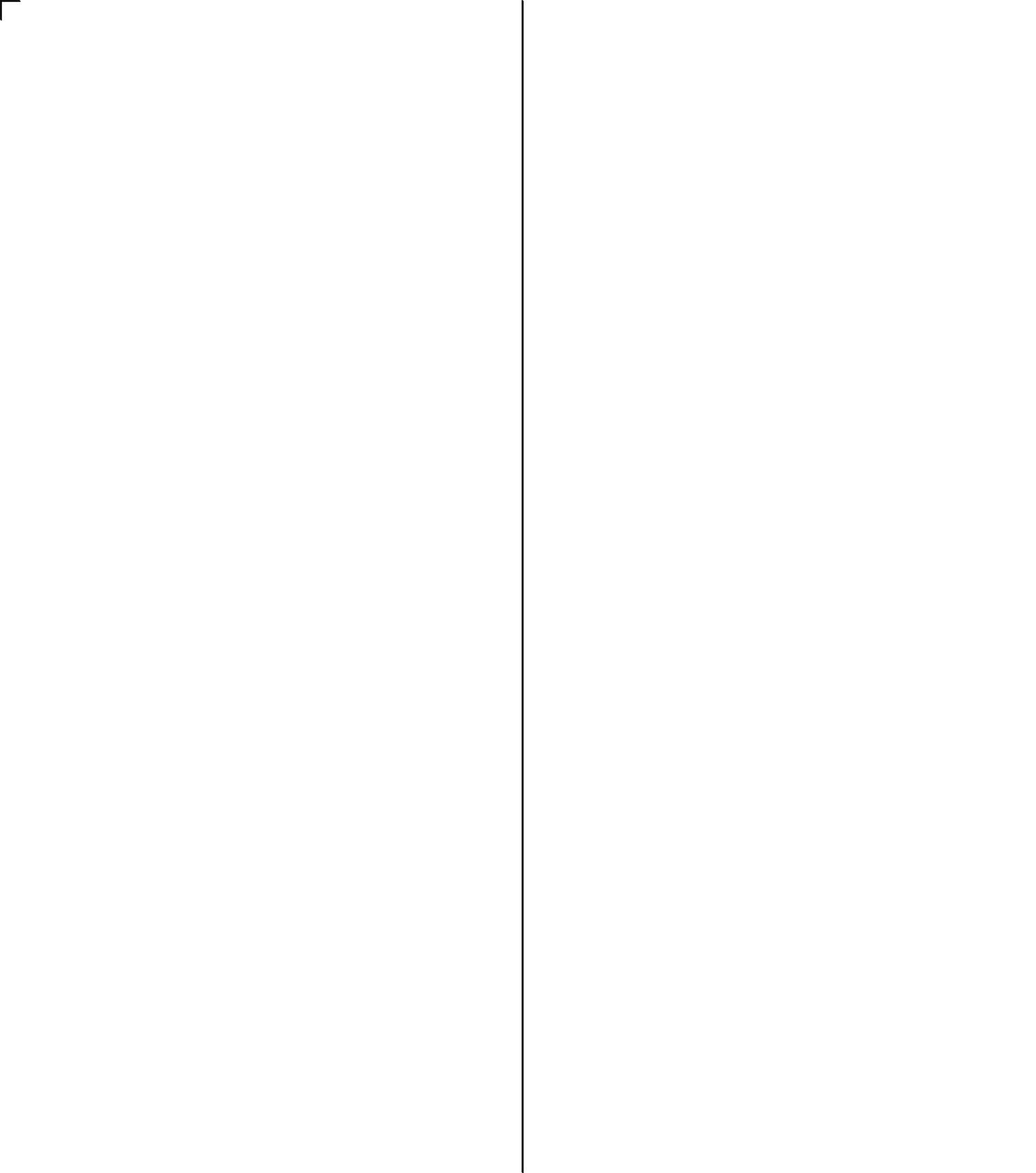
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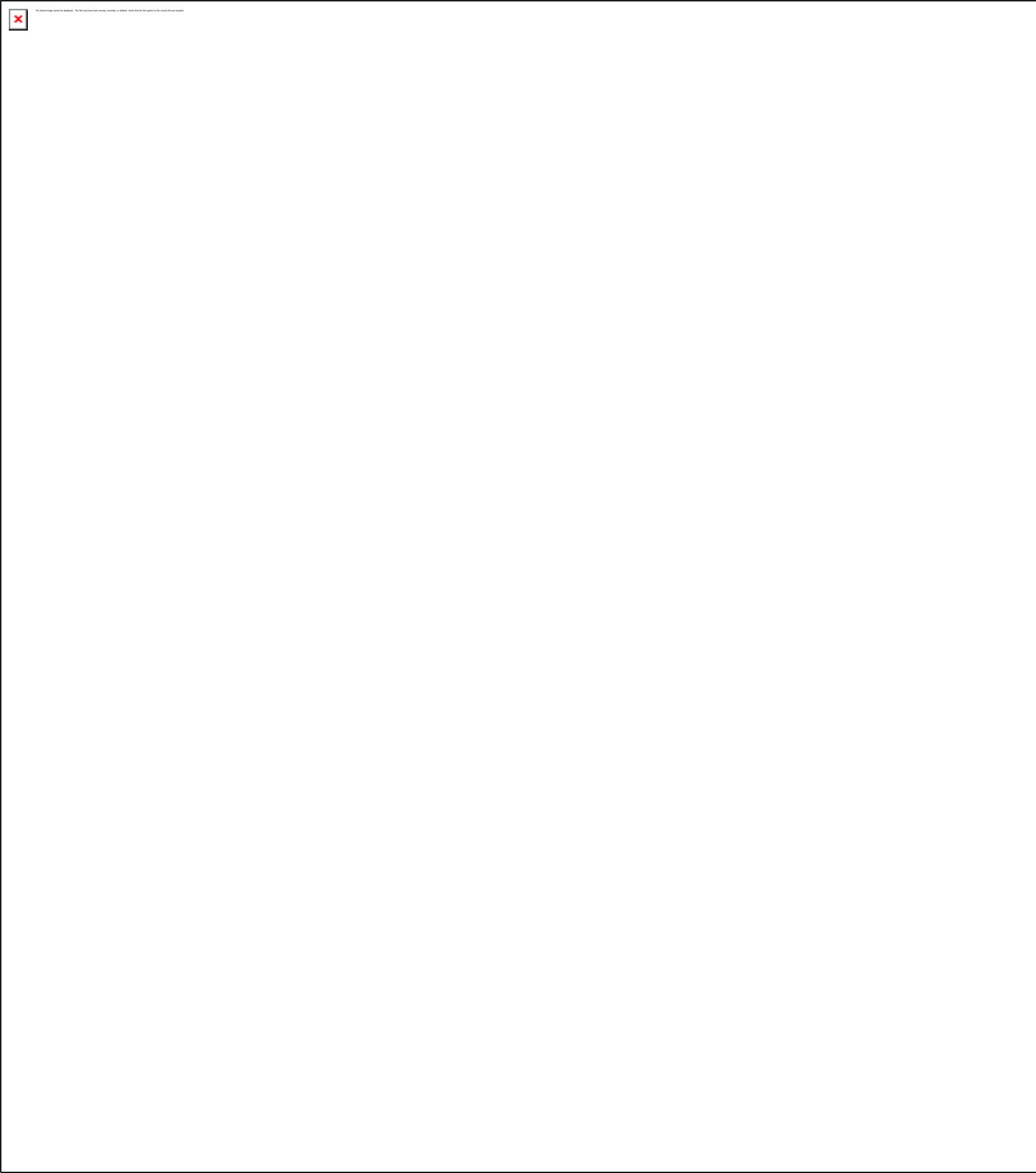
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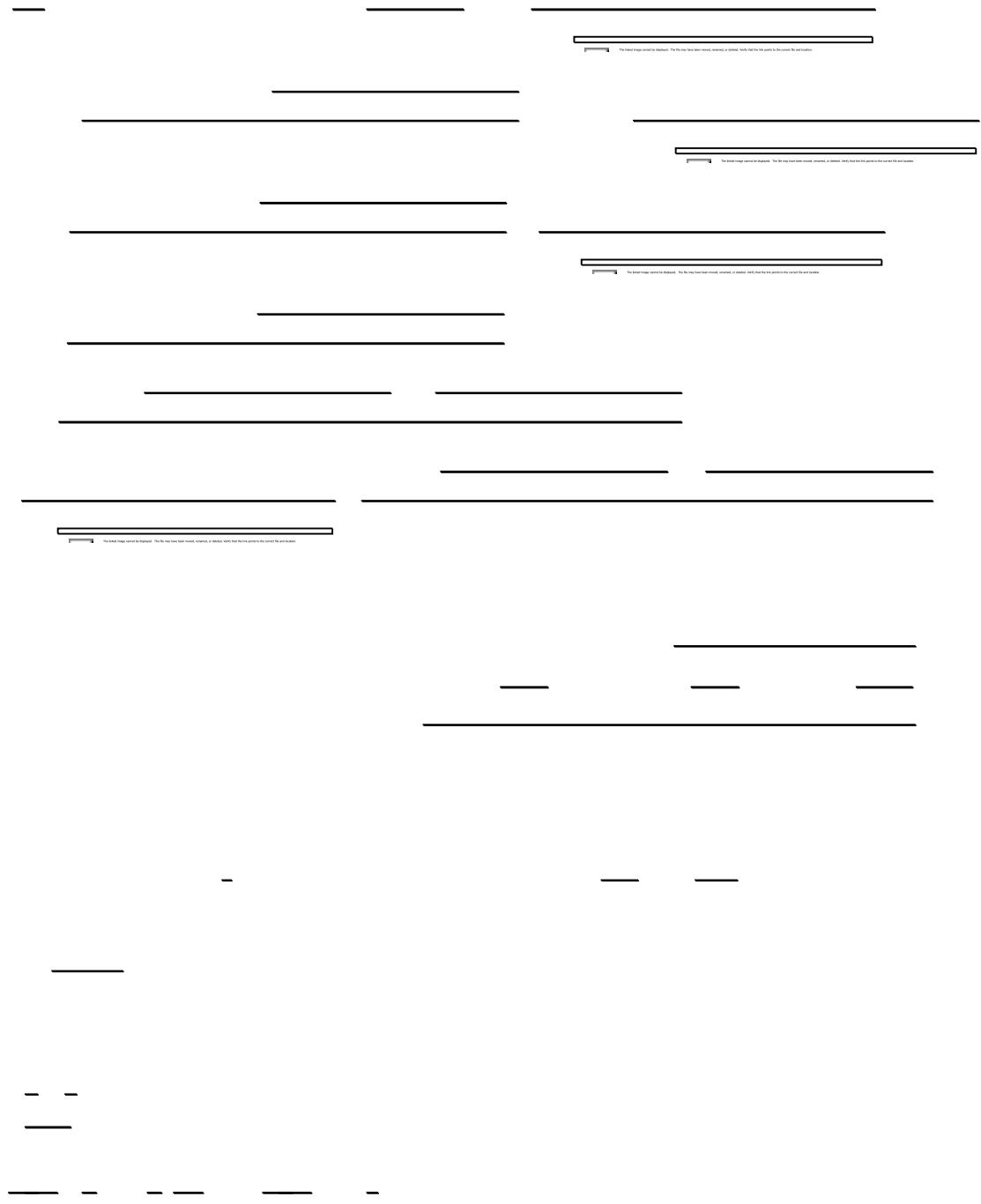
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$$\text{Pr8.3 } -3RKV_{2IN}$$

$$VS - .5KR(V_{IN} - VT)^2 - VT(V_{IN} - VT)$$

$$\text{Pr8.5 } (a) \frac{V_o}{V_i} = \frac{-\beta R_L}{R} \quad (b) V_{VOI} = R \frac{-\beta R_L R_I}{(R + R_2)}$$

$$\text{Pr8.7 } \sqrt{2VSKR} = 2VTKR$$

$$\text{Pr8.9 } (b) V_{OUT} = \frac{1}{KRS} + V_I - VT - \frac{2}{KRS(V_{IN} + VS - VT) + }$$

$$(d) \frac{dV_{OUT}}{dV_{IN}} = \frac{1}{K^2 R^2 S}$$

(e) $V_{IESTTEST}$ = R_S (f) infinite

-12

$$\text{Pr8.11 } (b) \frac{R_L R_E}{R_L + R_E} K(V_{IN} - VT)$$

$$\text{Pr8.13 } (a) V_O = 1 + \frac{V_I - R_0.6I}{(\beta + 1)R_E} \text{ and } I_E = \frac{V_I - 0.6R_L}{R_E + (\beta + 1)}$$

$$(c) \frac{V_O}{I} = 1 + \frac{1}{R_L}$$

$$(d) r_o = (R_E R_I) / \frac{1}{1 + \beta R_E R_I} \frac{R}{I}$$

and $i = R_L + \beta R_E$

$$(f) r_{ob} = (\beta + 1)R_E + R_O \text{ and Power Gain} = (\beta + 1)^2 (R_E + R_O) \frac{R_E^2}{2R_L + (\beta + 1)R_E R_O} \frac{1}{R_O}$$

chapter 9

Ex9.1 (a) $3/4\mu F$ (b) $4\mu F$ (c) $4/3\mu F$

chapter 10

Ex10.1 $i_1(t) = \frac{4}{3} e^{-t/\tau}$ mA for $t \geq 0$; $\tau = 3$ ms

Ex10.3 -5 volts

Ex10.5 (a) $v = 6e^{-t/\tau}$, $\tau = 500\mu s$ (b) $i = (6 \times 10^{-3})e^{-t/\tau}$, $\tau = 2\mu s$ (c) $v = 6e^{-t/\tau}$, (e) $i = (6 \times 10^{-3})e^{-t/\tau}$, $\tau = 1\mu s$

Ex10.7 (a) For $0 \leq t \leq 0$, $v = RI(1 - e^{-t/RC})$, and for $t > 0$, $v = RI(1 - e^{-t_0/RC})e^{-(t-t_0)/RC}$ $\tau = 1\text{ms}$

Ex10.9 2A

Ex10.11 $v_C = 2(1 - e^{-t/\tau})$, for $\tau = \frac{20}{3}$ ms

Ex10.13 $v_C = 1 + e^{-t/\tau}$

Ex10.15 (a) $C_{EQ} = 1\mu F$ (b) $\tau = 1\text{ms}$, $v_0(t) = 1 - e^{-t/\tau}$ (c) $v_0(t) = 1 - e^{-t/\tau}$; $\tau = 1\text{ms}$ for $t > 0$

Ex10.17 $v_0(t) = \frac{10}{5} e^{-t/\tau}$, $\tau = \frac{R}{5}$

Ex10.19 (A) $v_0(t) = 10 V(1 - e^{-t/\tau})$; $\tau = R \cdot C$, (B) $v_0(t) = 10V \frac{R}{R+R} e^{-t/\tau}$; $\tau = R \cdot C$, (C) $v_0(t) = 10(1 - e^{-t/\tau})$; $\tau = L/R$, (D) $v_0 = \frac{-10}{RC} t$

Ex10.21 (a) (i) $\tau = 1\text{s}$ (ii) $v_0 = 10e^{-t/\tau}$; $\tau = 1\text{s}$ (b) (i) $\tau = 1\mu s$ (ii) $v_0(t) = 5(1 - e^{-t/\tau})$; $\tau = 1\mu s$

Ex10.23 (a) $v_C = A(t - RC) + (V_0 + ARC)e^{-t/RC}$ $u_1(t)$ (b) $v_C = B(1 - e^{-t/RC})$

(c) $v_C(t) = AT + ARC e^{-t/RC} - 1 e^{-(t-T)/RC}$

$$\text{Pr10.1} \quad \boxed{\text{Vs}-\text{VR}_{\text{HON}}} \quad \boxed{\text{VL}-\text{V}} \frac{\text{RON}}{\text{S}\text{RON}+\text{RL}} \quad \boxed{\text{RONRL}}_{\text{GS}\text{RON}+\text{RL}}$$

(a) $t_{rise} = -t \ln \frac{\text{Vs}-\text{V}}{\text{Vs}-\text{VR}_{\text{HON}}}$ $\tau = \text{RLCGS}$, $t_{fall} = -t \ln \frac{\text{Vs}-\text{V}}{\text{Vs}-\text{VR}_{\text{HON}}}$ $\tau = \text{C}$
(b) $t_{pd} = 8.2\mu s$

$$\text{Pr10.3} \quad \boxed{\text{VL}-\text{V}} \frac{4\text{RON}}{\text{S}^4\text{RON}^2+\text{R}} \quad \boxed{\text{Vs}-\text{V}} \frac{4\text{R}}{\text{S}^4\text{RON}^2+\text{R}} \quad \boxed{\text{E}}$$

(a) A, B, C, and E must all be high and D must be low (b) $t_{fall} = -t \ln \frac{\text{Vs}-\text{V}}{\text{Vs}-\text{VR}_{\text{HON}}}$

$$\tau_{fall} = \text{CGS} \frac{4\text{RONRL}}{4\text{RON}} \quad \text{(c) } t_{rise} = -t \ln \frac{\text{Vs}-\text{V}}{\text{Vs}-2\text{VR}_{\text{HON}}}$$

$$\boxed{\text{Vs}-\text{V}} \frac{4\text{RON}}{\text{S}^2\text{RON}+\text{RL}}$$

$$\text{Pr10.5} \quad \boxed{\text{Vs}-\text{VR}_{\text{HON}}} \quad \boxed{\text{Vs}-\text{VR}_{\text{HON}}} \quad \boxed{\text{Vs}-\text{VR}_{\text{HON}}}$$

(a) $t_{rise} = -t \ln \frac{\text{Vs}-\text{V}}{\text{Vs}-\text{VR}_{\text{HON}}}$ $\tau = n \text{CGSRL}$ (b) $t_{rise} = n8.2\mu s$ (c) $t_{rise} = -t \ln \frac{\text{Vs}-\text{V}}{\text{Vs}-\text{VR}_{\text{HON}}}$
(d) $t_{rise} = (0.9 + n90.3)\mu s$

$$\text{Pr10.9 } v = -1V \text{ for } 2 < t < 3 \text{ and } v = -1/2V \text{ for } 3 < t < 5$$

$$\text{Pr10.11 } 0 < t < t_1: v_o(t) = \frac{V}{RC} t, t_1 < t < t_1 + t_2: v_o(t) = Vt_1 - \frac{Vt_1}{RC - (RC)^2} (t - t_1)$$

$$\text{Pr10.13 (a)} i_{AVG} = CVAf_0 \quad \text{(b)} R = i_{AA} = \frac{v}{Cf_0}$$

$$\text{Pr10.17 } v_L = \tau K(1 - e^{-t/\tau}), v_R = Kt - \tau K \quad 1 - e^{-t/\tau} \quad \tau = L/R$$

Pr10.19 (a) not true (b) true

Pr10.21 First: $v_o = e^{-t/\tau}$, Second: $v_o = 1 - e^{-t/\tau}, \tau = 0.5\text{ms}$

$$\text{Pr10.23 (a)} v_B = v_A \quad \frac{R}{R_1 + R_2} \quad 1 - e^{-t/\tau}, \tau = \frac{R_1 R_2 C_1 C_2}{R_1^2 + R_2^2} \quad \text{(b) (i)} v_B(0-) = 0 \quad \text{(ii)} v_B(t \rightarrow \infty) = v_A \quad \frac{R_2}{R_3 + R_2}$$

$$\text{Pr10.27 } v_R = (K_2 - K_1)e^{-t/\tau} + K_3 \tau \quad 1 - e^{-t/\tau}$$

$$\text{Pr10.29 (a)} V_S \quad \text{(b)} T_{min} = -CM(RL + R_{ON}) \ln 1 - \frac{V_H}{V_S} \quad \text{(c)} \frac{R_{ON}}{R_{ON} + RL} V_S \quad \text{(d)} T_{min} = -CM R_{ON} + R \frac{R_{ON} RL}{R_{ON} + RL}$$

$$\frac{RON}{RON+RLVS} \quad \frac{V_L - R_{ON} + RLVS}{RL + RLVS} \quad \frac{RL}{RON} \quad \frac{RON}{RON+RLVS} \quad \frac{RON RL}{RON + RL}$$

$$\ln \left[\frac{V_L - R_{ON} + RLVS}{RL + RLVS} \right] = -CM R_P \ln \frac{V_L}{V_S}$$

chapter 11

$$\text{Ex11.1 (a)} P_{\text{steady-state},0} = 0, \quad \text{(b)} P_{\text{steady-state},1} = R_{ON} \frac{V_{2S}}{+RL}, \quad \text{(c)} P_{\text{static}} = 2 \frac{V_{2S}}{(RL + R_{ON})} P_{\text{dynamic}} = (RL + R_{ON}) \frac{V_{2S} R_2 L C_L) 2T}{V_{2S} R_2 L C_L) 2T}$$

(d) (i) halved, (ii) quartered, (iii) halved, (e) Maximize R_L while looking out for dynamic constraints

$$\text{Pr11.1 (b)} R_S \frac{V_2}{V_2 - T_1 + T_2 + T_4} \quad \text{(c)} T_4^S (C_G + 2C_L) \quad \text{(d)} P_{\text{static}} = 2.9 \text{mW}, P_{\text{dynamic}} = 87.5 \mu\text{W}, \text{(e)} 0.18 \text{J} \quad \text{(f) 51\%}$$

$$\text{Pr11.3 (b)} P_{\text{static}} = \frac{N}{2} \frac{V_S^2}{RL + R_{ON}}$$

chapter 12

$$\text{Ex12.1 (a)} 2\alpha = \frac{1}{RC}, \omega_0 = LC \quad \text{since } \alpha < \omega_0, \text{ underdamped, (b)} v_C = Ke^{-\alpha t} \cos(\omega d t + \phi), \omega d = \omega_0^2 - \alpha^2, \quad \phi = \tan^{-1} \frac{\alpha}{\omega_0}, \omega_0 = 10 \times 10^6, \alpha = 3.33 \times 10^6, \text{(c) } v_C \text{ in RC circuit decays as } e^{-t/RC}, \text{ while } v_C \text{ in RL circuit decays with "envelope" } e^{-t/2RC}$$

$$\text{Ex12.3 } t = 0_+: i_1 = 2A, v_1 = 6V, i_2 = 3A, v_2 = 6V, i_3 = 4A, v_3 = 4V, i_4 = 1A, v_4 = 4V. \text{ Att} = \infty: i_1^l = 10A, v_1^l = 0, i_2^l = 0, v_2^l = 0, i_3^l = 10A, v_3^l = 10V, i_4^l = 0, v_4^l = 10V$$

$$\text{Ex12.5 } \frac{dv}{dt} |_{t=0} = 2V/s, \frac{di}{dt} |_{t=0} = 3 \frac{1}{A/s}$$

$$\text{Ex12.7 (a)} x_1 = e^{-2t} + e^{-4t}, \quad x_2 = e^{-2t} - e^{-4t}, \quad \text{(b)} x_1 = 2\cos(4t), \quad x_2 = 2\sin(4t)$$

Pr12.1 with small inductor: $v_C(t) = IR - \frac{LIR}{R+2C}e^{-\frac{Rt}{L}} + \frac{IR^2C}{R+2C}e^{\frac{-Rt}{L}}$, without inductor: $v_C(t) = IR - \frac{1}{1-\frac{RC}{L}}e^{-\frac{Rt}{L}}$.

Pr12.3 (a) $i_1 = \frac{L_2}{M_2-L_1L_2} R_{11}i_1 - RM_2 + M(M_2-L_1L_2)$ $i_2 = \frac{L_2}{M_2-L_1L_2}$ vs, $i_2 = \frac{-M}{M_2-L_1L_2} R_{11}i_1 + \frac{R_2L_1}{M_2-L_1L_2} i_2$
 $\frac{M}{M_2-L_1L_2} v_S$, (c) $v_2(t) = 0.05e^{-20202t} - 0.05e^{-20000t} u(t) - 0.05e^{-20202(t-0.005)} - 0.05e^{-20000(t-0.005)}$

Pr12.5 (a) $CA \frac{dv}{dt} + \frac{v_A - v_B}{R} = K(V_0 - V_B)i_2$, $C \frac{dv}{dt} + \frac{v}{R} = \frac{v_A - v_B}{R_A}$, (b) $i_s = -2K(V_0 - V_B)v_b$, (c) Overdamped

chapter 13

Ex13.1 P(a) HMA SEAG == 78° 16.8°, (d) MPAG HASE == 47.6° MAG == 45.47, PHASE == 18°, (c) MAG == 2136,

Ex13.3 $\frac{V}{I} = \frac{R}{Ls+R} = \frac{RLi\omega}{(L\omega)^2 + R^2} e^{j(\omega t + \phi)}$, $\phi = \tan^{-1} \frac{R}{\omega L}$

Ex13.5 $Z = j\omega \overline{RC} + \frac{1}{\overline{RC}} = 104 \text{ rad/s}$, $R = 100$, $C = 1 \mu\text{F}$

Ex13.7 $Z_s = j\sqrt{\frac{1}{\omega^2}}$

Ex13.9 $\frac{R}{\Sigma} = 2 \times 10 \text{ rad/s}$, $\frac{V(j\omega)}{I(j\omega)} = R + L\omega j$

Ex13.11 (a) $\frac{V}{V_0} = \frac{1}{(j\omega RC)^2 + R^2}, \phi = \tan^{-1}(-RC\omega)$, (b) $\frac{V_0}{V_i} = \frac{j\omega L}{R((\omega L)^2 + R^2)} e^{j\phi}, \phi = \tan^{-1} \frac{R}{\omega L}$,
(c) $\frac{V_0}{V_i} = \frac{1}{(j\omega RC)^2 + R^2}, \phi = \tan^{-1}(-RC\omega)$

Ex13.13 (a) $\frac{V}{V_0} = \frac{1}{\frac{1}{(\omega^2)^2} + \frac{1}{2}}, \phi = \tan^{-1}(-\frac{\omega}{100})$, (d) $V = \frac{1}{\sqrt{\frac{1}{(\omega^2)^2} + \frac{1}{2}}} e^{j\phi}, \phi = \tan^{-1}(-\frac{\omega}{100})$, (b) $v_0(t) = \frac{1}{2\sqrt{2}} \cos(100t - 45^\circ) + \frac{1}{200.01} \cos(10,000t - 89.4^\circ)$

Ex13.15 (a) $\underline{V}V_{0i} = \frac{Z_2 \cdot Z_4}{(Z_2 + Z_3 + Z_4) \cdot Z + (Z_3 + Z_4) \cdot Z_2}$

(b) $\frac{I_a(s)}{V_i(s)} = \frac{Z_3 \cdot Z_4}{(Z_3 + Z_4)Z_2 + Z_2(Z + Z_3 + Z_4)}$

Ex13.17 $\frac{I_a(s)}{V_i(s)} = \frac{Y}{Y + Y_1}; Y = \frac{Y^2(Y^3 + Y)^4}{Y^2 + Y^3 Y^4}$

Pr13.1 (a)(i) $Z = \frac{R}{1+j\omega RC}$ (ii) $Z = R + j\omega L$ (iii) $Z = j\omega C - \frac{j\omega RC^2 + 1}{2C(CR + j\omega C^2)}$

Pr13.3 (c) $H(j\omega) = 0 \text{ db at } \omega = 105$ (d) $1; 10; 100; 1,000; 10,000$

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